# Production of the LHCb Silicon Tracker Readout Electronics

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*Abstract*

We give an overview on the status of production of the LHCb Silicon Tracker Electronics. Lessons learned together with the industry in the preseries production of the Silicon Tracker Digitizer Boards were integrated into the design to optimize the production and assembly yield for the main batch of 700 Digitizer Boards. A report on the preseries readout module performance and on the testing procedures for the full production lot is given. In addition, a final proton irradiation test of a complete readout system has been performed, of which results will be presented.

## I. Overview

The Silicon Tracker of the LHCb experiment [1] consists of silicon strip detectors with a pitch of around 200 µm. For the Trigger Tracker station upstream of the magnet, a 500 µm thick sensor with 512 strips is used, while the three Inner Tracker Stations after the magnet feature 320 and 410 µm thick sensors of 384 strips each. The signals are amplified and processed by the Beetle readout chip [2], which transmits its data via differential analogue lines to the Service Boxes. Here, the signal is digitised and converted into an optical signal, which is transmitted via fiber of up to 120 m length to the counting house to an optical receiver card, which is located on the Level-1 preprocessing boards. An overview of the transmission side of the readout system is shown in Figure 1.

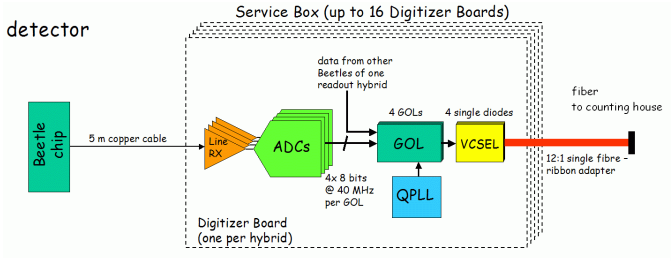


Figure 1: Overview of transmission side of the readout system.

## II. Service Box Concept

The concept of the Service Box allows a physical separation of sensor readout electronics and data transmission system. As the readout hybrids are located in the acceptance of the LHCb experiment, this reduces the amount of dead material and hence multiple scattering and generation of secondary particles. In addition, the location of the Service Boxes, which is just outside the detector's acceptance, features lower radiation levels and easier access for cooling and maintenance.

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Each Service Box holds up to 16 Digitizer Boards, which handle the signals coming from and going to the readout hybrids. As this includes not only the physics data, but also power supply, timing and slow control signals, this allows for a single cable connection between a hybrid and its associated Digitizer Board. For each Service Box, a Control card provides the interface to the experiment-wide Timing and Fast Control system (TFC) [3] and the Experiment Control System (ECS) [4]. The distribution of these signals among

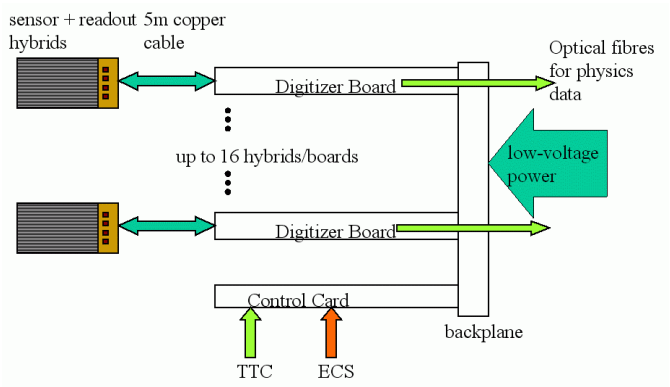


Figure 2: Schematic overview of Service Box.

the Digitizer Board within a Service Box is done with a custom-designed backplane. The backplane also carries the radiation-tolerant linear voltage regulators to supply the readout hybrids and the Service Box itself. An overview of a Service Box is shown in Figure 2.

### *A. Digitizer Board*

Any Beetle readout hybrid is connected with a 68-wire twisted-pair round cable of up to 5 m of length to a Digitizer Board. First, a line receiver converts the analogue detector signal from a differential signal into a single-sided signal. In addition to the elimination of common mode noise introduced on the cable, the line receiver matches the signal amplitude to the input of the 8-bit analogue-digital converter (ADC). Data of four ADCs, corresponding to the four analogue output ports of one Beetle are encoded by the CERN GOL chip [5] into the Gigabit Ethernet protocol and modulated onto a 850 nm VCSEL diode. The digital data is framed by using the *DataValid* signal of the Beetle readout hybrid to drive the TX_EN line of the GOL serializer. An antifuse FPGA from Actel Inc. [6] was used to form a 7-clockcycle triple-redundant shift register. This re-aligns the *DataValid* signal to the digitised data and allows for automatic re-synchronization of the optical link between physics triggers.

Two versions of Digitizer Boards have been designed: a TT version with 16 ADCs corresponding to a 4-chip TT hybrid and a IT version with 12 ADCs only to match a 3-chip IT-hybrid.

### *B. Backplane*

The Digitizer Boards are connected to the Control Card via the Service Box backplane. The distribution of timing and fast trigger signals is done via impedance controlled differential traces. Equal trace lengths were maintained to keep the time skew of the fast signals among different backplane slots minimal. For each slot, three positive linear voltage regulators provide the required voltages to the Beetle frontend hybrids , the Digitizer Boards and the Control Card. As all regulators are located close to each other, a common copper heatsink is used to dissipate the heat produced by the regulators.

### *C. Control Card*

The Control Card provides the interface of each service Box to the TFC and ECS systems. A TTCrq mezzanine [7] is used to collect clock, trigger and timing information from the TFC network. Two SPECS slave mezzanines [8] are needed to provide eight I2C busses for complete control of the GOL devices and the Beetle frontend chips associated with one Service Box, In addition, 36 I/O lines allow individual power control for each readout hybrid and for a group of four Digitizer Boards each.

## III. TESTS OF PREPRODUCTION HARDWARE

### *A. Digitizer Board (TT version)*

As communication to a PCB assembly company started rather early, some features to ease the production and assembly of the Digitizer Board were introduced into the first preproduction design:

- simple layer stack: 6 layers
- 140 x 328 $mm^2$, 1.6mm FR4
- 6 mil technology, no buried or blind vias
- minimum SMD size 0603
- standard, robust commercial connectors
- no tuning points

A first batch of 17 Digitizer Boards was produced in 2004 (Fig. 3). No JTAG chain and hence no boundary scan was included in the board's design, as the low interconnectivity between JTAG-compatible devices did not support a proper boundary scan. Before assembly, the boards were tested electrically. After assembly and visual inspection, all five BGA device on each board were X-rayed to verify the BGA soldering process. No faulty solder joint was detected.

Although the basic design proved to be functional, a minor routing error was found, which connected the wrong reference voltage to the line receivers. In addition, the shift-register was determined to be one clock cycle too short, which had to be fixed on a new set of antifuse FPGA devices. Out of the 17 boards, 16 boards worked immediately. One board had a broken via underneath one GOL chip, which could be repaired manually. This was most likely caused by the asymmetric layer stack, which was used in the TT version preproduction. In addition, this asymmetry resulted in a slight warping of the Digitizer Board along its long dimension. By request from the assembly company, the board stack was changed to a symmetric design, which would eliminate the warp and as a result reduce possible problems during assembly.

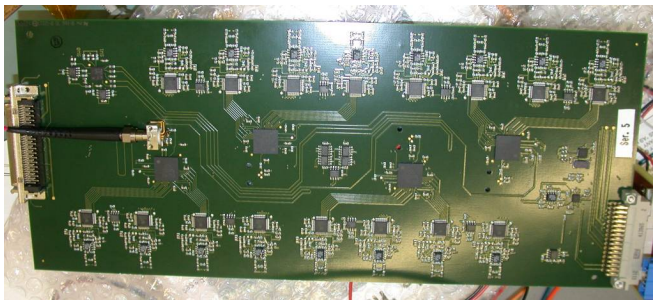

Figure 3: Photo of TT Digitizer Board.

Testing of the Digitizer Boards included a verification of the analogue performance of the first stage. Figure 4 shows a linearity plot, which was acquired by using the internal testpulse generator of the Beetle chip. For zero load capacitance at the Beetle inputs, a dynamic range of ±150.000 electronics was determined, in accordance with the specifications of the Beetle chip. The remaining non-linearity was traced to the internal testpulse generator, which itself is not perfectly linear.

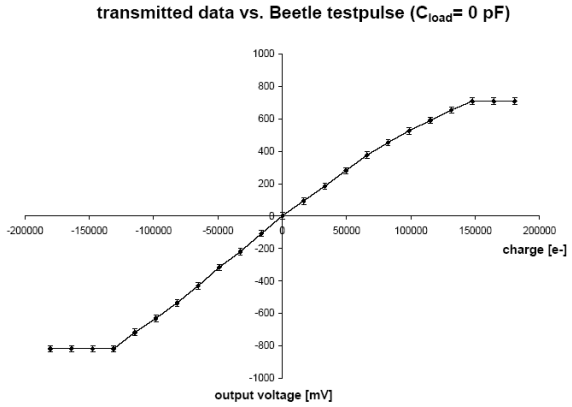


Figure 4: Linearity of the Beetle + Digitizer Board.

With up to 16 ADCs on one board, the synchronicity of the sampling points of the channels with respect to each other had to be verified. Channel-to-channel skew for the analogue signals was minimized as much as possible by using equal trace lengths from the input connector to the ADCs. Furthermore, the sampling clock for the ADCs is distributed symmetrically via a dedicated clock tree having its root located centrally on the board. For measuring the synchronicity, a digital signal edge was connected to all input channels in parallel. The sampling point was now shifted with respect to this signal edge by using the internal clock delays of a TTCrx, which was located on a reduced version of the Control Card. When plotting the averaged ADC value transmitted by the readout system for different clock delays, the spread of the sampling points can now be shown in Figure 5. A spread of less than 2 ns could be achieved, which is considered to be excellent compared to the flat top length

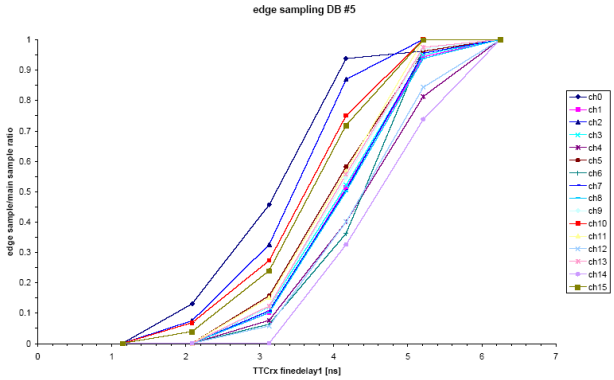


Figure 5: Sampling synchronicity of 16 channels.

of a Beetle signal of around 15 ns.

## *B. Backplane*

Initially, only two backplanes with 8 slots each were produced to provide a testbed for the preproduction of the Digitizer Boards. In addition, these backplanes served as prototypes for further testing. In this first version, the power supply planes and traces were found to be of too small cross section, which led to an unacceptable high voltage drop when drawing higher currents. Furthermore, it was discovered, that while the readout hybrids were switched off, the associated fast timing signals with LVDS levels were still powered and partially supplied the readout hybrids via the chip-internal protection diodes. In a second version of the backplane, which is currently in use at the system test at the University Zuerich, both these issues have been cleared by going from 4 to 6 board layers and doubling the copper thickness of the power planes from 18 µm to 35 µm.

### *C. Control Card*

The design of a fully functional Control Card version was slowed down due to the inavailability of radiation-tolerant components. Therefore, a non-radiation tolerant version with reduced functionality was developed to enable system testing of the Digitizer Boards. This version only carries a TTCrq mezzanine and a socket for direct I2C control with a commercial I2C master.

Since July 2005, a first prototype of a radiation-tolerant Control Card has been completed (Fig. 6). Although the system integration is still ongoing, preliminary results show basic functionality and compatibility with the TFC and ECS systems.

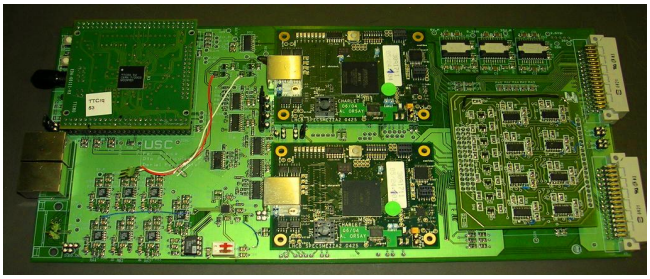

Figure 6: Control Card prototype**.**

### *D. System scale radiation test*

In Summer 2005, a final system-scale proton irradiation was performed at PSI(Switzerland) with protons of an energy of 60 MeV. Contrary to earlier irradiation campaigns, where individual components have been tested, this campaign featured a full Digitizer Board (TT version) mounted on a backplane. During the irradiation, test signals were digitized and transmitted to a monitoring setup in the counting house to verify the operation in real-time. After an integrated dose of 60 krad, equivalent to a fluence of about $4.4 \cdot 10^{11}$ p·cm$^{-2}$, no performance degradation or failure could be observed.

## IV. System-scale readout test

Starting in March 2005, a larger-scale readout system was set up at the University Zuerich. Ultimately serving as a burn-in teststand for the silicon sensor module production, this readout system momentarily consists of a TTC network, on which clock and trigger are transmitted to a Service Box loaded with 6 Digitizer Boards (Fig. 7). Of the six connected TT hybrids, up to three hybrids with 12 Beetles chips in total were digitized simultaneously and transmitted to a TELL1 board. The data then is sent via Gigabit Ethernet to a single DAQ PC, where offline analysis is done. A second TELL1 board and a LHCb Readout Supervisor for trigger control are already in place to enable rapid upsizing in the coming weeks.

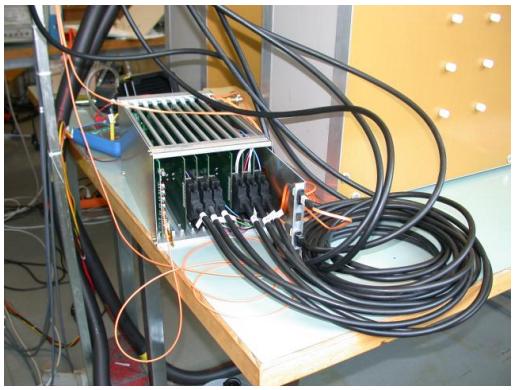

Figure 7: Service Box in system test.

## V. IT Digitizer Board preproduction

In Summer 2005, a second preproduction run was launched for 10 Digitizer Boards of the IT version with only 12 ADCs. The errors discovered in the preproduction of the TT version were included in the design as well as general updates of the application circuits of some device:

- symmetrical layer stack for PCB (non-halogen)
- fixed line receiver reference
- added QPLL RC-network for increased stability
- changed the VCSEL anode bias to 3.3 V, as 2.5 V proved to be too low
- improved firmware for antifuse FPGA (7-stage shift-register)

Very preliminary tests directly after delivery of the boards confirm basic functionality right out of the box.

## VI. Testing procedures

As the Digitizer Boards have no tuning points, testing is expected to be relatively fast. After initial test of supply currents without a readout hybrid attached, a complete transmission test with a readout hybrid can test all ADC channels in parallel. Reading back the ‘standard’ Beetle baseline also performs a check on the power supply lines, the fast signal paths and the slow control lines, which are propagating through the Digitizer Board. An additional injection of a large amplitude sinewave will be capable to test the dynamix rance of the analogue input stage of the Digitizer Board. Transmission of data over an optical fiber with an extra attenuation of 6dB provides a test for the minimum power margin for the tested VCSEL unit. The function of the antifuse FPGA shift-register is verified in during this procedure by live insertion and extraction of the optical fibre.

## VII. Conclusion and Outlook

The preproduction for the TT Digitizer Boards has been performed. Lessons learned and errors found have been included in the preproduction of the IT Digitizer Board to enhance the performance of the design. Tests on a system scale demonstrate the performance and compatibility to the detector and common LHCb hardware. A final irradiation test has confirmed the required radiation tolerance for the doses expected in the experiment.

The final production of the full quantity of boards (322 for the TT, 387 for the IT) is planned for the end of 2005 with turn-around times expected to be 8-10 weeks.

## VIII. References


[1] LHCb Technical Proposal, CERN-LHCC-98-004.

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[8] D. Breton et al., SPECS, The serial protocol for the experiment control system of LHCb, LHCb note 2003-004.