THE UA1 TRIGGER PROCESSOR

Birmingham, Queen Mary College, Rutherford Collaboration

Presented by G.H. Grayer, Rutherford

ABSTRACT

Experiment UA1 is a large multi-purpose spectrometer at the CERN proton-antiproton collider, scheduled for late 1981. The principal trigger is formed on the basis of the energy deposition in calorimeters. A trigger decision taken in under 2.4 microseconds can avoid dead time losses due to the bunched nature of the beam. To achieve this we have built fast 8-bit charge to digital converters followed by two identical digital processors tailored to the experiment. The outputs of groups of the 2440 photomultipliers in the calorimeters are summed to form a total of 288 input channels to the ADCs. A look-up table in RAM is used to convert the digitised photomultiplier signals to energy in one processor, and to transverse energy in the other. Each processor forms four sums from a chosen combination of input channels, and also counts the number of clusters with electromagnetic or hadronic energy above pre-determined levels. Up to twelve combinations of these conditions, together with external information, may be combined in coincidence or in veto to form the final trigger. Provision has been made for testing using simulated data in an off-line mode, and sampling real data when on-line.

The "fast trigger" processor for the UA1 experiment is a purpose built device built at the Rutherford and Appleton Laboratory (RAL) by the Electronics Group in collaboration with physicists from the University of Birmingham, Queen Mary College London, and RAL. It is highly specific to our particular experiment in its arithmetic, number of channels, organisation and construction. However, the general design is applicable to similar calorimeter triggers.

Because the device is so specific, it is necessary to briefly describe experiment UA1, which will run on the SPS proton-antiproton collider. This is scheduled to become operational during the second half of 1981. The apparatus (Fig. 1) consists of (i) a three dimensional drift chamber in a magnetic field, surrounded by (ii) electromagnetic calorimeters formed of lead scintillator sheets which contain the energy from electrons, gamma rays and neutral pions, in turn surrounded by (iii) hadronic calorimeters which in general contain the remaining energy for hadrons such as charged pions, kaons, nucleons, etc , of which a part is normally deposited in the electromagnetic calorimeters . Finally, (iv) drift tube chambers surrounding the whole assembly track the escaping muons. Further calorimeters and chambers surround the beam pipe outside the magnet (not shown).

Only the calorimeters have rapid enough readout for a "fast" trigger, which aims to produce a decision between subsequent crossings of machine bunches (the $p\bar{p}$ collider, unlike the ISR, is a bunched machine). This time is 3.8 μs, and allowing for 1 μs needed to clear ADC's etc., leaves only about 2.8 μs to form a decision. Hence the need to use a somewhat inflexible parallel processing of channels, which requires the hardware to be matched to our experiment. Of course, a positive answer from the fast processor does not necessarily commit the event to be recorded. It could just provide a filter for more complicated and lengthy computations involving data from other elements in the detector,i.e. the drift chambers.

The basic functions of the processor are :

(i) Multiplicity requirements on clusters of calorimeter elements exceeding certain thresholds ;

(ii) Thresholds on energy sums made over selected parts of the calorimeter ;

(iii) Combining requirements (i) and (ii) logically to form the final trigger or parallel triggers.

The programmable flexibility of the processor is confined to : (i) applying an arbitrary functional transformation to the incoming calorimeter pulse height information ; (ii) changing threshold levels on calorimeter elements and on the multiplicity of these elements ; (iii) selecting channels over which energy sums are made, and of the thresholds on these energy sums ; (iv) choosing combinations of these requirements to form triggers. Loading and control of the processor is via CAMAC interfaces from the experimental control computer or from a local CAVIAR for testing purposes.

The following describes in some detail how this is achieved. The photomultiplier signals from the calorimeters, 2440 in total, are reduced to a more manageable number by mixing the signals from regions of the apparatus subtending small solid angle. These logical units are known as trigger channels, of which there are 288, half from the electromagnetic calorimeters and half from the hadronic calorimeters. These combined signals are digitised into 8 bits in about 500 nsec by a fast charge-to-time hybrid (LeCroy QT100R, specially developed for this project) followed by a 500 MHz scaler. Pedestal correction is preset. The output of the ADC's are connected via 72 ribbon cables to the digital processors and a test box which will be described below.

The first level of the processor consists of identical "standard cards", each dealing with 8 electromagnetic calorimeter channels and 8 hadronic calorimeter channels, associated geometrically in the apparatus. A functional block diagram (Fig. 2) shows the signals entering at the top, when the following operations are formed :

(i) Each channel has 256 x 8 bit words of static RAM, thus providing a look-up table. This has three purposes : (a) to convert incoming digitised pulse height to common "energy" or "transverse energy" units so that they may be combined within the processor ; (b) to apply minor pedestal corrections if necessary; (c) there is the possibility of applying non-linear corrections to the signals should this be necessary; in fact our mixer/ADC system is linear well within the precision required by the trigger. Thus the algorithm used to calculate this table is N.(INPUT ± ΔP), where N is a normalisation constant (which may include a geometrical factor appropriate to that particular channel if transverse energy is required), and ΔP is a small pedestal correction.

(ii) Adjacent electromagnetic channels are added together, since there is a high probability that the energy from one shower overlaps two channels. This is continued (where appropriate) from board to board. Each sum is applied to two comparators. The outputs of these are led off to a "second level" multiplicity card, which counts the number of comparators which have set in each of the two groups. An example of the use of this is that one group of comparators would be set with a high threshold, and the multiplicity to ≥ 1, to trigger on a high energy electron from vector boson decay ($W \rightarrow e\nu$). The other group of comparators could be set to a lower threshold, and trigger on multiplicity ≥ 2 to search for decays such as $Z \rightarrow e^+e^-$.

(iii) The sum is formed of four electromagnetic channels and four hadronic channels by adding in pairs in a tree structure. This combination is determined by our geometry, and represents the minimum block of hadron calorimetry (remembering that hadronic showers in general commence in the electromagnetic calorimeters). Again, there is a

high probability that hadronic showers overlap two blocks, so adjacent blocks are added to form a physically meaningful shower energy sum. Again, the sums continue from card to card where appropriate according to detector geometry. Also in a similar way to the electromagnetic channels, two comparators are connected to each summed channel, the outputs being taken to the second level multiplicity summing card. Each group may be used in a similar way, i.e. one set with high thresholds for detecting single high energy hadron showers (jets), the other set having a lower threshold and a multiplicity threshold of 2 or more for jet pairs.

In addition to this multiplicity logic, the total energy of one of these two adjacent block sums (to prevent double counting) is taken out to the second level for energy summing.

The "second level" cards of the processor are those which act on the outputs of the standard cards. The multiplicity boards have already been partly described ; they have four independent circuits which count set comparators within a group followed by a comparator to select a threshold multiplicity. These four circuits correspond to the one and two electromagnetic showers and one and two hadronic jet triggers previously given as examples. Where physically appropriate, adjacent elements may be declustered, i.e. the multiplicity of clusters of adjacent elements rather than individual elements evaluated.

The other second level cards are gated adders ; they also contain four identical independent circuits, each forming an energy sum from any selection of standard cards, followed by a comparator on this sum. Examples of the use of these are :

(i) A trigger on high total transverse energy summed over the whole apparatus could form a relatively unbiased jet trigger.

(ii) A total energy sum over the whole apparatus exceeding a certain threshold could be used to veto double interactions, an important consideration as beam intensities increase.

(iii) By evaluating the energy sums on two halves of the apparatus, an energy imbalance trigger may be formed to trigger on neutrinos which carry off substantial energy (e.g. in W decays).

The second level logic thus passes on 8 logical trigger bits, indicating whether the four multiplicity thresholds or four energy sum thresholds have been exceeded. In fact, we have built two processors as described, one which will be programmed to calculate in total energy, the other weighted to calculate in transverse energy. Thus a total of 16 trigger bits are passed on to the "third level" logic board. This card is capable of combining these trigger bits logically, together with up to four external logic signals (one of which could, for example, be an indication of tracks in the muon chambers). Up to 12 combinations of these trigger bits can be formed, in which any bit can be in coincidence, in veto, or ignored. These 12 triggers are OR'd, the final signal being taken to initiate data acquisition or a second stage trigger (for example, microprocessor track -finding in the muon chambers).

Such a complex system must have extensive testing and monitoring facilities to retain confidence. Firstly, all registers and RAMs have been provided with readback for checking. Secondly,certain intermediate results of the processor may be read back via the CAMAC interfaces. These facilities are useful for commissioning and testing the system, but are

too slow for monitoring purposes. "Test boxes" have therefore been constructed, containing a total of 640 8-bit read registers. These are connected to (i) the 288 8-bit digitised trigger channels entering the processor, and (ii) intermediate and final results such as energy sums on a standard card, comparator status, and trigger bit status. The status of the whole processor can be strobed into these registers, then read out as convenient without interruption of the trigger. A software simulation of the trigger can then be performed on the input data in the monitoring computer, and the results compared with those produced by the processor. This will be carried out during normal operation as a continuous monitor on a sample of events, both accepted and rejected by the trigger. For accepted events, the contents of the text boxes are written to tape with the rest of the event information as a record of the trigger.

A further facility provided by the test boxes is that the 288 trigger channels are also provided with write registers. By gating off the trigger ADC outputs, these registers may be used to play simulated data to the processor for testing, and the results read back via the read registers. Because the circuitry is directly coupled, if the inputs are held, so are the results after the propagation/settling time. This makes fault finding relatively easy.

The construction of the processor uses large wire wrap boards to achieve high density and a certain modification flexibility. In total there are 40 standard cards in the first level, six gated adder boards and six multiplicity boards in the second level, and one third level logic board. These are contained in six purpose-built crates each having a controller and integral power supply unit.

At the time of writing, the hardware is essentially complete and testing using the test boxes described above is in progress.

Further details of the REMUS controller incorporating a microprocessor chip to be used to read out the test boxes for data acquisition were given in paper No. 64 (poster session) at this conference.

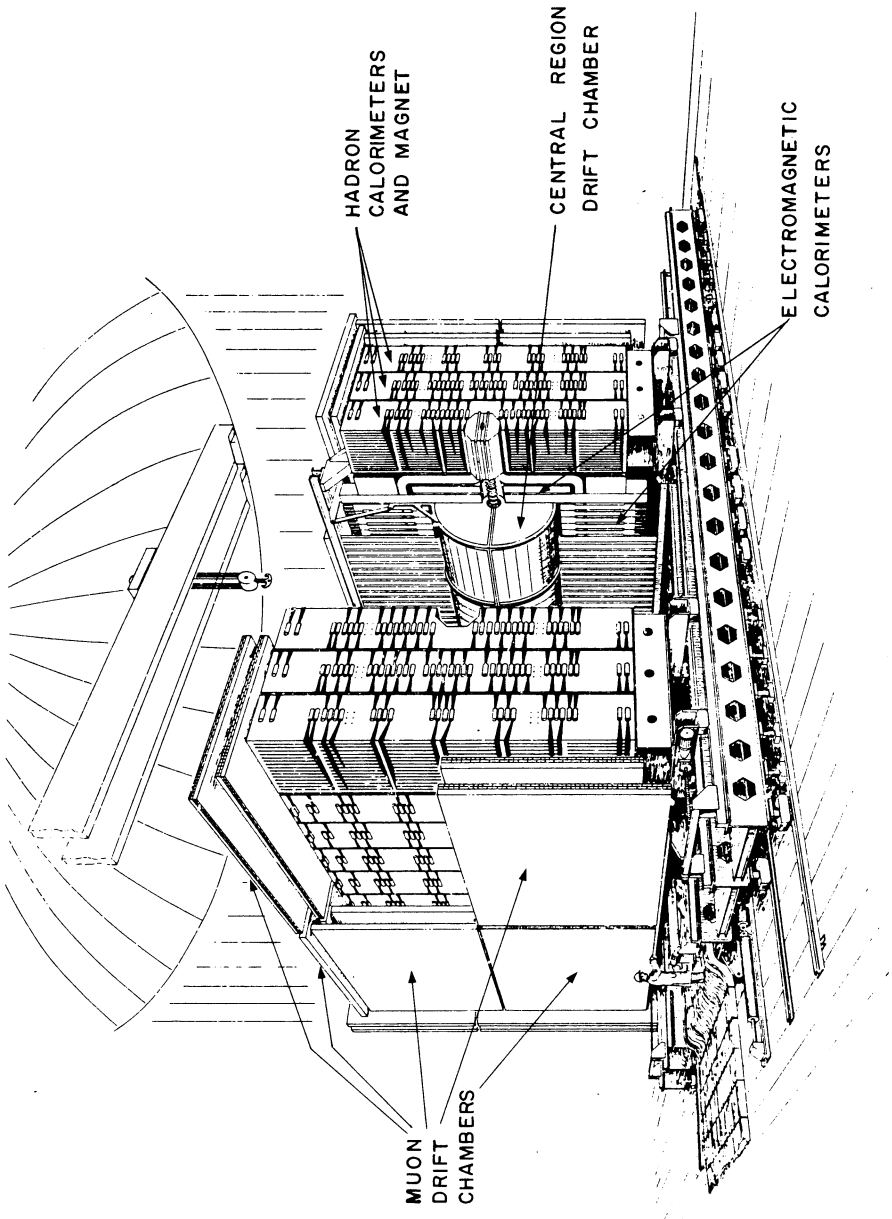

Fig. 1 Principal detectors in experiment UA1

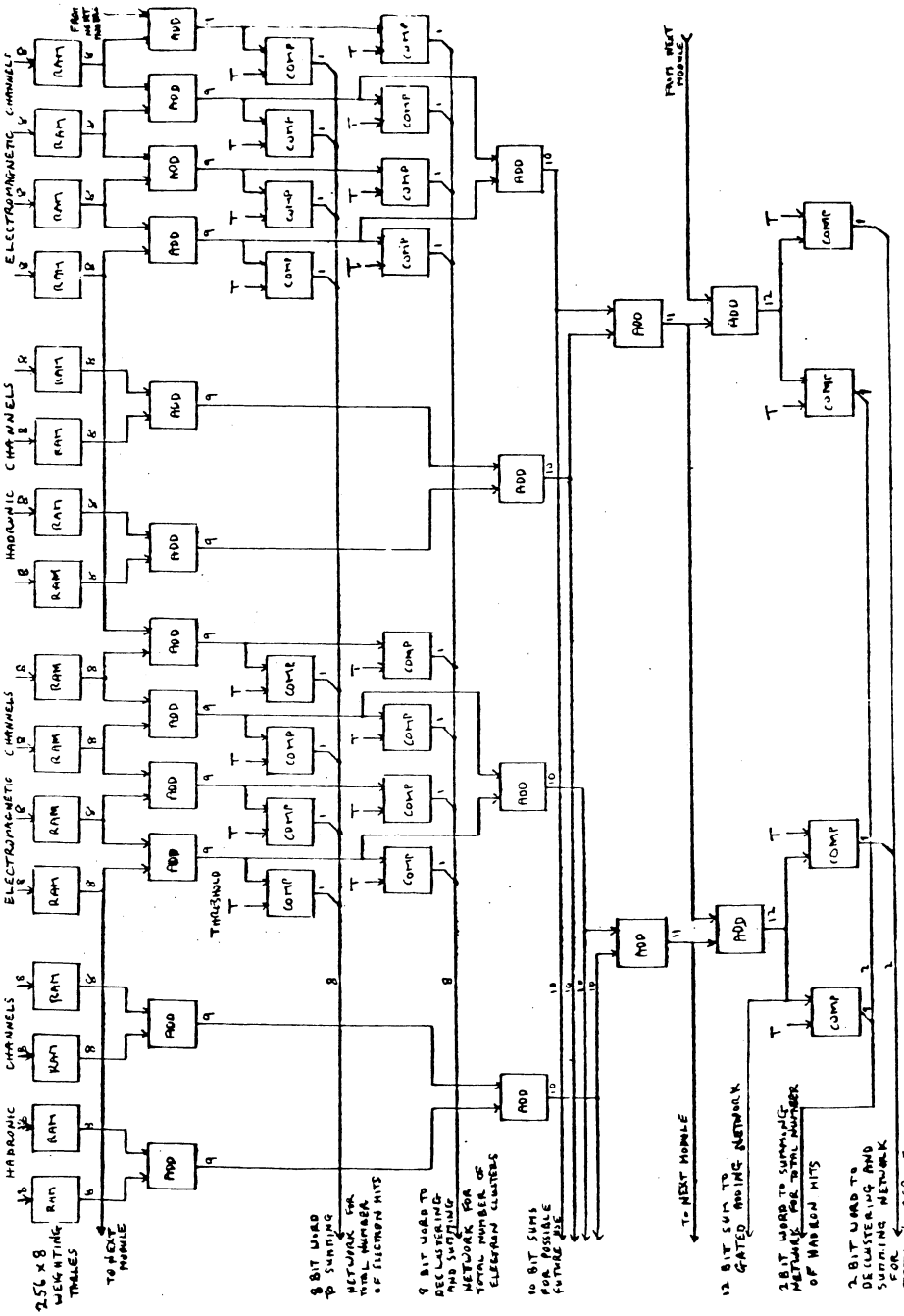

Fig. 2 Block schematic of a standard card