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SIGNAL ENCODING FOR PARTY-LINE DIGITAL DATA TRANSMISSION

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(submitted to Electron. Lett.)

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Geneva,
August 1975

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Indexing terms: Data transmission, Encoding, Party-line circuits

A digital encoding method is described which permits a single clock-generator to synchronize data transmission on a party-line bus shared by many transceivers. The requirements for either a separate bus for clock distribution, or individual clocks in each transceiver, are eliminated by the use of a signal set which allows the bus to carry data and synchronizing information generated simultaneously by separate sources.

Data-handling devices or control modules equipped with open-collector transistor bus-drivers and high input-impedance receivers[1] may be interconnected by a single unbalanced party-line (Fig. 1) with appropriate terminations and bias. This configuration is attractive in applications[2] where a large number of devices are concentrated within a relatively local area, and low cost is a more predominant consideration than the sacrifice of speed incurred by the use of passive line pull-ups and serial data transmission.

Whether word (or byte) transmission in such a system is synchronous or asynchronous, a periodic clock signal is required by any active transmitter to generate serial data at a defined bit rate, and by the receivers to decode the signals on the party-line. An individual clock-generator is normally provided for this purpose at each of the transceiver modules; or, if a single system clock-generator is employed, its output is distributed to all the transceivers by an additional bus separate from the data party-line[3]. In asynchronous reception with local clocks, synchronization is effected at the start bit which precedes each transmitted word, and the clocks are designed to have sufficient stability to remain adequately phased for the duration of the word. On the other hand, in a synchronous system (and in pseudo-asynchronous transmission in which the interval between words is variable but quantized to an integer multiple of the

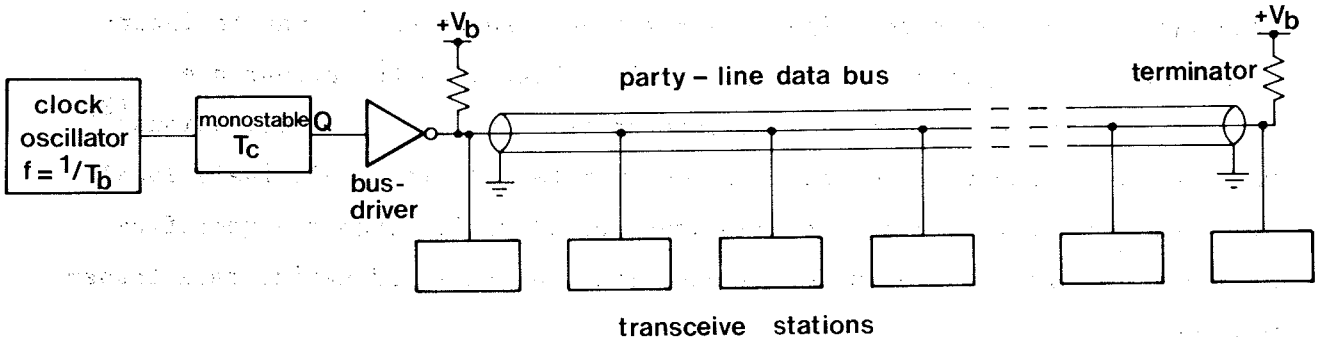

Fig. 1 Party-line serial data-link with single clock injector

T_b = data-cell duration T_c = clock pulse duration

system clock period), the serial data may be transmitted by a code having self-clocking properties. The schemes most generally used for this purpose, bi-phase level[4], bi-phase mark[5] or space, and Miller code[6,7], are illustrated in Fig. 2. The exclusive-OR of NRZ-L data and short-duration clock pulses also yields a signal sequence from which the clock can readily be reconstituted at the receiver[8].

In an important class of party-line systems, many transceivers are interconnected by a bus of limited total length, and high data-rate is less important than economy of circuitry in each module serviced. It is therefore possible to utilize a baud rate low enough for time-skew due to propagation delays, mismatch reflections and rise-time distortion[9] on the bus to be negligible. A valuable cost-saving can then be effected by the use of an encoding method such that not only can the receiving devices reconstitute the clock from the transmitted waveform, but also the active transmitter can utilize a system clock distributed to it by the same party-line as that on which it is sending.

Study of the examples of the signal waveforms generated by the standard self-clocking encoding schemes shown in Fig. 2 reveals that none of them have the required properties. The party-line signal is the inclusive-OR (convention logic 1 low on the bus, high otherwise) of the transmitter outputs which are applied to it, so that a signal waveform set is required for which there is a time interval at logic 1 in the same phase of each data-cell for either member. The signal during this time interval can then be generated by the system clock rather than by the active transmitter. It is also convenient for the implementation, although not essential, if both members of the set have a coincident logic 0 to 1 transition at the start of this time period.

A signal set satisfying these requirements, and also having power spectral properties compatible with baseband line transmission, is shown in Fig. 3, and an example of an encoded waveform is shown in Fig. 2, together with its clock and data transmitter components. The continuously running system clock (see Fig. 1) grounds the party-line by its bus-driver

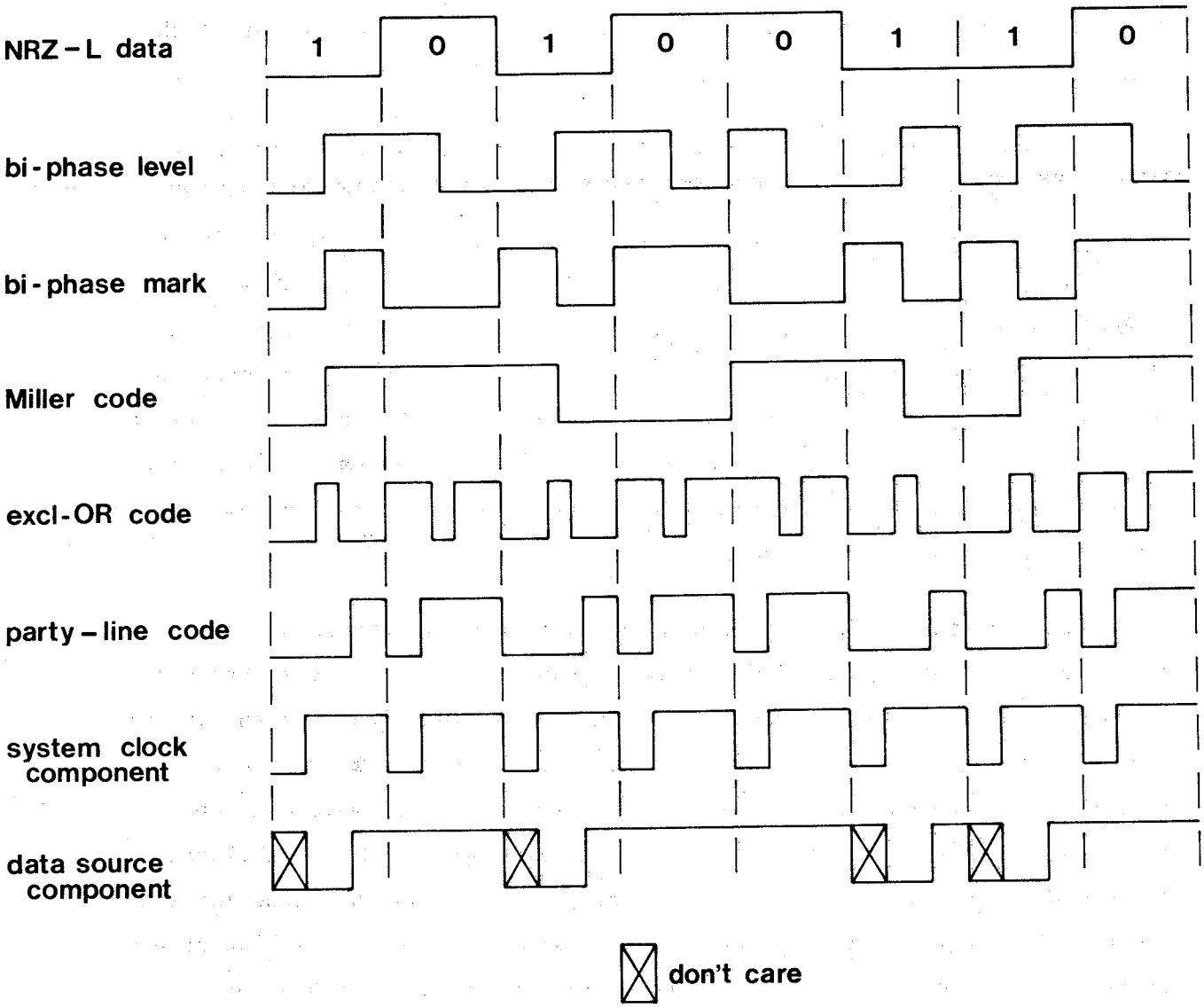

Fig. 2 Comparison of party-line digital encoding with standard self-clocking schemes

All signals shown logic 1 low as they would appear on a party-line

for a time interval T_c at the start of every data-cell of period T_b (T_c/T_b = 0.25 - 0.35). During a 0 data-cell the data transmitter remains off, while during a 1 data-cell it grounds the party-line from a time overlapping with the clock pulse until T_c before the end of the cell.

A party-line transceiver using the encoding method described is readily implemented as shown in Fig. 4. Triggered by the high to low transition which occurs on the bus at the start of each data-cell, a monostable of duration $T_b/2$ samples the bus state at the mid-point of each cell and sets the D-type bistable in the case of a data 1. A short duration (eg. $T_b/100$) monostable, also triggered at data-cell start, generates a clock pulse of which either edge may be used to enter the received serial data into a parallelizer. The same pulse strobes the output of a serializer during transmission. For a data 1, the monostable of duration (T_b-T_c) is triggered to cause the first waveform of Fig. 3 to be generated on the party-line, while for a data 0 the bus-driver remains off, so that the second waveform is generated on the bus by the system clock.

In the case of party-line devices utilizing MOS/LSI universal asynchronous receiver transmitters (UARTs), which are format-compatible with many computer data communications interfaces and microprocessor asynchronous communications interface adaptors (ACIAs), a clock may be required at a frequency multiple (typically 16) of the data rate. The encoding scheme presented here may be employed equally in this application, the single system clock being applied to the bus at the rate required by the UARTs, and each transmitted data-cell spanning 16 periods of the signal waveforms of Fig. 3. The implementation suggested in Fig. 4 also remains applicable. The UART transmitter section output is sampled 16 times per data-cell at the tx data input gate, while the rx data bistable output is applied directly to the UART receiver section input since it follows the changes in the data component of the party-line signal only.

The requirement for a relatively high clock frequency on the party-line in this case is compensated by the fact that unlimited time-skew may be permitted since actual phase-synchronization of the clock and the

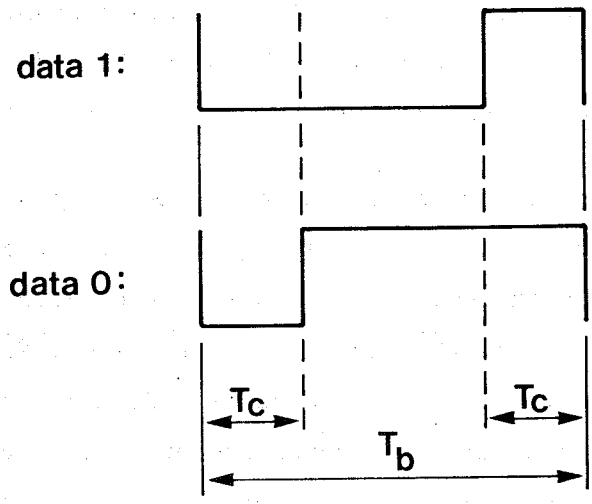

Fig. 3 Signal set for single-clock party-line communications

T_b = data-cell duration T_c = clock pulse duration

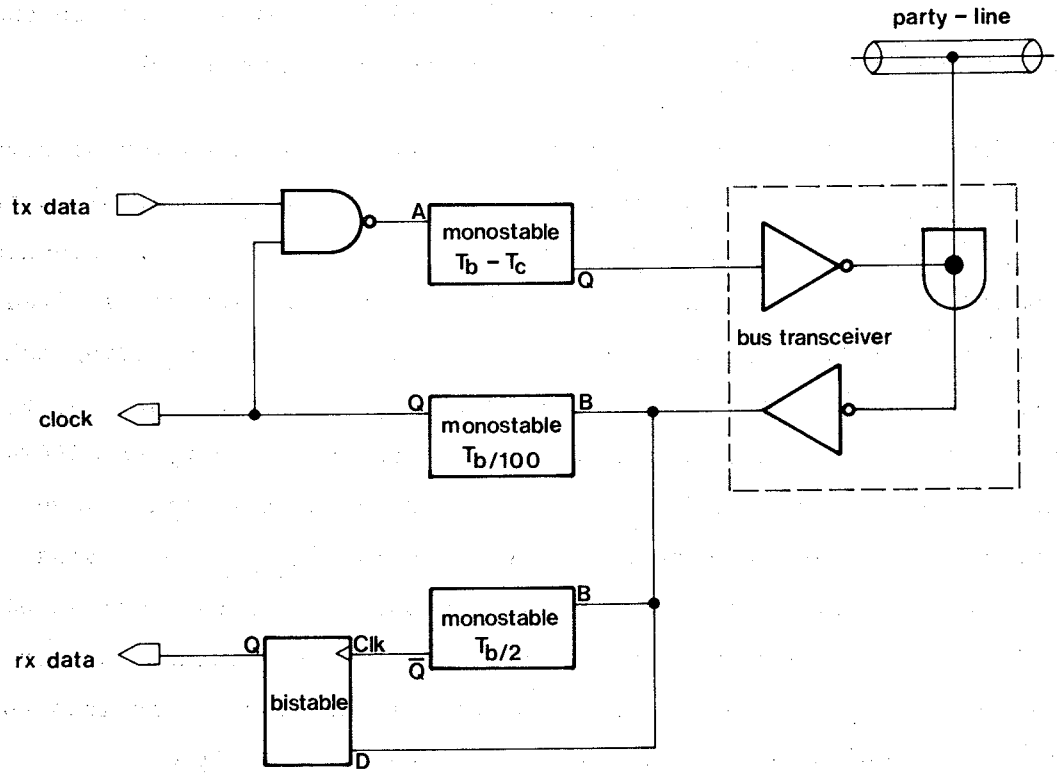

Fig. 4 Principle of party-line transceive station

Monostables are negative-edge triggered at A inputs, positive-edge triggered at B inputs. Bistable is D-type

data sequence is no longer required. The signal attenuation characteristics[10] of a typical short data bus are also adequate for the maximum 200 kHz clock rate required for data transmission at up to 12.5 kbit/s. This rate exceeds the requirements of most asynchronous data communications devices and typically approaches the operating limit of the UART itself.

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14th August 1975

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