A radiation tolerant fiber-optic readout system for the LHCb Silicon Tracker

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Abstract

A fiber-optic readout system has been designed for the LHCb Silicon Tracker to transmit the detector data to the counting room at a distance of 120 m from the detectors. In total, data from over 272000 detector channels have to be transmitted at an average trigger frequency of 1.1 MHz. In the design of the system, special attention was given to its radiation tolerance, as the transmitting section is located close to the beamline and therefore is exposed to moderate particle fluences and ionizing dose during the expected operational life of 10 years. We give a general overview of the readout link scheme and present performance data on its reliability and radiation tolerance obtained from first preseries elements of the system.

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1. Introduction

The LHCb experiment [1], which is one of the four large experiments at the new Large Hadron Collider (LHC) at CERN, is going to study decays of B-mesons and precisely determine CP-violating parameters in the b-quark sector. The LHCb Tracking System is described in [2]. The Silicon Tracker consists of two sub-systems: a Trigger Tracker, which is located upstream the spectrometer dipole magnet, and the Inner Tracker downstream of the magnet. Both sub-systems transmit their detector data via a digital fiber-optic readout system to the counting house, approximately 120 m away from the detector.

2. Overall readout system layout

The Silicon Tracker is based on silicon microstrip sensors as detection devices. A Trigger Tracker sensor has 512 strips with a pitch of 183 µm while an Inner Tracker sensor features 384 strips with a pitch of 198 µm. Depending on the area, which has to be covered by a single readout module, up to four sensors are connected in series. At the end of each readout module, a hybrid carrying the Beetle readout amplifiers [3] is connected to the sensor strips via a pitch adapter. As the Beetle chip has 128 inputs, three chips handle the signals from an IT readout module, while four chips are needed for a TT readout module.

Each Beetle readout amplifier integrates charge signals from its 128 inputs and stores it into an internal analogue derandomizer pipeline. Upon receiving a Level-0 trigger signal, which occurs at an average rate of 1.1 MHz, the analogue data of the corresponding event are multiplexed into four analogue differential output drivers. To maintain the Signal-to-Noise ratio of these signals, it was chosen to digitize them close to the detector and transmit digital data over optical fibre. Figure 1 shows an overview of the system.

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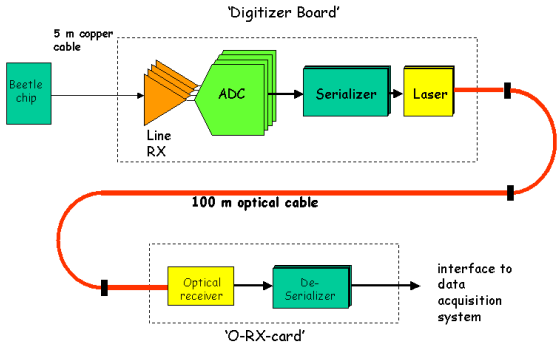

Fig. 1. General overview of the digital optical readout sytem

Analogue signals from each readout hybrid are connected via a twisted pair copper cable of about 5 m in length to a Digitizer Board, which prepares the data for digital optical transmission. The Digitizer Boards are housed in Service Boxes, which are located close to the detectors but outside of the acceptance of the LHCb experiment. This approach minimizes the amount of dead material inside the acceptance of the experiment and at the same time relaxes the requirement for radiation tolerance of readout components due to the increased distance to the beampipe.

On each Digitizer Board, data from one readout hybrid are received by differential line receivers that match their signal levels to the input range of the following single-channel analogue-to-digital converters (ADC). As each Beetle has four analogue outputs, a Digitizer Board for a Trigger Tracker readout hybrid digitizes 16 channels, while an Inner Tracker Digitizer Board carries 12 ADCs. The ADCs are running continuously at 40 MHz and are phase-locked to the sampling clock of the readout amplifiers. 32 bit wide data from four converters associated to a single Beetle readout chip are connected to a CERN Gigabit Optical Link chip (GOL), which has been designed in a dedicated radiation hard layout process and produced in 0.25 µm CMOS technology [4]. The GOL chip multiplexes the data into a single Gigabit Ethernet signal of 1.6 Gbit/s data-rate. Integrated into the GOL is a laser driver that controls a VCSEL diode, which couples the optical signal into a single fiber cable. The data are then transmitted to the counting house using a multimode multi-ribbon fiber cable. There, the cable is connected to a 12-channel integrated optical receiver module, located on an optical receiver card (O-RX card). Two receiver cards form the input stage to the Trigger ELectronic and Level-1 (TELL1) board [5], which serves as an interface to the LHCb data acquisition system.

3. Digitizer Board performance

Each Digitizer Board digitizes data on several channels in parallel and care has to be taken when distributing the sampling clock to the ADC devices on the board to ensure simultaneous sampling on all channels. For a given Digitizer Board, all input channels belong to a single readout hybrid, on which the readout chips are located close to each other. All signals from the hybrid are routed through the same cable, which apart from the inevitable cable-inherent channel-to-channel skew provides equal propagation delays for all signals. All signals therefore arrive at the input of the Digitizer Board at the same time. To equalize propagation delays on the Digitizer Board itself in addition to the necessary impedance controlled layout, the routing of the signal lines has been done such that equal trace lengths are maintained as much as possible. Equal propagation delays for the sampling clock were realized by using a clock distribution tree. The channel-to-channel variation of the sampling times of a single Digitizer Board was tested by injecting a digital signal simultaneously into all Digitizer Board inputs. By varying the phase of the sampling clock with respect to the input signal, the phase of the leading edge of the digital signal could be determined with sub-ns precision. The measured peak-to-peak variation of the leading edge phase was determined to be less than 2 nsec (see Fig. 2). This is in good agreement with the specified channel-to-channel variations of the devices used for the clock distribution network. This variation is considered to be negligible for the operation in the experiment.

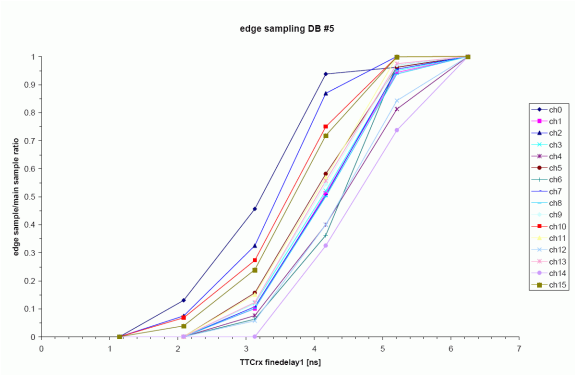

Fig. 2. Leading edge of a digital test signal, simultaneously sampled by 16 channels

Each Beetle readout chip provides a digital signal synchronous to the analogue output to mark the presence of data. This is used to enable an automatic resynchronization of the optical link between readout frames. By doing so any single event triggered loss of link synchronization is resrticted to the loss of a single readout frame, which greatly enhances the robustness of the transmission system.

The complete Digitizer Board is supplied with only two voltages (+5 V, +2.5 V). With a total power dissipation of less than 5 W for a board area of 14 x 33 cm^2, convective cooling is considered to be sufficient.

4. Optical Link performance

Several methods exist to characterize the performance of an optical transmission link. One of them is the determination of the Bit Error Ratio (BER) which gives the ratio of wrongly received bits to the total number of bits transmitted. In general a BER of 10^{-12} or better is considered to be adequate in commercial applications. A test was performed using a setup comparable to the planned LHCb installation (100 m fiber, 3 fiber interfaces) and no errors were detected over a period of over 4 hours resulting in a BER rate of less than 10^{-13}. This test was performed with random digitized data from a readout hybrid without a sensor attached. Another bit error rate measurement is under preparation in cooperation with the LHCb Outer Tracker group at University Heidelberg. In this test, pseudo-random bit streams and an optical attenuator will be used. This will permit a precise determination of the optical power budget. Calculating the theoretical optical power margin from the available datasheet specifications of the VCSEL diode and the receiver, a typical power margin of 14 dB is expected by summing up average performance data for all devices in the transmission system. When summing up guaranteed parameters instead, a worst case margin of 5dB is calculated.

Another method for the characterization of an optical link transmission system is the determination of the eye diagram. For this, the Gigabit data signal is probed using a fast oscilloscope set to infinite persistence while the transmission clock is triggered continuously. The superimposed signal transitions form a pattern commonly referred to as ‘eye’. A wide open eye with clear separation of the ‘0’ and ‘1’ states and without any transitions inside a bit interval is characteristic for a robust transmission. In recent years, advances in analysis packages for fast oscilloscopes have made a quantitative measurement possible. The phase variation for each data signal transition can be accurately measured and compared to the ideal transition time, resulting in a measurement of the time jitter. When recording data over an extended period of time, the absolute range of the observed time jitter can be compared to the jitter allowed by the receiver for proper discrimination of the data. This is visualized by the so called ‘bathtub-curve’. Here, the ratio of wrongly discriminated bits to total transmitted bits is plotted versus the position inside a bit interval. Obviously, this ratio is close to 0.5 for sampling positions close to the beginning or the end of a bit interval as the data transition take place here. The ratio is of the order of 10^{-12} and better in the middle of a bit interval, as the eye opening and hence the bit separation is best. The BER can now be estimated by comparing the width of the bathtub curve with the specified minimum eye opening required by the receiver for a correct determination of the bit interval and subsequent data discrimination. Figures 3 and 4 show the bathtub curve and the corresponding eye diagram for a fiber length of 100 m[6] . The eye diagram shows a clean opening of the eye and the bathtub curve gives an estimate of the bit error rate of 10^{-16} for an eye opening of 0.6 bit intervals (UI).

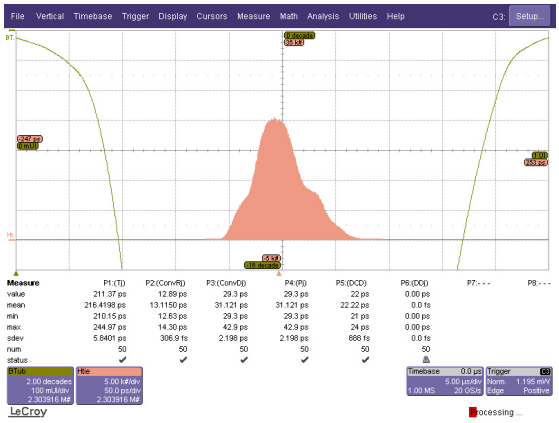

Fig. 3. Bathtub curve for the optical link with 100 m fiber.

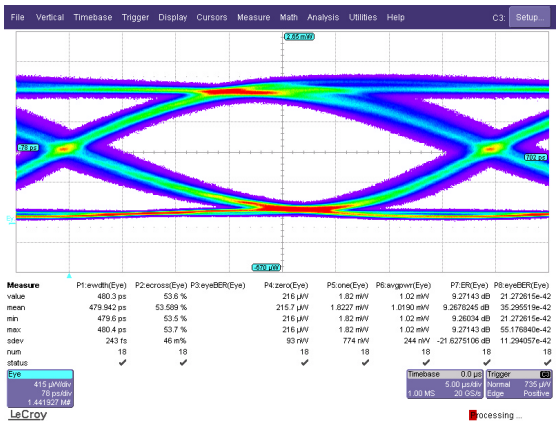

Fig. 4. Eye diagram for the optical link with 100 m fiber.

5. Service Box

17 Digitizer Boards for the TT station, each carrying 16 ADCs, have been produced in a preseries production run. Apart from minor layout errors, all

6 measurements provided by Paolo Frascati, LHCb Muon group, Frascati

boards work within specifications. Another 10 Digitizer Boards for the IT version, carrying 12 ADCs each and including all know error fixes and some minor improvements are currently being produced. The Digitizer Boards have been mounted in a prototype Service Box including a custom made backplane for power and timing signal distribution.

For each Service Box, a dedicated Control Card centrally sources the timing signals. For this purpose, each Control Card carries a TTCrq mezzanine to receive the clock and trigger information from the LHCb TFC network [6]. In addition two SPECS slave mezzanines [7], which are also located on the Control Card, interface the detector frontend electronics to the LHCb Experiment Control System ECS [8].

The distribution of timing and slow control signals from the Control Card to the connected Digitizer Boards is done via a custom-made backplane. All signal traces for fast timing signals are routed such that an even propagation delay for all Digitizer Boards in one Service Box is maintained. The backplane also carries the radiation hard voltage regulators [9], which supply the Digitizer Boards and the readout hybrids connected to them with power. A common water-cooled heatsink is used to extract the power dissipated by the linear regulators.

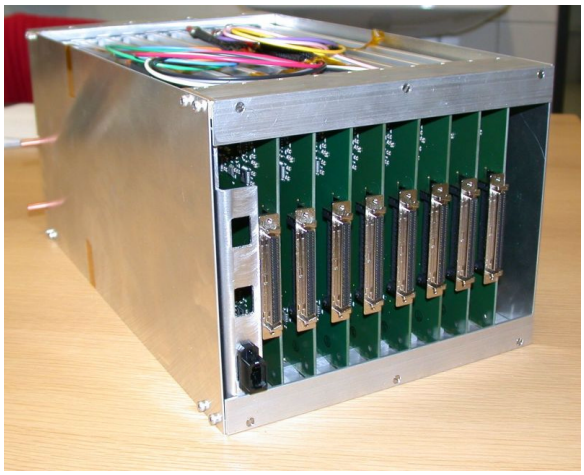

Fig. 5. Half-scale prototype of Service Box.

Integration tests to the LHCb DAQ hardware (TELL1 board [6], Readout Supervisor [7]) have started and have confirmed the compatibility of all hardware components. A full readout chain has been assembled, using identical hardware as foreseen for the detector installation. It includes all readout elements starting from the readout hybrid and leading up to the Gigabit Ethernet interface of the TELL1 board to the CPU farm and therefore represents a complete connectivity test.

6. Outlook

A total of 280 Digitizer Boards are needed for the Trigger Tracker subdetector, and 336 Digitizer Boards are needed for the Inner Tracker. The full production of these boards is scheduled to start in late Summer 2005. 48 Service Boxes with the associated number of backplane boards are also planned for production later this year. Since the boards contain no elements that would need tuning, board commissioning is expected to proceed quickly and be completed well in time for the detector installation and commissioning that will begin in May 2006.

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