LOW NOISE ELECTRONICS FOR EXPERIMENTS AT LHC. DESIGN SUGGESTIONS.

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1. INTRODUCTION

The need of reducing the collection times of solid state detectors will lead to thin layers, 150 to 200 μm thickness. Consequently, the charge made available by minimum ionizing particles will be rather small, between $1.2 \cdot 10^4$ and $1.6 \cdot 10^4$ electrons for unity multiplicity. Front-end electronics with adequately low noise must be designed to detect such small amounts of charge and the problem looks to be harder if the short times available to process the signals are accounted for.

2. ELECTRONIC LIMITATIONS AND DESIGN SUGGESTIONS

The charge detectability limits at very short processing times will be discussed here with reference to two solutions that meet respectively the case of a detector capacitance C_D of a very few pF and that of a detector capacitance C_D in the 10-to-100 pF range of even larger.

With reference to solid state detectors, the former case approaches the application condition of microstrip chambers, while the latter can be applied to more general solid state structures. Capacitances beyond 1 nF might be presented by the sampling cell of a silicon calorimeter.

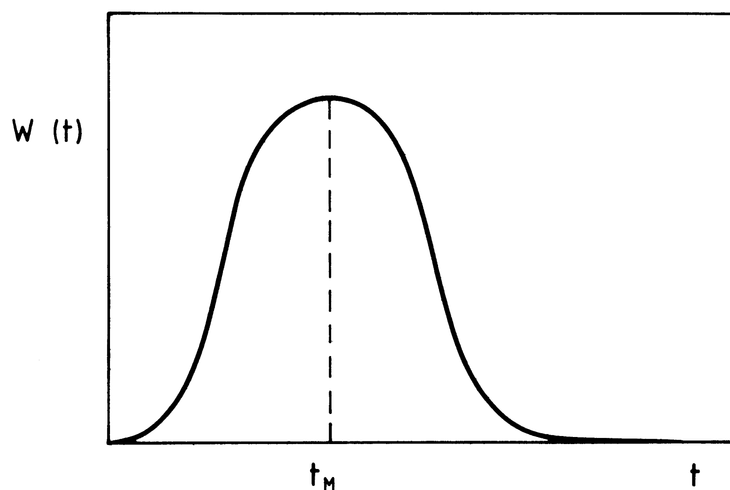


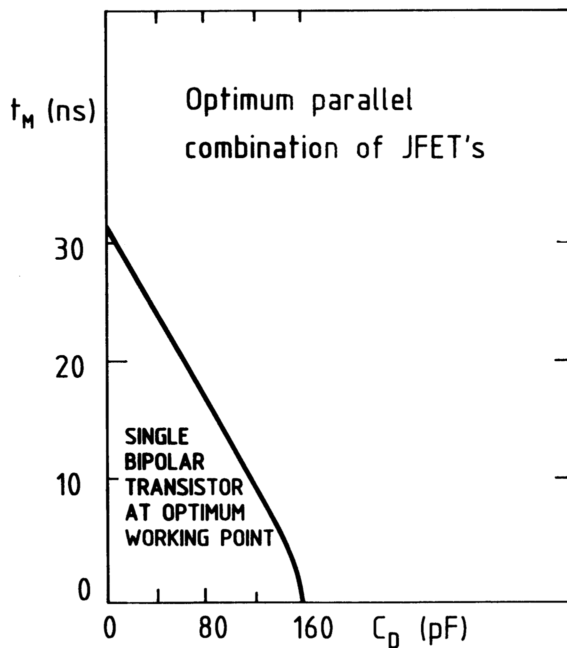
Fig. 1 - Reference δ-response of the analog processor.

The discussion here, moreover, aims at being not restricted to solid state detectors alone, for it covers the general problem of a radiation detector which can be described as a capacitive source and which has no built-in charge multiplication and for which the main source of degradation in the charge measurement is represented by the external electronics.

The equations that are written below refer to a shaping network following the preamplifier, with a δ-impulse response of the type shown in Figure 1, that is, a piecewise quadratic time dependence.

It has been shown that a bipolar transistor with a cutoff frequency of some GHz is the most suitable device at small C_D and short t_M. This statement is made evident by Figure 2, which shows in the $(C_D, t_M$ plane the boundary curves between the regions where a single bipolar transistor is less or more noisy than the optimum combination of field-effect devices. The equivalent noise charge is given by :

$$\overline{ENC}^2 = 2kT[(R_{BB'}C_D^2 + \frac{(C_D+C_B)^2}{2g_m}) \frac{\alpha_{F1}}{t_M} + \frac{g_m}{2\beta} \alpha F2 t_M]$$



where k is Boltzmann's constant
T is the absolute temperature
g_m the transconductance
C_B the diffusion capacitance :
$g_m/C_B=\omega_T$
$R_{BB'}$ the base spreading resistance
β the base-to-collector current gain
α_{F1} and α_{F2} two parameters depending on the shaper employed.

Fig. 2- Boundary curve separating the regions where the bipolar transistor has better or worse noise behaviour than the optimum parallel combination of JFETS.

For the shaper assumed here as a reference, which is of the type described by Figure 1, the values of α_{F1} and α_{F2} are respectively 8/3 and 14/15.

As an example, a transistor working at a collector current of 1mA, with β=100, f_T=1GHz, $R_{BB'}$=10Ω would give at C_D=5pF, values of the equivalent noise charge of

800 rms electrons at t_M=5ns
870 rms electrons at t_M=10ns

These values would be adequate, as far as the signal-to-noise ratio goes, even in the case of a single M.I.P. in a 150 μm thick Si detector.

b) Larger values of C_D

Field-effect devices of large gain-bandwidth product, capacitively matched to the detector are perhaps the best solution. The equivalent noise charge is in this case:

$$ENC^2 = 8KT \cdot \frac{0.7}{\omega_T t_M} \cdot C_D \alpha_{F1}$$

A device with a gain-bandwidth product f_T of 5GHz would yield, for C_D=100pF, an ENC of 1250 rms electrons at t_M=5ns and 900 rms electrons at t_M=10ns. GaAs field-effect transistors suit the actual case well.

Additional line broadening due 1/f - type noise sources has to be expected, but the basic feasibility conclusions about low noise electronics do not change in a substantial way.

The future technological advance of IGFETs of large bandwidth intended for applications in the field of communications might provide interesting alternatives. It has to be pointed out that the analysis carried out so far has the purpose of clarifying in both cases, namely very small C_D's and average-to-large C_D's, the optimum achievable theoretical values and the best solutions conceivable nowadays.

Several problems remain still open. Among them, the feasibility on a large monolithic scale of the solutions proposed above. High density bipolar circuits with adequate noise performances may be feasible in monolithic technology even now. Something is moving in the direction of integration of GaAs devices. Remembering that the realization phase of the instrumentation considered here will start in a few years' time, some of the present technological limitations can be assumed of minor importance in the design.

3. DETECTOR LIMITATIONS

In the actual applications of silicon detectors, values of t_M below 10 ns can be hardly employed. This lower limitation of t_M is set by the detector collection time.

As pointed out in Ref. 2, the slower tail of the detector current pulse is determined by the holes drift. To achieve complete charge collection, about 10 ns are required in a 150 μm thick detector. It is true that a reduction in the collection time can be achieved by increasing the voltage applied to the detector beyond the value at which total depletion occurs, as long as the holes' drift velocity does not reach saturation. However, a 5ns collection time can be assumed as a lower limit which can be hardly reduced in a detector, though it is as thin as 150 μm.

To preserve the value of the collected charge, the peaking time t_M of the shaper must be adequately longer than the collection time of the detector.

The signal at the shaper output, which is the convolution of the detector current pulse and of the shaper function W(t) may have a basewidth of some tens of nanoseconds, thus exceeding the time interval between bunch crossings. If 200 μm detectors are used, the collection time would be longer and the problems releated to the width of the pulses at the shaper output become more serious.

4. PILE-UP LIMITATIONS

It seems reasonable to assume that the time separation between two bunch crossings is longer than the collection time of the detector and that not more than one event occurs at every bunch crossing. The need of taking the best advantage of the accelerator luminosity might, however be in conflict with the time requirements for the detector electronics arising from charge detectability considerations. In other words, the shaped pulses at the output of the analog processors may have a basewidth exceeding the distance between bunch crossings. As a consequence, two events belonging to two subsequent bunch crossings may occur within the basewidth of the shaped pulses. This would give rise to a pulse-on-pulse pile-up in a non-segmented detector. In a highly segmented detector, although the probability that the same segment be hit in two subsequent bunch crossings might be very small, two events occurring at a time distance shorter than the pulses basewidth lead to attribution ambiguities even if they involve different detector segments.

A system which allows operation at pulse basewidths longer than the interval between bunch crossings, yet preserving the events identity is shown in Figure 3. The system of Figure 3a) employs a wideband preamaplifier-amplifier combination, so that the signal $V_1(t)$ is close in shape to the detector current pulses.

Shaping is implemented by units, three in the example, that are switched sequentially on the amplifier output. The configuration of Figure 3a) avoids either pile-up in a non-segmented detector or ambiguities in a segmented detector at basewidths of the shaped pulses shorter than the interval between bunch crossing multiplied by the number of splitting channels. So, as shown in Figure 3b) three lines are necessary to cope with the case of longer shaping (dotted signals). For the shorter pulses (continuous line) two shapers would suffice. The system of Figure 3a) can be thought of as a gated shaper to which a demultiplexing feature has been added.

It goes without saying that in a highly segmented detector, splitting channels may be very heavy in terms of cost and complexity. However, it is a proposed solution for detectors whose use could otherwise be impaired by the time constraints set by the accelerator.

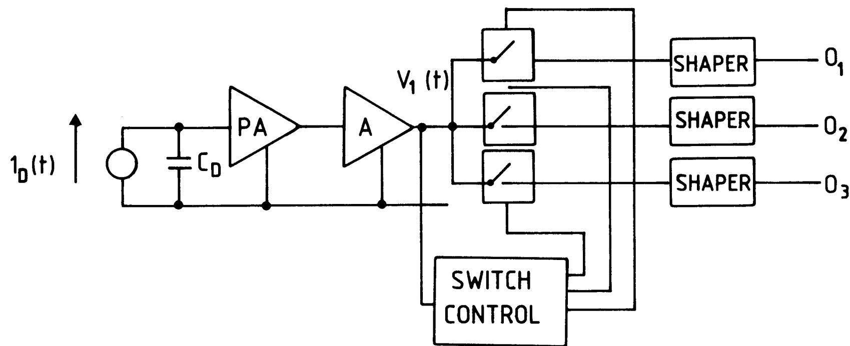


Fig. 3a : system allowing pulse duration longer than the interval between bunch crossing.

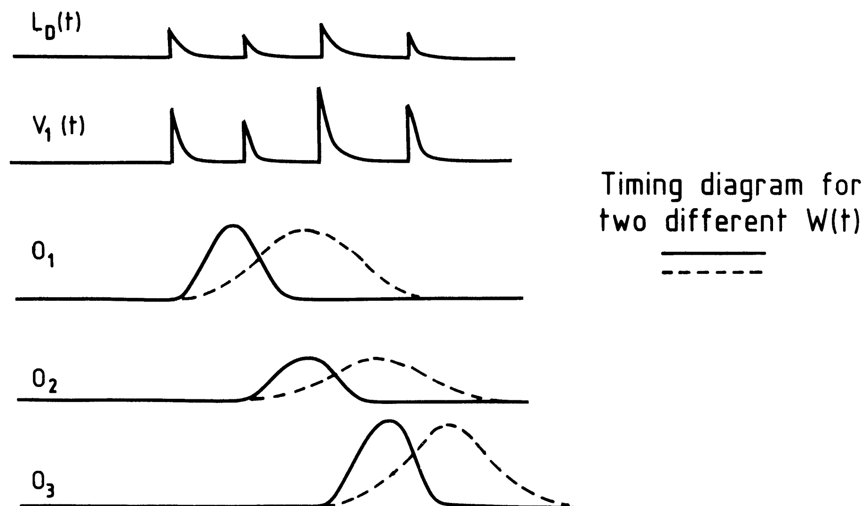


Fig. 3b) Timing diagram for two different W(t).

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