DATEP : 120 CHANNEL PM HV REGULATOR*

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ABSTRACT

DATEP (Distributore Alta Tensione Programmabile) has been designed to distribute high voltage to some 1500 PM's for the gamma detectors (part C) of EHS. Each unit has its own microprocessor controller which performs continuous checking of the 120 channels and allows operator interaction.

Channel regulators are based on a specially developed thick film hybrid circuit that allows to get on overall temperature coefficient better than 50 ppm/^{0}C.

1. INTRODUCTION

DATEP (Distributore Alta Tensione Programmabile) has been designed to distribute high voltage to some 1500 PMs for the gamma detectors (part C) of EHS. Each DATEP unit supplies up to 120 HV channels whose voltage can range from about -200 V to -2048 V in steps of 2V. The maximum difference allowed between channels is 512 V. DATEPs need an external HV power supply, as they only provide active regulation. Each unit has its own microprocessor controller, which performs continuous checking of the 120 channels and allows operator interaction through a standard RS 232C terminal or control through a special CAMAC unit. This latter unit can control up to 16 DATEPs (1920 channels).

2. SYSTEM DESCRIPTION

Each DATEP unit consists of a special 6 U crate which contains three types of module :

a) HV regulation module (up to 15) ;

b) interface card ;

c) microprocessor card.

The mechanical standard is the well-known Eurocard (double). All the cards are connected through a back plane with bus lines.

Each HV regulation module has eight channels and the outputs from each set of three modules are grouped together in one connector (24 outputs). An overall representation of the system is given in Fig. 1. In the next sections the different modules will be described in detail.

3. HV REGULATION MODULE

The block diagram of the regulator module is given in Fig. 2.

The data lines (DD0-DD7) come directly from the microprocessor, through the bus, and the microprocessor can therefore write a byte into any channel buffer. Selection of the module and the channel is made by address lines AD0-AD6 ; the address lines go to the bus buffered by the interface. The module addresses are wired into the positions (slots) along the bus and are read using the SL lines.

The actual output of a channel is given by :

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$$V_n = V_{off} + V'_n ,$$

where the offset voltage V_{off}, is supplied to every module by the interface and can be varied in steps of 8 V from about -200 V to -2048 V, and V'_n is the analog value corresponding to the byte written by the microprocessor into the buffer of the n^{th} channel. V'_n can vary from 0 to -512 V in steps of 2 V.

The low-level regulator is made as a hybrid (thick film) in order to have compactness, good precision, and temperature coefficient on the critical resistors that define gain and stability (laser trimmed). The high-voltage divider is also a thick film laser-trimmed resistor.

The overall temperature coefficient is better than 50 ppm/^{0}C.

The measured Z_{out} impedance is about 50 Ω from d.c. to 100 Hz and becomes about 1 kΩ at 1 kHz. Ripple from the main power supply is attenuated 500 times at 100 Hz.

The actual outputs V_n (through the divider) are multiplexed onto the bus line ANOP. An ADC located on the interface card allows the microprocessor to monitor each of the output voltages in turn. Conversion is made by a 12-bit successive approximation ADC. A least count of 0.5 V is possible if the actual output is limited to -2048 V.

4. INTERFACE

The block diagram of the interface is given in Fig. 3.

The transceivers and control lines (top part of the drawing) provide the possibility of connecting in a daisy chain up to 16 DATEPs to one CAMAC station. The connection for the data lines is bidirectional, while the connection for the control lines is not. Upon recognition of the DATEP code, the interface, according to the data direction, provides the connection of the data lines to one of the parallel I/O ports of the microprocessor. The DATEP code or address is defined by its position in the chain : i.e. the n^{th} DATEP automatically responds to the code n. The interface, as already mentioned, provides buffering for the address lines of the DATEP dataway. In the microcomputer memory address map, all the addresses of the following type :

AD15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	0	0	X	X	X	X	X	X	X	X	X	X

are considered as address of the DATEP channels. When the interface recognizes a memory reference instruction with such a code, it provides buffering of the 7 least significant bits onto the DATEP dataway.

Address buffering is not necessary for data loading into the channel buffer, but it is necessary for keeping the channel selected while performing AD conversion of the ANOP line to read the actual output voltage. AD conversion takes about 20 μs (see later). V_{off} is written as a byte, and is converted by a 10-bit DAC (with the two least significant bits grounded). This DAC has a 12-bit linearity and typical temperature coefficient of 15 ppm/^{0}C.

The external HV can be read by AD converter but cannot be set by the microprocessor. On the interface there is also a hardware protection that allows a maximum difference of about 700 V between V_{off} and the external HV. If the limit trips V_{off} is forced to follow the external HV with the specified difference, and an alarm is set : HV LIMIT.

The interface also provides the reference voltage V_{ref} for the DACs of all the channels

(see Fig. 1). The temperature coefficient of V_{ref} is about 5 ppm/°C. The actual high-voltage output is given for channel n (see Fig. 2) by :

$$V_n = \alpha \left[\frac{b \times 8}{1024} V_{off} + \frac{n}{256} I_{DAC} \times (1.25k) \right]$$

$$= \alpha \left[\frac{b \times 8}{1024} V_{off} \quad \frac{V_{ref}}{(5.1k)} (1.25k) \right]$$

where α is the ratio of the high-voltage divider, b is the byte written in the V_{off} buffer, n is the byte in the channel n, and resistors 5.1 k and 1.25 k are laser trimmed on the hybrid regulator.

5. MICROCOMPUTER

The microcomputer that controls the DATEP unit is based on the well-known Z80. Its structure is given in Fig. 4. The actual firmware makes use of less than 3 kbytes. The use of the PIO (parallel I/O) ports has already been described ; the serial RS 232C port is used for connection with a terminal in off-line operation. The microcomputer has the possibility of making automatic baud-rate evaluation.

The microcomputer board is completely compatible and interchangeable with Mostek SDB-80E or OEM-80E. The following functions are implemented in the controlling firmware :

a) operator interaction through the serial terminal (off-line operation) ;

b) CAMAC control through a special CAMAC station (on-line operation) ;

c) updating, display, and listing of the channel outputs ;

d) monitoring of channel outputs and error recognition.

6. CAMAC INTERFACE

Up to 16 DATEPs in polling connection can be handled by a computer through a single station CAMAC interface module.

Standard CAMAC functions allow the exchange of commands and messages between DATEPs and computer.

Whenever DATEP is ready to issue a message or send the answer to a previous command, a LAM is set and handled by the computer. Whenever a command is sent to a DATEP, its main program is interrupted, the command accepted and then executed.

Error conditiond are detected and memorized during check procedure. If an error condition is present after the check of the last channel, an error message is issued by the DATEP and any pending command will be ignored.

7. CONCLUSIONS

Since beginning of 1980, ten DATEP are used to control HV of the PMs of IGD while three units are used for FGD. A complete software package for the main computer has been written to allow easy set up and monitoring of the actual HV values.

Measurements made in CERN with climatic chamber show a temperature coefficient of 35 ppm/°C from 20°C to 40°C.

In Fig. 5 a typical channel output is given.

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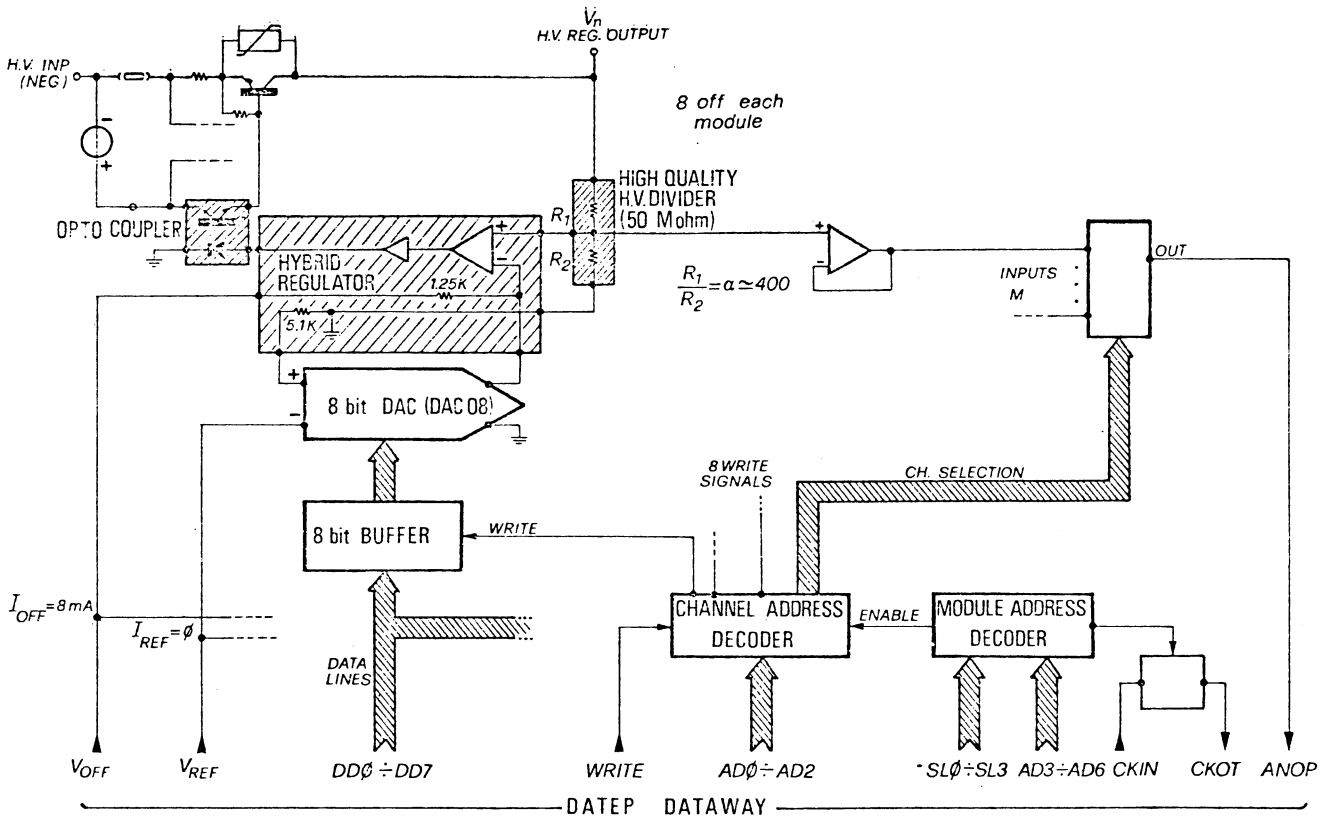

Fig. 1 H.V. regulator module

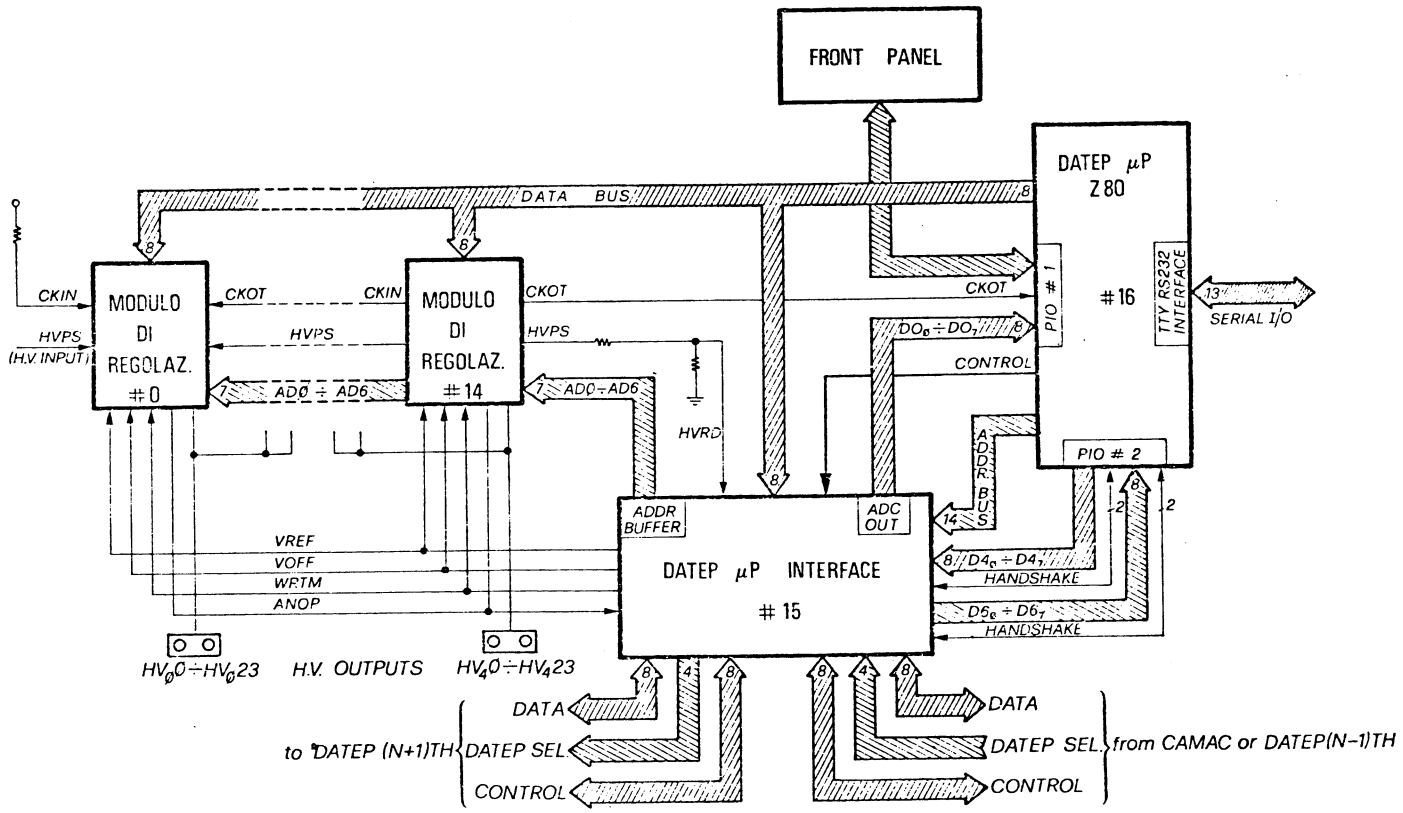

Fig. 2 Block diagram

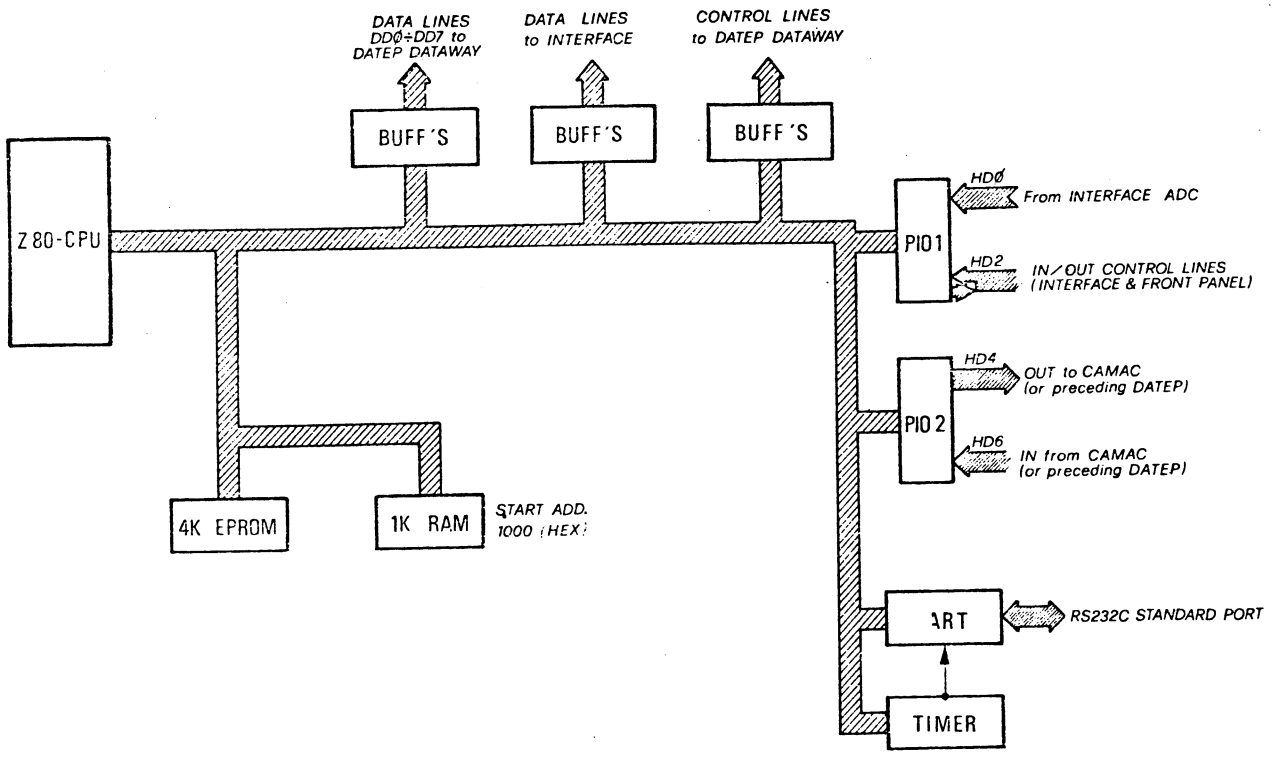

Fig. 3 Interface

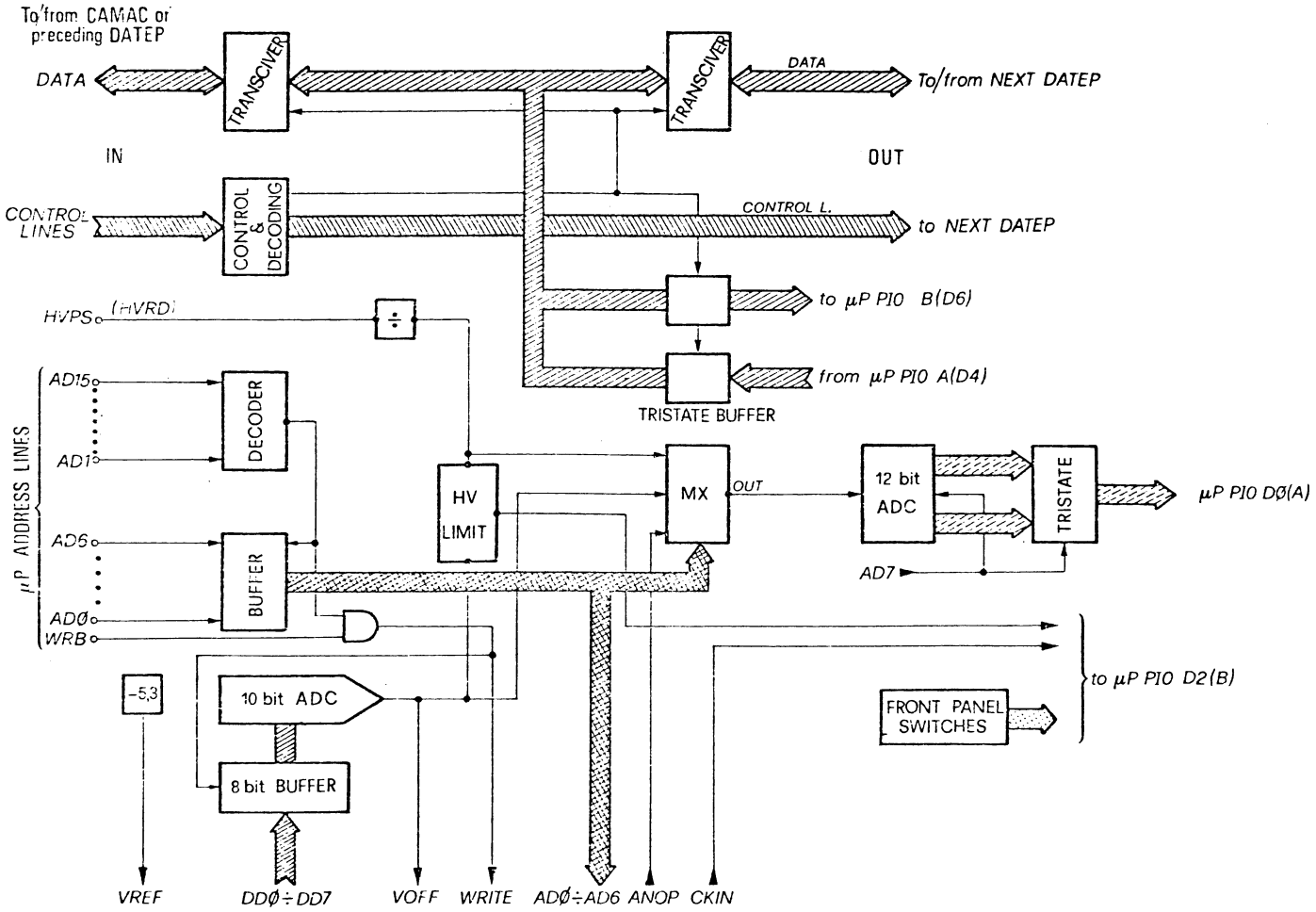

Fig. 4 μ-processor

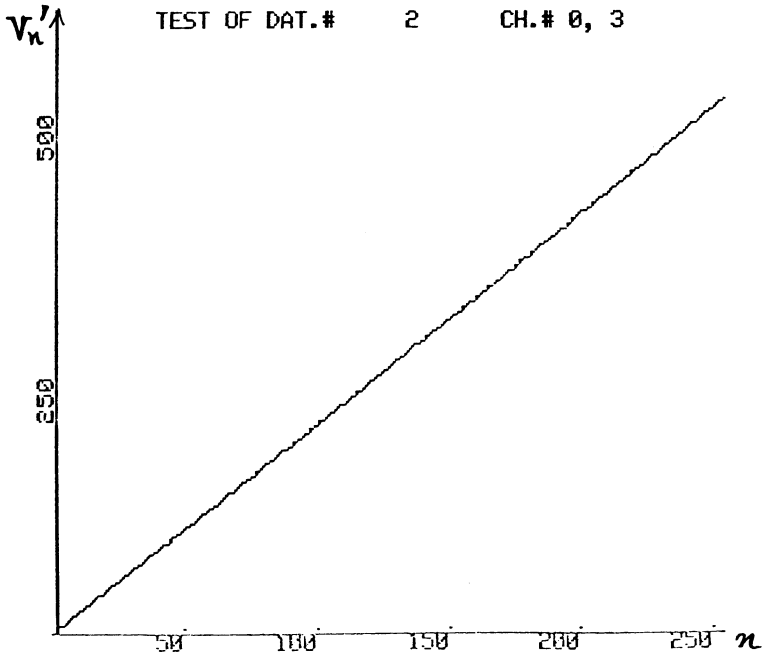

Figure 5