THE BIT SLICE MICRO-PROCESSOR "GESPRO" AS A PROJECT IN THE UA2 EXPERIMENT

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ABSTRACT

The bit slice micro-processor GESPRO, as it is proposed for use in the UA2 data acquisition chain and trigger system, is a CAMAC module plugged into a standard Elliott System crate via which it communicates as a slave with its host computer (ND, DEC). It has full control of CAMAC as a master unit.
GESPRO is a 24 bit machine (150 ns effective cycle time) with multi-mode memory addressing capacity of 64 K words. The micro-processor structure uses 5 busses including pipe-line registers to mask access time and 16 interrupt levels. The micro-program memory capacity is 2 K (RAM) words of 48 bits each. A special hardwired module allows floating point (as well as integer) multiplication of 24 x 24 bits, result in 48 bits, in about 200 ns.
This micro-processor could be used in the UA2 data acquisition chain and trigger system for the following tasks :
a) online data reduction, i.e. to read DURANDAL (fast ADC's = the hardware trigger in the experiment), process the information (effective mass calculation, etc...) resulting in accepting or rejecting the event.
b) read out and analysis of the accepted data (collect statistical information).
c) preprocess the data (calculation of pointers, address decoding, etc...).
The UA2 version of GESPRO is under construction, programs and micro-programs are under development. Hardware and software will be tested with simulated data. First results are expected in about one year from now.

I. INTRODUCTION

Designed in 1975, a first version of the bit slice micro-processor GESPRO has been successfully operated in a physics experiment (WA2/WA46) at CERN since 1977 (1), (2). This system allowed the increase of the online CAMAC data acquisition (data taking) capacity due to event selection (rejection) based on physical criteria which could be different for each type of trigger. It was also used for data reformatting of the accepted events as well as keeping track of all kinds of rejected events. The system has been developped to run on a NORD 10 computer. The experience obtained with this system has been used to develop a more sophisticated micro-processor with new hardwired operators which could also run on other computers than NORD.

II. ARCHITECTURE

The bit slice micro-processor GESPRO, as it is proposed for use in the data acquisition chain and trigger system of the UA2 experiment (3) at the $p\bar{p}$ collider at C.E.R.N., is a CAMAC module plugged into a standard Elliott System CAMAC crate via which it communicates as a slave with its host computer. In the case of UA2 this will be a VAX 11/780 (Digital Equipment). In the System crate GESPRO has full control of CAMAC as a master unit.

GESPRO is a 24 bit machine with multimode memory addressing capacity of 64 K words in modules of 8 K. Its effective cycle time is 150 ns. The microprocessor structure uses 5 busses including pipe-line registers to mask access time and 16 interupt levels. The layout of the machine is shown in figure 1. The main structure of the micro-processor is based on the series INTEL 3000. 15 of the 16 interupt levels may be used either by hardware or by software. Actually 12 interupts are forseen for hardware use.

The micro-program memory capacity is 2 K (RAM) words of 48 bits each. The micro-instruction format is shown in figure 2. One instruction contains 4 fields which are working in parallel. This allows simultaneous execution of jump instructions, logical or arithmetical operations, mask operations and special hardwired operator activations.

A special hardwired module allows floating point as well as integer multiplication of 24 x 24 bits, result in 48 bits, in about 200 ns.

GESPRO software (operation system) is written in assembler language including specialized microprogrammed tasks. A cross-assembler, a micro-code compiler and a debugging program of micro-programs are available on NORD 10 (NORD 100) computers. The programs and micro-programs, specialized for the application, have to be developped individually. When power starts up, the micro-processor has to be loaded once with a special micro-program memory loader CAMAC module.

III. APPLICATION AND OUTLINE

The micro-processor GESPRO, as described above, could be used in the UA2 data acquisition chain and trigger system for the following tasks :

a) online data reduction ;
   i.e. to read out only a part of the detector, the DURANDAL (those are fast ADC's which define the second level hardware trigger of the experiment), then to process the information (effective mass calculation, etc...) resulting in accepting or rejecting the event.
b) read out and analysis of the full set of accepted data (collect statistical information).
c) preprocess the data (calculation of pointers and multiplicities, address decoding, etc.)
d) select or at least flag special trigger events defined by physical criteria.

The advantage of preprocessing the data in such a way is obvious. One keeps flexibility in the application due to programming ; in addition the micro-programming will allow for high speed in processing. For the host computer the work will be substancially reduced due to event rejection and the prestructuring. Therefore the host computer will be mostly available for online control of the experiment. The number of data tapes will be reduced and a gain in computer time of the big computers for writing data summary tapes may be obtained.

The UA2 version of GESPRO is presently under construction. The hardware is nearly finished, and has been successfully tested. Most programs and micro-programs are under development. A special hardware configuration will be prepared to simulate the hardware of the experiment. The hardware and the software of the micro-processor will then be tested with this configuration on simulated data. Machine and running software will be operational at the end of this year. First results are expected in one year from now.

REFERENCES

(1) Multiprocessor acquisition system including a special purpose CAMAC dedicated microprocessor .
Y. LECOQ et al., C.R.N.-HE 78-16

(2) Particle and antiparticle production by 200 GeV/c protons in the charged Hyperon Beam at the CERN SPS.
M. BOURQUIN et al., Nucl. Phys. B153 (1979) 13.

(3) UA2 Data acquisition
V. HUNGERBÜHLER, Contribution to this conference.

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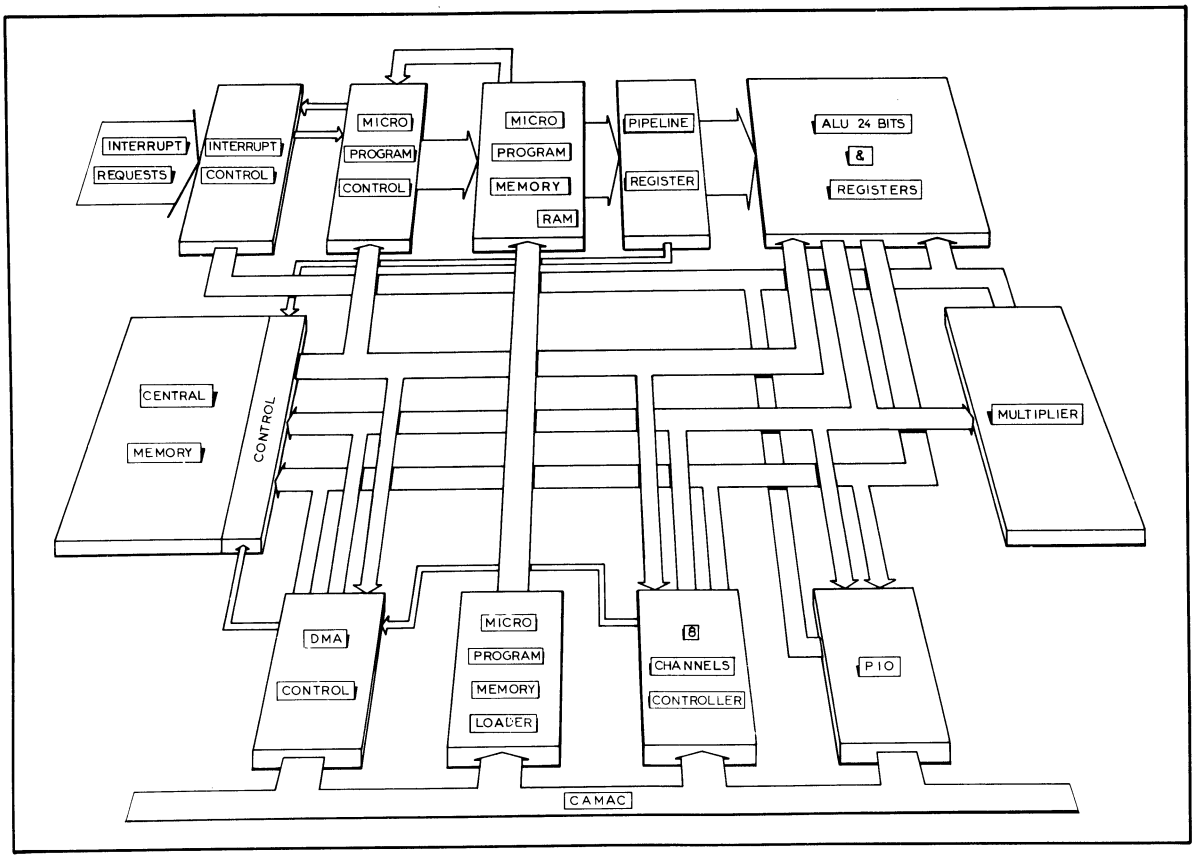

Fig. 1 Layout of the hardware structure of GESPRO

MICRO INSTRUCTION FORMAT (48 BITS)

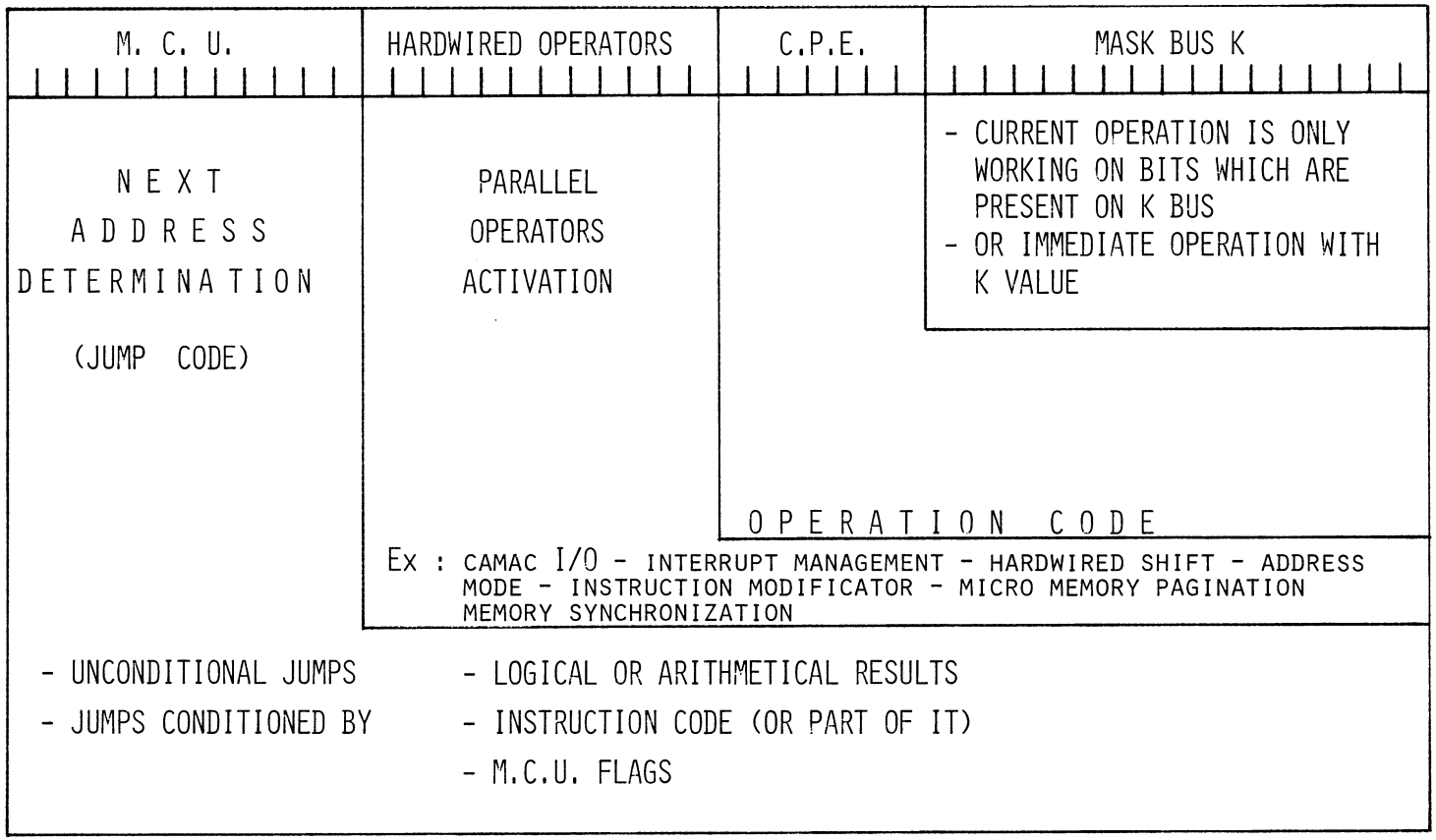

Fig. 2 Micro-instruction format