

INTELLIGENT TRIGGER PROCESSOR FOR THE CRYSTAL BOX

by

G.H. Sanders, H.S. Butler, M.D. Cooper, G.W. Hart, C.M. Hoffman,
G.E. Hogan, H.S. Matis, V.D. Sandberg, R.A. Williams
Los Alamos National Laboratory, Los Alamos, NM 87545

E.B. Hughes, J. Rolfe, S. Wilson, H. Zeman
High Energy Physics Laboratory and Department of Physics,
Stanford University, Stanford, CA 94305

ABSTRACT

A large solid angle modular NaI(Tl) detector with 432 phototubes and 88 trigger scintillators is being used to search simultaneously for three lepton flavor changing decays of the muon. A beam of up to 10^6 muons stopping per second with a 6% duty factor would yield up to 1000 triggers per second from random triple coincidences. A reduction of the trigger rate to 10 Hz is required from a hardwired primary trigger processor described in this paper. Further reduction to <1 Hz is achieved by a microprocessor based secondary trigger processor.

The primary trigger hardware imposes voter coincidence logic, stringent timing requirements, and a non-adjacency requirement in the trigger scintillators defined by hardwired circuits. Sophisticated geometric requirements are imposed by a PROM-based matrix logic, and energy and vector-momentum cuts are imposed by a hardwired processor using LSI flash ADC's and digital arithmetic logic. The secondary trigger employs four satellite microprocessors to do a sparse data scan, multiplex the data acquisition channels and apply additional event filtering.

I. INTRODUCTION

A new experimental facility is being constructed at the 800 MeV Los Alamos Meson Physics Facility (LAMPF) to study extremely rare processes. The apparatus, referred to as the Crystal Box, consists of a large solid angle modular sodium iodide detector, surrounding a trigger hodoscope and a cylindrical drift chamber. The first application of this detector is a simultaneous search for the lepton flavor changing decays of the positive muon to $e^+\gamma$, $e^+\gamma\gamma$, and $e^+e^+e^-$, with a sensitivity to branching ratios as low as 1×10^{-11} .

High incident muon rates and copious accidental triggers require a sophisticated trigger processor to reduce the volume of recorded data. The system designed for this application is a multilevel assembly of hardwired logic, programmable matrix logic and microprocessor based devices. A major portion of the system has been tested with a prototype version of the detector.

II. THE DETECTOR

Figure 1 is a representation of the Crystal Box. Covering more than 2π steradians to assure high acceptance for the 3-body decays, it consists of 360 sodium iodide modules, 6.35 cm x 6.35 cm cross-section and 30.5 cm (12 radiation lengths) long, plus 36-corner crystals 6.35 cm x 6.35 cm and 63.5 cm long. All crystals are packaged in a single hermetically sealed enclosure, isolated only optically from each other. The design energy resolution of 5% at 52.8 MeV provides strong rejection of unwanted backgrounds.

The array surrounds a central rectangular volume approximately 64 cm x 64 cm and 66 cm long. The central region contains the muon stopping target, a cylindrical drift chamber and trigger hodoscope. The stopping target consists of 1.3 mm of polyethylene, tilted at 45° with respect to the beam and presenting a cross section 10 cm in diameter. This arrangement optimizes the vertex resolution, enhancing the rejection of random coincidences.

The drift chamber has eight signal planes with a total of 728 cells. Employing 10° - 16° stereo, it is designed to present as little material as possible to the electrons and photons traversing it.

The trigger hodoscope consists of 36 scintillators, with each scintillator covering one row of 10 crystals. The scintillator material, Pilot B, is 1.27 cm thick and 5.7 cm wide, but covers only the central seven crystals in each row to insure full shower containment. The scintillators are thus only 44.5 cm long with 15 cm long light pipes at each end, coupled to XP2232 photomultipliers. An electron is identified by a coincident signal from a sodium iodide crystal and the scintillator in front of it. A photon is denoted by a sodium iodide signal accompanied by no response from the plastic counters. This photon veto function is made complete by 16 guard counters covering the insensitive end regions of the primary hodoscope counters.

III. THE RAW TRIGGER RATES

The trigger processor described in this paper, and a great deal of the other custom designed electronics described elsewhere is motivated by the high raw trigger rate we encounter compared to the rarity of the processes we are searching for, and the extraordinary cost of implementing the hardware portion of the trigger with commercial electronics.

A. The Beam

The LAMPF beam seen by a user in the Stopped Muon Channel consists of up to 120 macropulses per second, with duration varying from approximately 500 microseconds to 750 microseconds, or a duty factor between 6% and 9%. This implies high instantaneous rates in our detector when the muon stopping rate is between 1×10^5 Hz and 2×10^6 Hz. In addition, there is a strong incentive to completely process the data taken in 1 macropulse during the roughly 8 milliseconds between pulses. A desirable goal is then to pass no more than one or two triggers per pulse to the on-line computer.

B. The $\mu \rightarrow eee$ Reaction: Raw Rates

For the $\mu \rightarrow eee$ reaction, the raw trigger rate comes from triple random coincidences from normal muon decay. The hardware trigger is formed purely from the plastic trigger scintillators. The logic requires that at least three trigger counters fire within 5 ns, and that no two adjacent counters are involved in this coincidence. We refer to these two requirements as SIMULTANEITY and NON-ADJACENCY, and we will describe two modules designed to implement these requirements.

The raw trigger rate is given by

$$\#triggers/sec \text{ (average)} = (\#\mu/sec)^3 (\tau_R)^2 (\Omega_i^3 / DF^2) (N)(N-3)X(N-6) \quad (1)$$

where

$\#\mu/sec$ = average μ stopping rate

τ_R = coincidence resolving time = 5 ns

Ω_i = solid angle/ 4π of average scintillator = $0.54/36 = 0.15$

DF = duty factor in meson area after linac beam is distributed to various beam lines = 0.06

N = 36 counters.

This set of assumptions gives

$$\text{average } \#triggers/sec = (8.35 \times 10^{-16})(\#\mu/sec)^3. \quad (2)$$

Table I gives the trigger rates and scintillator singles rates under several assumptions for the μ stopping rate. We use 6% useful duty factor throughout.

Without further on-line suppression, $5 \times 10^5 \mu/\text{sec}$ is the highest rate at which we could expect to run the experiment, in order to limit the trigger rate to no more than a few per macropulse.

Average μ/sec	Inst. μ/sec	Average Rate/Counter	Inst. Rate/Counter	Average Trigger Rate	Inst. Trigger Rate	Trigger/ Pulse
1×10^5	1.7 MHz	1.5 kHz	25 kHz	0.84 Hz	14 Hz	0.007
3×10^5	5 MHz	4.5 kHz	75 kHz	23 Hz	376 Hz	0.2
5×10^5	8.3 MHz	7.5 kHz	125 kHz	104 Hz	1.7 kHz	1
1×10^6	17 MHz	15 kHz	250 kHz	835 Hz	14 kHz	7
2×10^6	33 MHz	30 kHz	500 kHz	6.7 kHz	111 kHz	56

C. The $\mu \rightarrow e\gamma\gamma$ Reactions: Raw Rates

Both the plastic scintillators (trigger and guard counters) and the sodium iodide crystals participate in the trigger. In principle, a positron can be logically defined as a scintillator in coincidence with contiguous sodium iodide crystals and a photon can be logically defined as sodium iodide signals with no coincident scintillator signal. However, there are many problems that make such a scheme extremely difficult to implement. These problems include defining "contiguous." How close to a scintillator must the sodium iodide crystal be? How do we define an energy threshold (should the threshold be on an individual crystal or on a "cluster")? How does one differentiate between a shower with a lot of spreading and a positron close to a photon? To circumvent these problems, the trigger logic is defined around detector quadrants. A quadrant with a positron (i.e., a scintillator signal) is defined as a positron even if it also has a photon. A quadrant with sodium iodide signals but no scintillator is called a photon. An $e\gamma\gamma$ trigger requires one and only one positron quadrant and two other photon quadrants. An $e\gamma$ trigger requires a positron quadrant and a photon quadrant opposite to the positron. Note that an $e\gamma\gamma$ event with two of the particles close to each other is considered an $e\gamma$ trigger: the two event types are separated off-line.

The raw trigger rate for $\mu \rightarrow e\gamma\gamma$ is given by

$$\# \text{triggers/sec (average)} = (\# \mu/\text{sec})^3 (\gamma_p)^2 (\tau_R)^2 (\Omega/4\pi)^3 1/DF^2 (3/4) (3/4) \quad (3)$$

where

μ/sec = average stopping μ rate yielding an electron for each μ decay

γ_p = probability of conversion to a photon = 0.01

τ_R = coincidence resolving time used in $e\gamma\gamma$ logic = 15 ns

$\Omega/4\pi$ = solid angle $/4\pi$ = 0.54

DF = meson area duty factor = 0.06.

This gives

$$\text{average } \# \text{triggers/sec} = 3.69 \times 10^{-19} (\# \mu/\text{sec})^3 \quad (4)$$

from triple randoms. The trigger rate from random coincidence of an e^+ with the process $\mu^+ \rightarrow e^+ \gamma \nu \nu$ is comparable. Table II shows the trigger rates and singles rates for a range of μ stopping rates. Part (c) of the table shows the rate for 2-body $e\gamma$ triggers given by

$$\# \text{triggers/sec (average)} = (\mu/\text{sec})^2 \gamma_p \tau_R (\Omega/4\pi)^2 1/DF (1/4) = (\mu/\text{sec})^2 1.82 \times 10^{-10}. \quad (5)$$

Once again, the desire to trigger at less than one trigger per macropulse indicates an upper limit of $5 \times 10^5 \mu/\text{sec}$ for the 2-body $e\gamma$ trigger.

Thus, a $\mu \rightarrow eee$ trigger rate of one per pulse, in parallel with a 2-body $e\gamma$ trigger of ≤ 1 per pulse is the way to run the experiment. The μ stopping rate would then be between 3 and 5×10^5 Hz. From Table II(a), this stopping rate is also about as high as one should go, considering sodium iodide singles rates. At 5×10^5 μ /sec, the single crystal rate is about 750 Hz. Since about 10 crystals participate in a shower, a conservative estimate of the singles rate in a crystal is really closer to 7.5 kHz. With 250 ns NaI pulse widths, the pile-up probability is about 0.5 percent. This increases linearly with stopping rate. The singles rate per quadrant is already up to a megahertz.

TABLE II (a),(b),(c)						
(a) Single Rates:						
<u>Average</u> <u>μ/sec</u>	<u>Inst.</u> <u>μ/sec</u>	<u>Average</u> <u>Rate/Crystal</u>	<u>Average</u> <u>Rate/Row</u>	<u>Average</u> <u>Rate/Quad</u>	<u>Inst.</u> <u>Rate/Crystal</u>	<u>Inst.</u> <u>Rate/Quad</u>
1×10^5	1.7 MHz	0.15 kHz	1.5 kHz	13.5 kHz	2.5 kHz	225 kHz
3×10^5	5 MHz	0.45 kHz	4.5 kHz	41 kHz	7.5 kHz	675 kHz
5×10^5	8.3 MHz	0.75 kHz	7.5 kHz	67.5 kHz	12.5 kHz	1.13 MHz
1×10^6	17 MHz	1.5 kHz	15 kHz	135 kHz	25 kHz	2.25 MHz
2×10^6	33 MHz	3.0 kHz	30 kHz	270 kHz	50 kHz	4.5 MHz

(b) $\mu \rightarrow e\gamma\gamma$ 3-body Trigger Rates:				
<u>Average</u> <u>μ/sec</u>	<u>Inst.</u> <u>μ/sec</u>	<u>Average</u> <u>Trigger Rate</u>	<u>Inst.</u> <u>Trigger Rate</u>	<u>Trigger/</u> <u>Pulse</u>
1×10^5	1.7 MHz	3.6×10^{-4} Hz	0.006 Hz	5×10^{-5}
3×10^5	5 MHz	0.01 Hz	0.165 Hz	0.001
5×10^5	8.3 MHz	0.046 Hz	0.77 Hz	0.006
1×10^6	17 MHz	0.37 Hz	6.2 Hz	0.05
2×10^6	33 MHz	3 Hz	49 Hz	0.4

(c) $\mu \rightarrow e\gamma\gamma, e\gamma$ 2-body Trigger Rates:				
<u>Average</u> <u>μ/sec</u>	<u>Inst.</u> <u>μ/sec</u>	<u>Average</u> <u>Trigger Rate</u>	<u>Inst.</u> <u>Trigger Rate</u>	<u>Trigger/</u> <u>Pulse</u>
1×10^5	1.7 MHz	1.8 Hz	30 Hz	0.015
3×10^5	5 MHz	17 Hz	250 Hz	0.125
5×10^5	8.3 MHz	46 Hz	750 Hz	0.4
1×10^6	17 MHz	180 Hz	3 kHz	1.5
2×10^6	33 MHz	729 Hz	12 kHz	6

Early measurements with prototype detector modules confirm the rates we have described. The conclusion is that a number of considerations conspire to select a stopping rate of 5×10^5 μ /sec as a peak beam intensity. Additional intensity requires fast trigger suppression and pile-up rejection. At the indicated intensity, the combined raw trigger rate is approximately two per macropulse, or 240 Hz. The ultimate goal is to operate the experiment at even higher rates.

For the moment, we have required that the primary hardware trigger processor provide an overall suppression of at least 10. The secondary microprocessor based system would then have to respond to an average trigger rate of 10 to 20 Hz with a 6% duty factor.

IV. THE INTELLIGENT TRIGGER PROCESSOR

The system we have designed consists of two main subsystems. The primary trigger hardware is required to trigger on all three reactions in parallel and to suppress the combined raw trigger rate by more than a factor of 10. The primary system consists of

conventional commercial fast logic, hardwired ECL-based logic of our own design, and logic employing information stored in programmable read-only memories (PROM's).

The secondary processor employs four satellite microprocessors, one for each crystal quadrant, to acquire and preprocess the data. A Microprogrammable Branch Driver (MBD) acquires the scintillator and drift chamber data. These five microcomputers substantially reduce the volume of information to be transferred to the on-line computer and monitor the sodium iodide calibration as well. Final filtering of the data occurs in the on-line PDP-11/44 that should write to tape at event rates no more than 1 or 2 Hz. The overall reduction in recorded events lies somewhere between a factor of 100 to 1000.

V. THE PRIMARY TRIGGER

This subsystem consists of separate trigger logic for the $\mu \rightarrow eee$ reaction, and the $\mu \rightarrow e\gamma$ and $\mu \rightarrow e\gamma\gamma$ reactions. We will first describe the logic requirements imposed on each portion of the primary trigger and then describe the specific implementation.

A. $\mu \rightarrow eee$ Trigger Specification

1. SIMULTANEITY - This requirement is the ability to accept coincidences of three scintillator hits whose timing pulses are all within ± 2.5 nanoseconds of each other. To achieve this cleanly requires a 36 input voter coincidence module with high system bandwidth, discriminator performance free of anomalies, slewing and walk, and removal of timing walk induced by position dependence in the trigger counters.
2. NON-ADJACENCY - In real time, comparable to the SIMULTANEITY logic, we must accept only those triggers where at least three hits occur in a cleanly separated way. We must reject those events where two hits are in adjacent counters, lest we accept false triggers induced by soft electromagnetic showers illuminating neighboring counters. The matrix logic employed must have speed comparable to the SIMULTANEITY logic.
3. PRETRIGGER - A simple, primitive pretrigger is required in order to strobe the higher level portions of the logic. We use the coincidence of SIMULTANEITY and NON-ADJACENCY.
4. GEOMETRY - The topology of legal 3-body decays is quite different from the distribution of random triple coincidences. Imposing this requirement with a hardware matrix logic is fast and simple. Based on Monte Carlo simulation, it suppresses the raw trigger rate by about a factor of four including the non-adjacency suppression. The matrix logic requires the state of the trigger counters to be latched upon a pretrigger. This latch circuit can also be used for automated system exercising, and for the slow data acquisition.
5. VECTOR MOMENTUM - The GEOMETRY requirement is a crude kinematic cut. It allows only those geometries consistent with a 3-body decay of a particle at rest. An additional and more stringent requirement is the imposition of hardware cuts on the total energy of the three bodies, or even the vector momentum sum. The key electronic capability is fast, cheap digitization of sodium iodide pulse height in real time. This must be done to about 6-bit accuracy in less than 100 nanoseconds.

B. $\mu \rightarrow e\gamma\gamma$ and $e\gamma$ Trigger Specifications

The 2- and 3-body logic are accommodated simultaneously, though we have shown the 2-body trigger rate will clearly dominate. Since these rates are modest, a relatively loose trigger based upon quadrants of 90 crystals (with associated corner crystals) as the

basic trigger elements appears to be sufficient. Using quadrants, we impose the various requirements of particle identification, time coincidence, geometry and energy.

1. PARTICLE IDENTIFICATION - The reaction $\mu \rightarrow e\gamma$ is a 2-body reaction with one positron and one photon. The signal for an electron (positron) is a shower in the sodium iodide crystals of a quadrant in coincidence with a scintillator from that quadrant. The scintillators used are the double-ended counters covering the fiducial area of the quadrant. A photon is identified by a sodium iodide shower in any quadrant vetoed by any scintillator firing in that quadrant. A veto can come from a double-ended counter, or one of the guard counters.

The 3-body reaction $\mu \rightarrow e\gamma\gamma$ requires three quadrants with appropriate particle identification. It should be noted that these are fairly loose requirements since the trigger does not associate the signals from the plastic detectors and the sodium iodide more precisely than on a quadrant by quadrant basis. Final purification can be done in the on-line or off-line software. The trigger purity will deteriorate at high rates, and we may eventually need a tight trigger.

2. TIME COINCIDENCE - Since these reactions are triggered by plastic scintillator-sodium iodide coincidences, the time resolution must be limited by the sodium iodide. With the timing discriminators we have developed^{1]} a real-time resolution of 10-15 ns is very conservative. The most serious source of error in the on-line timing resolution comes from the use of entire quadrants of crystals as trigger elements.

The sodium iodide discriminator outputs for individual crystals are logically OR'd on a quadrant wide basis. The timing distribution in the trigger is smeared by the quadrature sum of many crystals, skewed by early firing crystals. We shall see this in a discussion of the proposed logic.

3. GEOMETRY - The 2-body reaction must always populate back-to-back quadrants. The logic requires an e^+ and γ in opposite quadrants.

The 3-body reaction has a similar geometry. Legal triggers come from an e^+ with either two photons or more in any other quadrants, or an $e^+\gamma$ trigger as composed in the 2-body reaction (with an energy requirement of 90 to 120 MeV in all three).

4. ENERGY - The 2-body trigger must have approximately 50 MeV in each back-to-back quadrant. The 3-body trigger must sum all quadrants to approximately 105 MeV.

VI. THE IMPLEMENTATION OF THE PRIMARY TRIGGER

Parallel to our description of the required trigger algorithms, we describe the specific design used.

A. $\mu \rightarrow eee$ Trigger Logic

Figure 2 illustrates this portion of the system. Signals from each end of the double-ended trigger counters are split into two portions. One is recorded by a CAMAC ADC when a trigger occurs. The remainder fires the timing discriminator^{1]} we have developed for this detector. One output from each discriminator is fed to a meantimer circuit^{2]} also developed for this experiment. The meantimer produces an output whose timing is independent of the relative timing of each of the two input signals, effectively removing position dependence in the timing information from the long counters.

One meantimer output goes to the $\mu \rightarrow e\gamma$ and $\mu \rightarrow e\gamma\gamma$ logic. A special high edge-speed output goes to a module that imposes the SIMULTANEITY requirement. This custom circuit, which will be described in a later publication, produces an output if three or more inputs arrive within ± 2.5 nanoseconds of each other.

Another meantimer output is used by a NON-ADJACENCY module based upon previous work,^{3]} but adapted to our needs. It receives 36 inputs and turns off outputs corresponding to adjacent counters. A second module, identical to the SIMULTANEITY box, is used as a voter coincidence on its outputs, though the timing requirements are not as tight as in the SIMULTANEITY trigger. The NON-ADJACENCY logic necessarily distorts the timing information, so the two requirements are imposed separately, rather than in a single circuit.

The SIMULTANEITY and NON-ADJACENCY outputs are put into coincidence, with the timing determined by the SIMULTANEITY signal. This coincidence is used as the PRETRIGGER, which is one component of the $\mu \rightarrow eee$ trigger and provides a gate to the latch module shown.

The latch module provides the levels for the GEOMETRY matrix logic. It also provides the ability to exercise the system through CAMAC. Designed for this detector, the latch module provides standard NIM inputs and a NIM gate, parallel ECL level outputs, and TTL level shift register inputs and outputs. This flexibility facilitates computer-controlled system diagnosis. The ECL level outputs are presented to the GEOMETRY matrix logic.

Our original concept for the GEOMETRY matrix module employed a standard ECL gate matrix to define legal and illegal 3-counter combinations, similar to previous work by one of us.^{4]} The approximately 36^3 combinations, reduced even by the 8-fold symmetry of our detector, would have required an exceptionally large number of integrated circuits. The high speed required of this module (<50 ns) dictated ECL logic speed. The design has settled upon the use of ECL programmable read-only memory (PROM) chips (Motorola MCML0149), which provide access times between 7 and 25 ns.^{5]} Employing all the symmetry of the detector, all legal combinations of three counters, including events with additional struck counters, can be programmed into 144 of these 256 x 4 bit PROM's. A Monte-Carlo calculation provides us with the list of legal 3-counter hits that are then burned into the PROM's. Later changes in the apparatus, such as reduced target size or increased material in front of the trigger counters can be accommodated by recalculating these legal hits and reprogramming the small number of PROM's affected. The circuit details and performance will appear in a later publication.

The final component of the $\mu \rightarrow 3e$ trigger is the VECTOR MOMENTUM circuit. This portion of our system is not yet fully developed, and we intend to run the early stages of our experiment without it. The key technology has, however, been developed and used by us in a prototype version. For each row of sodium iodide crystals, a linear sum is formed as part of the $\mu \rightarrow e\gamma$ and $e\gamma\gamma$ triggers. This sum is converted to a 6-bit digital number by a peak sensing ADC using the TRW1014J^{6]} flash ADC chip. Conversion is completed typically within 30 nanoseconds, and data rates up to 30 MHz are possible. With 6-bit accuracy and an arithmetic processor to apply a vector momentum cut in three dimensions, an order of magnitude suppression of our trigger rate is predicted. The exact suppression is dependent on the final design details.

The 16 guard counters with single photomultiplier tubes are shown in Fig. 2 with their pulse splitters and timing discriminators. They are not used in the $\mu \rightarrow eee$ trigger.

B. $\mu \rightarrow e\gamma\gamma$ and $\mu \rightarrow e\gamma$ Trigger Logic

The sodium iodide is used more extensively in forming these triggers. The front end circuit for the 360 regular crystals and the 36 double-ended corner crystals is shown in Fig. 3. Each raw signal passes through a filter circuit designed to clip and compress the

pulse. Superior to a cable clip, the details will appear in a later publication. Its main purpose is to minimize pile-up at the high singles rates we expect. The clip filters are followed by a 3-way signal splitter and a gain of 10 amplifier that supplies sufficient signal amplitude for the timing discriminators.

The timing discriminators are identical to those used on the scintillators except for the adjustment of the constant fraction circuit, which is optimized for the sodium iodide pulses. The discriminator outputs are used for the timing portion of this trigger, and for the precision time-to-amplitude (TAC) converters used in the secondary system described below.

A second fraction of the analog signal is digitized by precision integrate-and-hold modules multiplexed to an ADC by the intelligent multiplexers also mentioned in our discussion of the secondary system. The remaining analog signal is applied to linear summing circuits to form energy sums for the rows and quadrants of crystals.

Figure 4(a) shows how the linear sums are formed for each of the rows and the corner crystals of one quadrant. LeCroy 127FL linear fan-in modules are used for this function. These sums are used in the VECTOR MOMENTUM hardware previously described, and in the $\mu \rightarrow e\gamma$ and $\mu \rightarrow e\gamma\gamma$ trigger described below.

Figure 4(b) illustrates the use of the timing discriminator outputs to form a time signal for use in the $\mu \rightarrow e\gamma$ and $\mu \rightarrow e\gamma\gamma$ trigger. A special 90 input logic fan-in has been developed to provide a single time signal for each quadrant. Individual row signals and test inputs are indicated. This relatively crude technique should be sufficient at the stopping rate of 5×10^5 Hz, where Table II(a) indicates the quadrant singles rate is 67.5 kHz.

Figure 5 describes the central portion of the trigger hardware for the two photon reactions. Each quadrant is identified as an electron or photon quadrant by the logic shown. The quadrant signal from the timing fan-in is put in coincidence with the trigger scintillators to denote an electron. A veto is formed from the trigger and guard counters, to identify the photon.

The linear sum of the sodium iodide signals is used for two kinds of energy cut. The $\mu \rightarrow e\gamma$ trigger requires a back-to-back deposit near 50 MeV in each of two quadrants. A total energy sum close to 105 MeV is required for the $e\gamma\gamma$ trigger. The details of this implementation are straightforward, employing standard commercial electronics.

VIII. THE SECONDARY TRIGGER AND DATA ACQUISITION SYSTEM

Having formed one of three different primary trigger signals corresponding to the three reactions under investigation, additional processing of the data is required to reduce both the trigger rate and the number of data words per event. A secondary system employing several microprocessors has been developed to carry out these additional requirements.

The combined primary trigger rate is about 10 Hz, after employing the hardware trigger logic described above. At a muon stopping rate of 5×10^5 Hz, with a data collection time of 4×10^6 seconds, the experiment will sample 2×10^{12} muon decays. At 10 Hz, the secondary system will process 4×10^7 events.

Each event contains pulse height and time information from 432 sodium iodide channels, pulse height and time information from 88 scintillator channels, time information from 728 drift chamber wires, 120 scaler channels, and assorted latch bits and status words. Without compaction, more than 1000 words would be required per event.

Since most channels are empty in a real event, considerable reduction in the volume of information recorded by the data acquisition system can be achieved by eliminating empty channels.

Calculations and preliminary tests with the hardware indicate an average event will contain only 70 drift chamber signals and 200 words of data from the sodium iodide. The sparse data scan for the drift chamber is performed by commercial hardware (the LeCroy 4290 system). Our secondary hardware performs this function for the crystal data.

Given the above conditions, three main goals were established for the secondary system. Events had to be processed, on the average, in the 8 milliseconds between accelerator pulses. We refined this to include the capability to handle two events in consecutive pulses, but not events in three consecutive pulses. The incident trigger rate had to be reduced from 10 Hz to a rate of 1 Hz written on magnetic tape. Each event had to contain about 350 words, implying removal of empty channels. This would confine the recorded data during the entire experiment to 500 magnetic tapes.

At the LAMPF laboratory, a considerable body of data acquisition hardware and software has been developed, and we felt constrained to use as much of this system as possible. An extensive network of PDP-11 computers exists, with at least one at each beam line. Most data is taken through CAMAC using a Microprogrammable Branch Driver (MBD).^{7]} The software supporting this configuration is a standardized, powerful program called "Q".^{8]}

Early tests with the main data acquisition PDP-11 showed that it could not fulfill all three of our goals. It could not discard empty data channels and apply additional cuts to reduce the 10 Hz trigger rate. The MBD processor possesses no floating point capability, so it is not suitable for event cuts, and it is too slow to do the sparse data scan on all 432 sodium iodide channels in the time allotted.

An additional level of intelligence was added to the system in the form of four LSI-11/23 microcomputers with one assigned to each quadrant.

Figure 6 illustrates the essential features of the secondary trigger processor in a schematic form. The 90 crystals in one quadrant (and the 18 corner crystal signals) are connected to specially designed integrate-and-hold modules and time-to-amplitude converters, as shown in Fig. 3. These modules integrate a signal in response to a master trigger from the primary trigger hardware. The integrated result for each channel is held until the LSI-11/23 commands the multiplexer to connect each channel to the precision ADC for digitization. The LSI-11/23 thus acquires each of the 216 data words produced by this operation. Each channel is tested and the set of data is reduced to contain only the active data channels. Thus, the main functions performed for us by the LSI-11/23 are the crystal data acquisition, multiplex control and sparse data scan. Communication between this "Intelligent Multiplexer" and the ADC and hardware multiplexer is through a direct interface designed by us. Communication with the CAMAC branch highway is through the Auxiliary Crate Controller (ACC) via the "Q-bus".^{9]} This differs from the more common practice of connecting the ADC directly through the CAMAC dataway.

The LSI-11/23 performs an additional function, and is capable of an important additional role if needed in the future. During the experiment, the gains of the 432 sodium iodide channels must be continuously monitored and controlled in order to achieve the design energy resolution. After initial and periodic calibration, the gains are stabilized by an additional event trigger active only during the last 5% of any

accelerator pulse not producing an ordinary trigger. During this stabilization period, the hardware will accept a trigger from a single ordinary muon decay. The characteristic shape and energy cutoff of the Michel spectrum will be stored in the LSI-11/23 for each crystal in the quadrant. These spectra are used by the main data acquisition PDP-11/44 to update the individual channel gains during the run.

The additional kinematic cuts needed for reduction of the trigger rate from 10 Hz to a tapping rate of 1 Hz could be performed in the LSI-11/23 processors. This would necessitate considerable communication between the four satellite processors. To avoid this complexity, these cuts will be performed within the main PDP-11/44, an acceptable situation under our initial running conditions. At a later time, however, these cuts may be performed upstream by allowing one LSI-11/23 to access all four memories after the sparse data scan is complete. A fast Special Processor Unit (SPU) with a 142 ns cycle time could be added to speed this process. Thus, we may eventually perform the multiplexing, sparse data scan, and cuts entirely within the Intelligent Multiplexers.

The Auxiliary Crate Controller system we use consists of the BiRa Model 1101 ACC Q-bus Adapter, the BiRa Model 1151 ACC Dataway Access Port and the BiRa Model 1150 ACC Control Port. The specific roles performed by these modules are described in Ref. 9, and the manufacturer's literature. The ACC controls the communication between the LSI-11/23 Q-bus and the CAMAC dataway and is responsible for setting system flags and providing system synchronization.

Figure 7 is a more detailed view of the secondary system emphasizing the circuitry for one crystal quadrant and elucidating the arrangement of event trigger pulses, system status signals, and synchronization pulses. This specific arrangement has been used by us in a recent test run.

If the operator and computer signal a ready condition, the logic enables either the normal master trigger or the stabilization event trigger as selected. The appropriate trigger causes a hardware interrupt in the LSI-11/23 processor, the CAMAC modules used in the drift chamber and scintillator data acquisition, and the event trigger module. The latter module signals the MBD with the appropriate "Q-event"^{8]} number. Events 9 and 10 are thus triggered by the hardware and initiate acquisition by the MBD of the drift chamber and scintillator data. Simultaneously with this process, the Intelligent Multiplexer system is acquiring and processing the crystal data. With event levels 9 and 10 triggered the MBD processes, in priority order, event level 10, followed by 9. The last operation performed in processing event 9 is the software triggering of event levels 11 and 12. The LSI-11/23 is interrogated to determine if it has completed processing its crystal data. When this condition is achieved, the MBD receives the crystal data. At the completion of processing event level 12, the MBD software responds to event 11, and dumps, in a synchronized manner, all portions of the specific physical event to the PDP-11/44. Hardware signals employed in the system are shown in Fig. 7.

The system allows us to compress the data acquisition time by using a considerable amount of distributed parallel processing. It can handle two master triggers during consecutive machine pulses. Furthermore, it is easily modified or expanded due to the flexible architecture and software.

During a stabilization event in which single positrons from muon decay are recorded, the LSI-11/23 acquires the crystal data from a quadrant, and uses approximately 60 K words

of memory to histogram the pedestals and positron energy spectra for all 108 crystal channels. These data are stored, periodically retrieved by the PDP-11/44, analyzed, and the gain and pedestal results are downloaded into the LSI-11/23 microprocessors via the Dataway Access Port, permitting on-line monitoring of all crystal gains. Stabilization is also performed using a flasher and fiber optics system connected to all crystal channels. In processing stabilization triggers, the "Q-event" hardware is not used as Fig. 7 indicates.

IX. SUMMARY

In a complex facility designed to search for extremely rare processes among a background of copious accidental triggers, a trigger processor employing many kinds of technology has been developed to reduce the volume of data that must be analyzed after the experimental run is completed. A reduction from a maximum data rate of 1000 events per second, each containing more than 1000 words, to a rate of approximately one event per second, containing about 350 words, is achieved. Many additional functions are performed as well.

The system consists of high speed digital matrix logic, programmable hardware logic, and distributed microprocessor-based intelligence employed in a layered system. Most of the key design choices and the overall architecture have been described. Detailed articles on each of the important systems and modules will appear at a later time.

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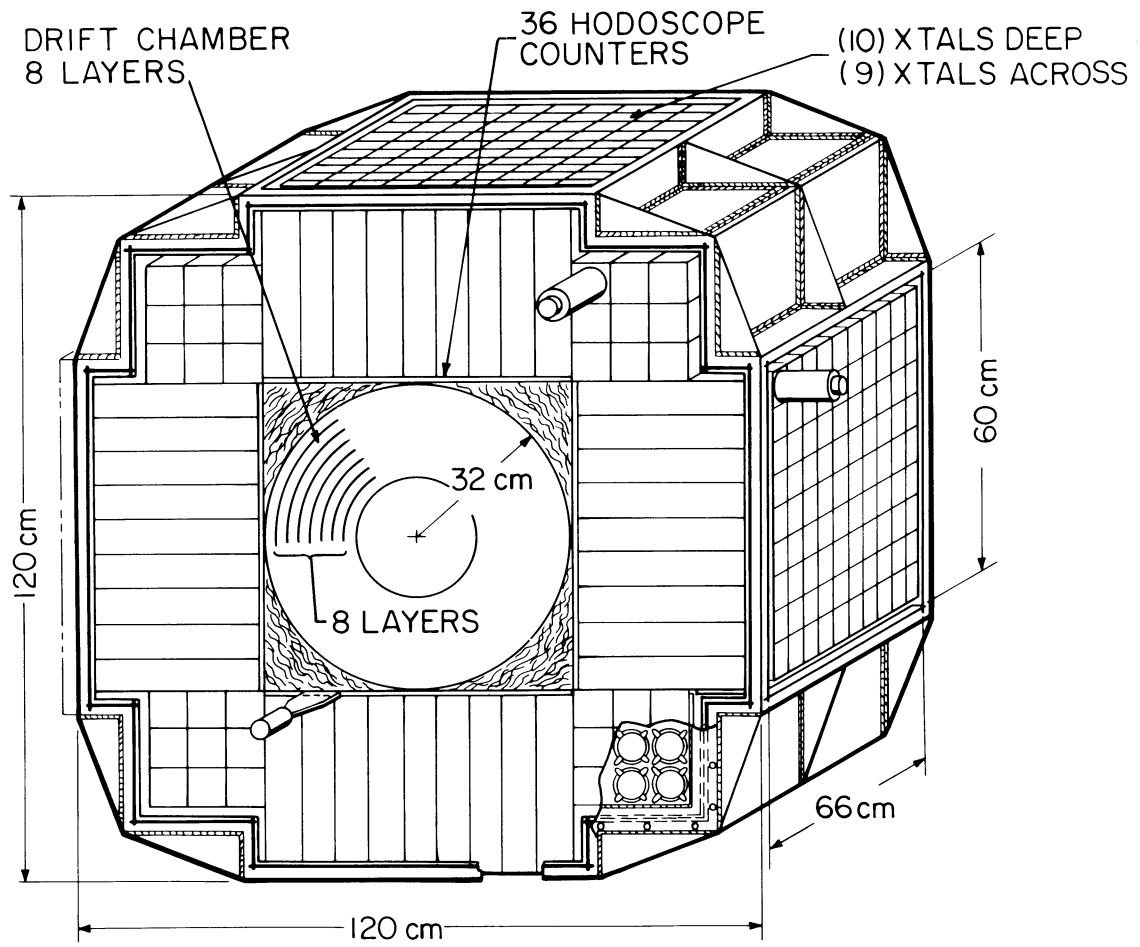


Fig. 1. Conceptual drawing of the Crystal Box detector to be used to search for several rare muon decays.

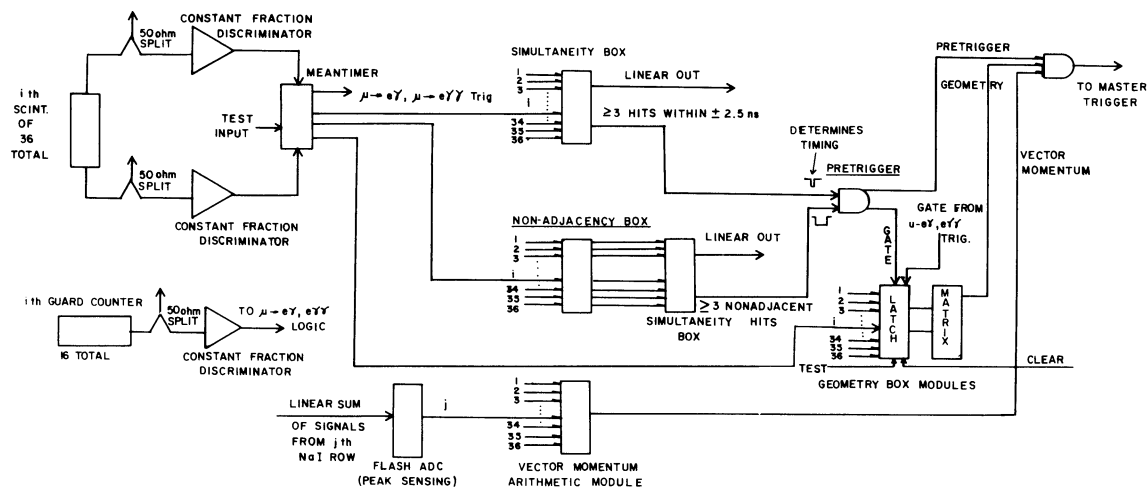


Fig. 2. Logic used to compose the primary master trigger for the $\mu + eee$ reaction. Signal processing circuits for the plastic scintillators are also shown.

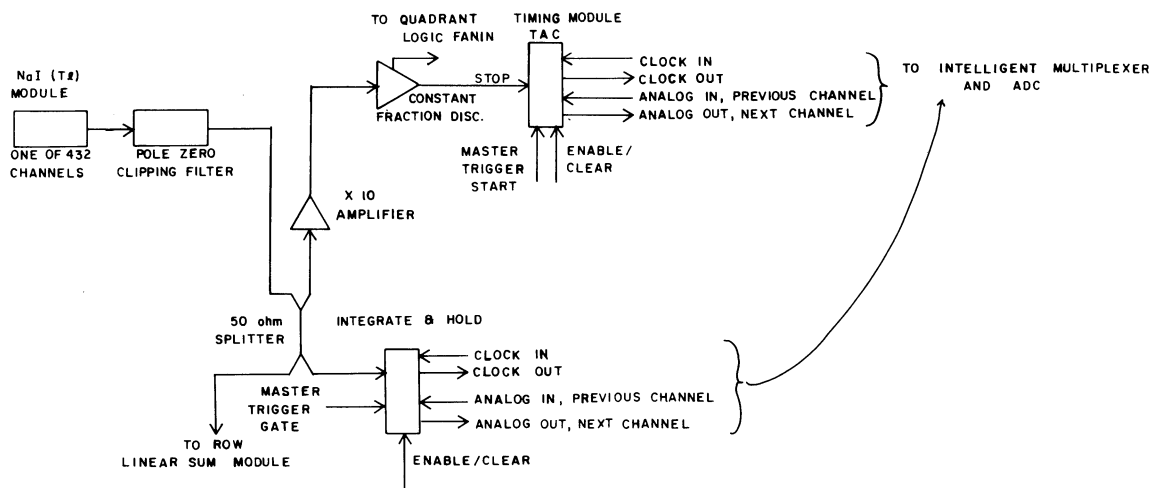


Fig. 3. Circuits to process the signals from the sodium iodide crystals for use in later stages of the trigger logic and data acquisition system.

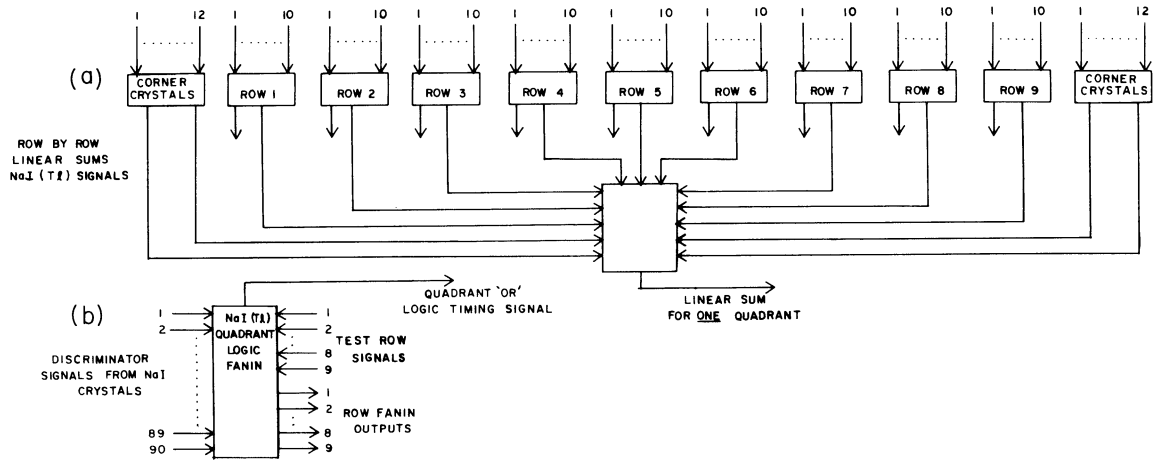


Fig. 4. Circuits to combine the signals from all the crystals in one quadrant of sodium iodide modules. (a) A linear sum is formed for use in the energy and momentum portions of the trigger. (b) Discriminated pulses are combined in a logic fanin for use in the time portion of the trigger logic.

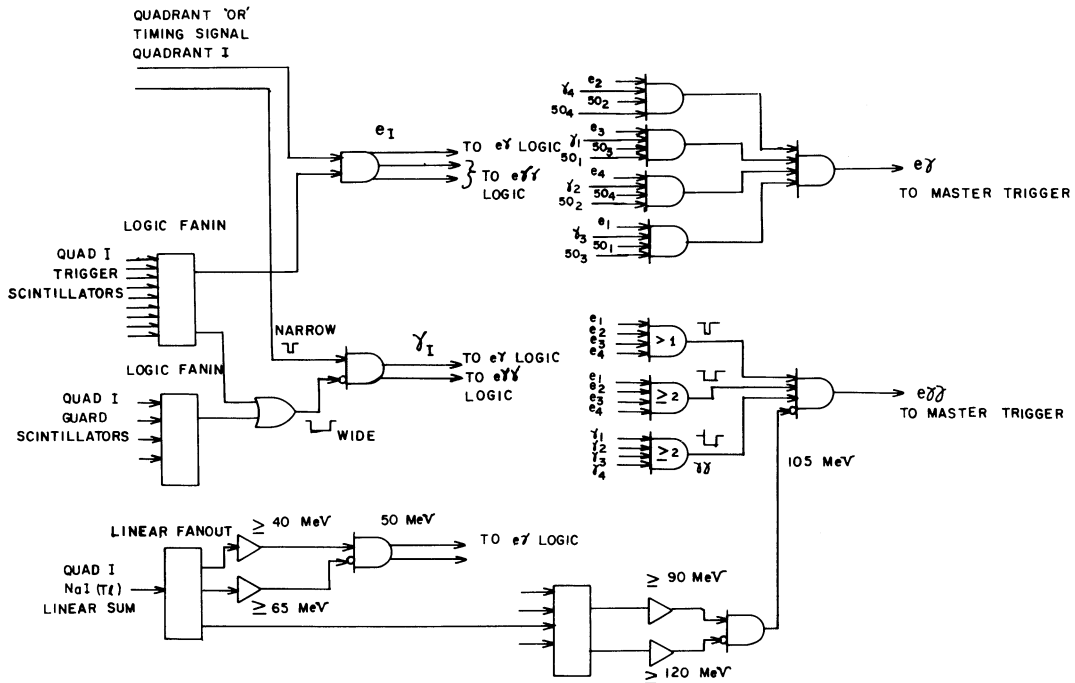


Fig. 5. Logic used to compose the primary master trigger for the $\mu + e\gamma$ and $\mu + e\gamma\gamma$ reactions.

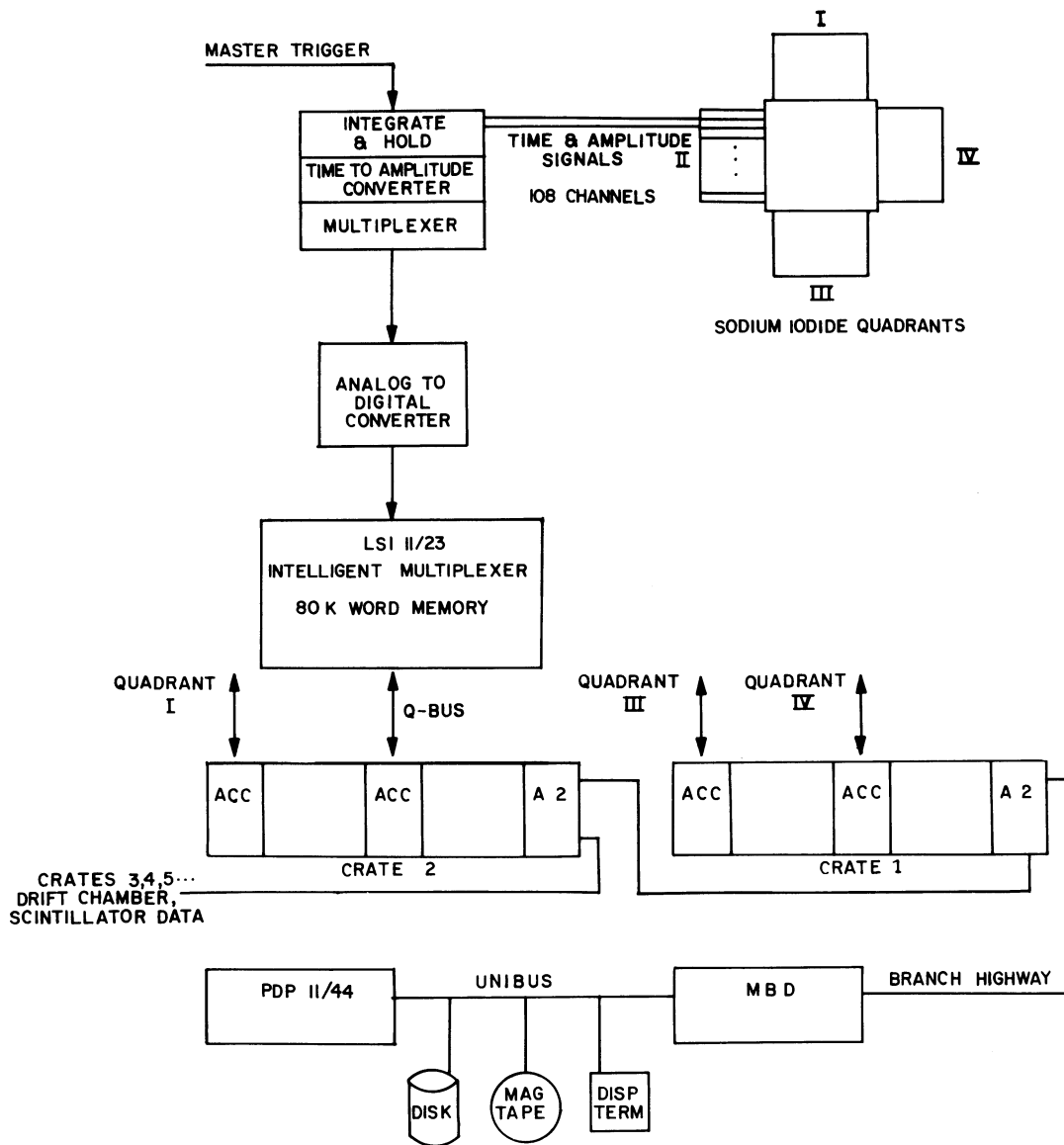


Fig. 6. Schematic representation of the secondary trigger processor. Signals from the sodium iodide modules in each quadrant are acquired through the Intelligent Multiplexers. Other portions of the experiment are acquired through the CAMAC Branch Highway. The MBD combines all portions of the data for transmission to the PDP-11/44.

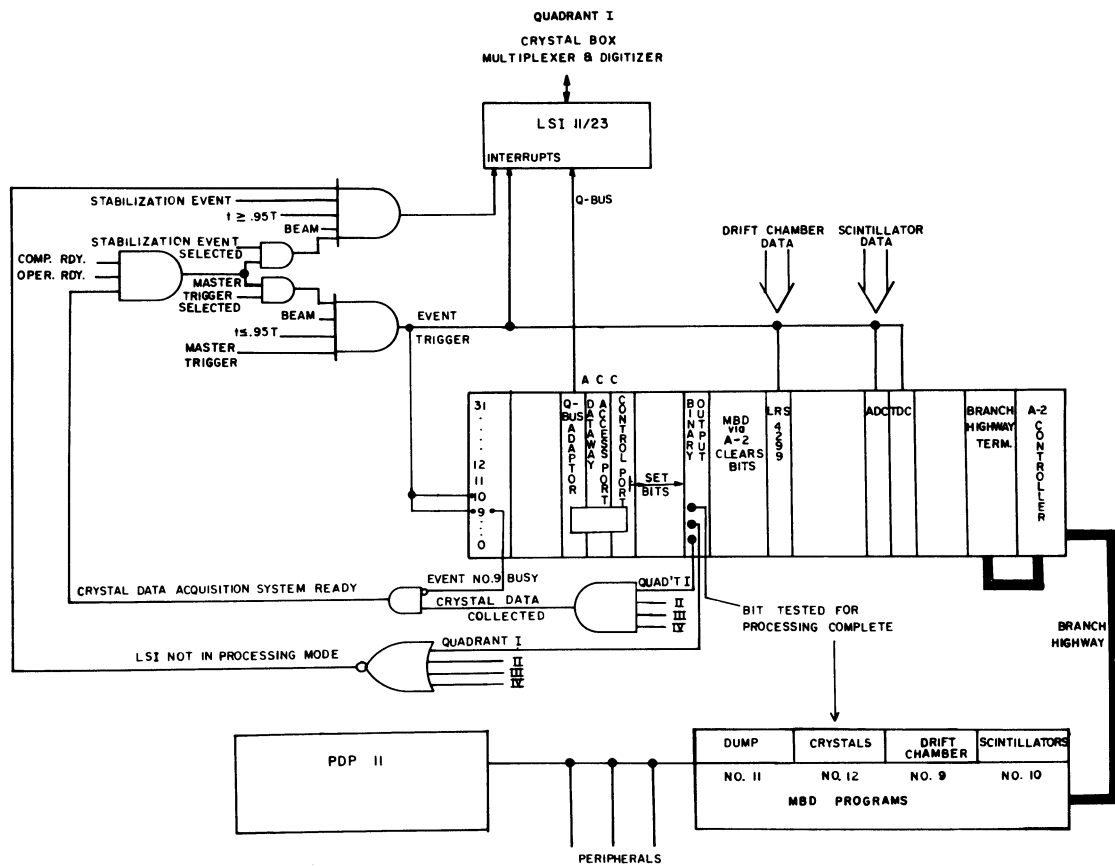


Fig. 7. Details of the secondary processor for one quadrant illustrating the interrupt handling and system synchronization.