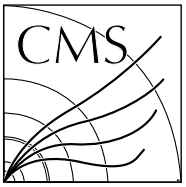
Available on CMS Information server

CMS NOTE 2005/008



The Compact Muon Solenoid Experiment

CMS Note

Mailing address: CMS CERN, CH-1211 GENEVA 23, Switzerland

April 26, 2005

Photodetector Power Supply System for the CMS Hadron Calorimeter

L. Dimitrov, B. Kunov, I. Vankov

Institute for Nuclear Research and Nuclear Energy, Sofia, Bulgaria

J.E. Elias, S. Sergueev[1], A. Ronzhin

Fermi National Accelerator Laboratory, USA

Abstract

The power supply system developed for the hybrid photodiodes used as photodetectors in the hadron calorimeter of the CMS experiment at LHC in CERN is described. The system includes about 500 channels, with two different voltage outputs on each channel, one high voltage output – up to 14000 V and one bias voltage output – up to 200 V. All output voltages are floating to facilitate single-point ground configuration. The system is computer controlled and ready to be interconnected with the CMS slow control facility.

Submitted to *Nuclear Instruments and Methods in Physics Research*

[1] *Fermilab and Joint Institute for Nuclear Research, Dubna, Russia*

1 Introduction

The Compact Muon Solenoid (CMS) is one of the new general purpose detectors now under construction for the new Large Hadron Collider (LHC) at CERN [1]. The CMS hadron calorimeter (HCAL) [2] is a sampling calorimeter with alternating layers of brass absorber and plastic scintillator tiles. Light collection is provided by wavelength shifting fibers embedded in groves cut in the tiles. The shifted light is coupled to clear optical links to the proximity focused hybrid photo diodes (HPDs) [3]. Photoelectrons emitted from the HPD photocathode (Figure 1) are accelerated by a strong electric field and stopped in a reverse biased PIN diode target. There, electron-hole pairs are produced, generating the electrical signal. The HCAL contains about 500 HPDs in total. For their normal operation two voltages are required, an accelerating voltage around 8 to 10 kV and a bias voltage about 80 to 100 V.

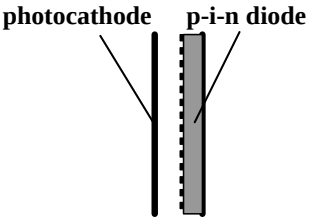


Figure 1. HPD structure.

2 Power Supply System

To provide the voltages required for the HCAL HPDs, a multichannel power supply system has been developed.

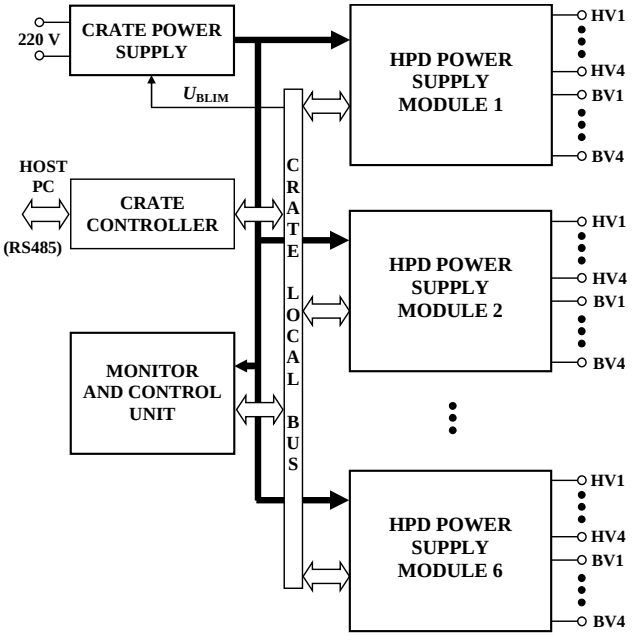


Figure 2. Block diagram of the HPD power supply crate.

Figure 3. HCAL HPD power supply crate.

The basic unit of the system is a 19" 6U Euro-standard crate. One crate (Figures 2 and 3) holds six HPD power supply modules, one crate controller module (HVC-02), one crate power supply module (CPS-01) and a monitor and control unit.

There are 4 high voltage and 4 bias voltage channels in each HPD power supply module. Four trimmer potentiometers are installed in the monitor and control unit (Figure 7 and 9) for presetting the upper limit values of the HPD output voltages (U_{HLIM}, U_{BLIM}) and currents (I_{HLIM}, I_{BLIM}). These limits are common to all high voltage or bias channels of the crate. The voltages corresponding to these limit values are distributed to the modules using 4 analog lines of the crate local bus. The monitor and control unit also contains 7 LEDs indicating the status of the crate.

The crate controller provides data and instruction communication between the host computer and the crate via an RS485 interface. The internal interface with the HPD power supply modules is realized by the crate local bus using a custom protocol [4].

3 HPD Power Supply Module

The block diagram of the HPD power supply module is shown in Figure 4. Each high voltage channel (HV CHANNEL) contains a specialized DC-DC converter, described in detail in [5]. The output voltage can be set from 0 to 14 kV. A linear stabilizer [6] is used in the bias voltage channels (BV CHANNEL). The output voltage can be set between 0 and 200 V.

In each power supply module, a local control block (LOCAL MODULE CONTROL) receives all output voltage set values from the crate local bus in serial mode sent by the crate controller. The local control block transfers

the set values to the digital-to-analog converters (DAC) that provide the reference voltages for each output. These data are stored only in the DAC of the corresponding channel.

All analog signals corresponding to the output voltage and load current values are fed consecutively through a multiplexer (MUX) to the analog-to-digital converter (ADC) in order to be read (in serial mode) by the local control block. These signals are also sent to the individual channel comparators (CMP), where they are compared with the corresponding voltage or current limit values received by the crate local bus. In case of overvoltage or overcurrent in any channel its comparator sends an alarm signal to the local control block, which immediately clears the DAC of the corresponding channel, dropping the output voltage to zero. An alarm signal is also sent to the crate controller.

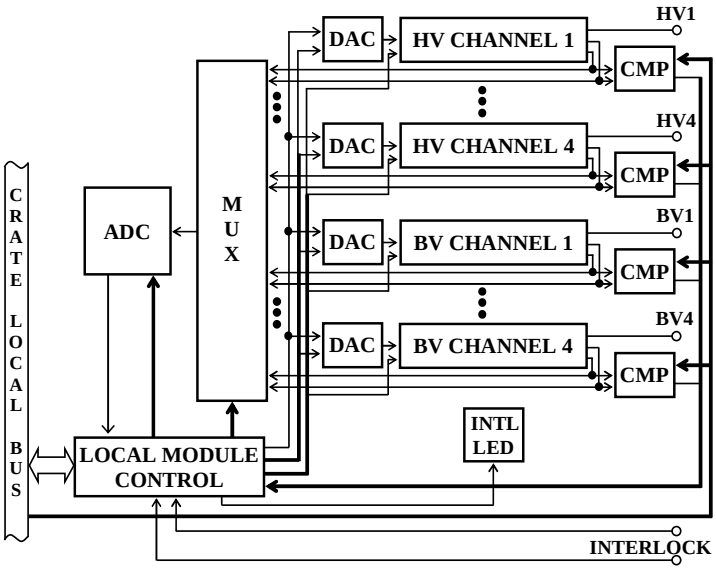


Figure 4. HPD power supply module block diagram.

The output high voltages of each module are fed by a 4-wire HV cable to one HCAL readout box containing 4 HPDs. In order to control the integrity of all these chains a 2-wire interlock line is used. At any interruption of the interlock circuits the local control block immediately disables all channels, activates the module front panel LED (INTL) and communicates the interlock error condition to the crate controller.

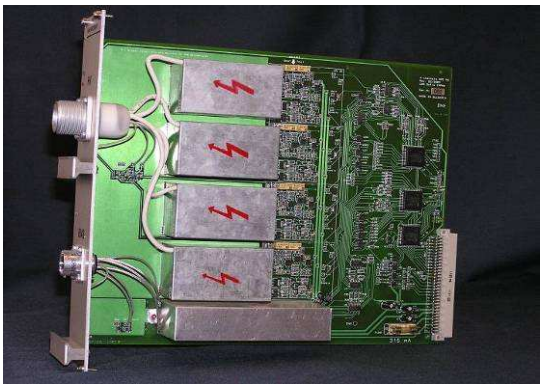


Figure 5. The HPD power supply module.

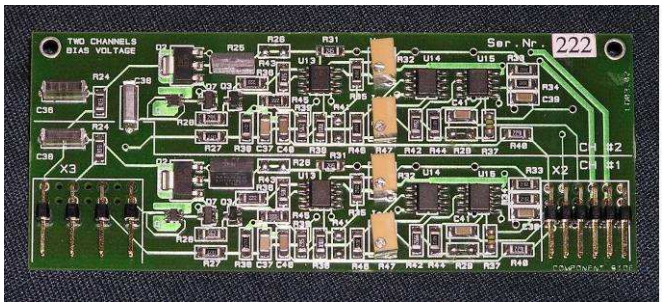


Figure 6. Two bias voltage channels PCB.

A photograph of an HPD power supply module is shown in Figure 5. The high voltage transformer and the Cockcroft-Walton circuit of each HV channel are housed in a small metal box and coated with silicon. Two bias voltage channels are located on a small printed board (Figure 6), and both boards of this type are covered by an aluminum shielding.

4 Crate Controller Module and the Monitor and Control Unit

The block diagram of the crate controller module and the monitor and control unit are shown in Figure 7. The crate controller receives the set values of the output voltages from a host computer by the RS485 interface. These data can be recorded in monitor and control unit local memory in order to be used as default values in future measurements. In the crate controller, a control logic block (CONTROL LOGIC) sends right set value data to the modules, checks the status of the HV channels, reads the value of the output voltages and currents and stores all these values in local memory (MEMORY). Thus, when the host computer addresses the crate controller, the requested information can be sent without delay.

Three principal lines are provided for data transfer – bus clock (CLK), bus data read (D-RD) and bus data write (D-WR). Four address lines are used by the crate controller to address the modules (MD[0..3]). One of them enables all modules for write operation. The other three address lines determine the local module geographical address in the crate. A separate line (ST) enables instruction transmission. In addition a bus reset line (RES) is provided to initialize all modules and channels.

The crate controller has a high priority external input (KILL). The response depends on the duration of this signal. If it is shorter than 40 us (so called "short KILL") only the CPU is reinitialized, but the output voltages are not affected. At the "long KILL" (longer than 40 us) the CPU is reinitialized and all output voltages are decreased to zero. In order to increase the reliability of the system, a special self-initializing function of the crate controller CPU (so called "watch dog") is foreseen.

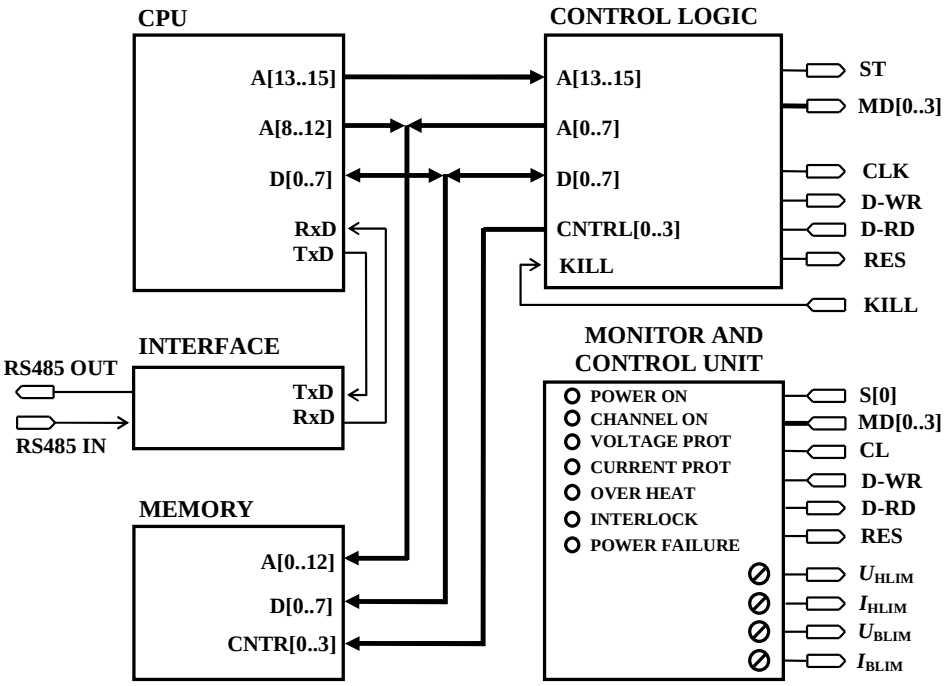


Figure 7. Crate controller module and monitor and control unit block diagram.

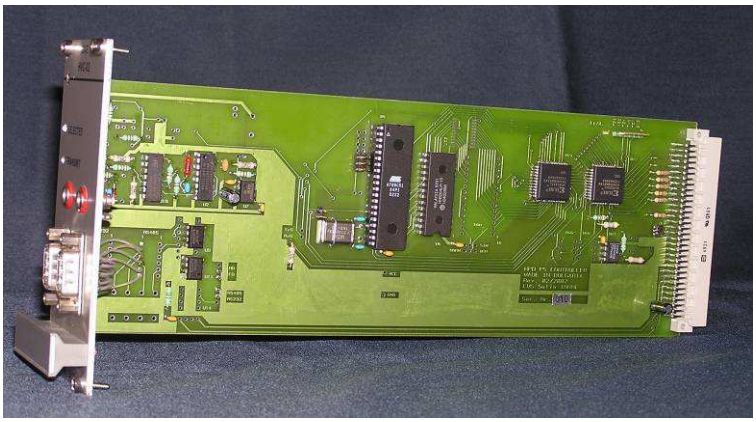


Figure 8. Crate controller module.

The crate controller CPU is an Atmel single-chip microcomputer (AT89C51). As mentioned above, the serial interface RS485 has been selected as the link between the crate controller and the host computer. Up to 128 crates of this type can be controlled by one computer.

The monitor and control unit displays the status of the system using 7 front panel LEDs:

- POWER ON (yellow) – the crate power is switched on;
- CHANNEL ON (green) – at least one output voltage is active;
- VOLTAGE PROT (red) – over-voltage detected in at least one channel;
- CURRENT PROT (red) – over-current detected in at least one channel;
- OVER HEAT (red) – the inside temperature of the crate is above 40 ^{0}C;
- INTERLOCK (red) – at least one interlock interruption is detected;
- POWER FAILURE (red) - at least one crate power supply voltage is out of range.

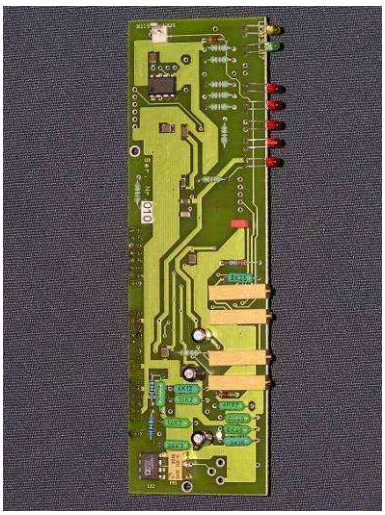


Figure 9. Monitor and control unit.

This status information is available to the host computer over the RS485 link. Many additional status parameters monitored by the crate controller are also accessible via the link. Software monitoring tools in the host computer can then be used to display this additional information (Figure 11 and 12):

- for each channel –
  - on/off,
  - ready – the output voltage is established,
  - up/down – transition processes in the output voltage,
  - voltage fault – the difference between the set value and the estab-

lished value of the output voltage is out of accepted range,
    - overvoltage,
    - overcurrent;
- for each module –
    - on/off,
    - overvoltage in any channel,
    - overcurrent in any channel,
    - voltage fault in any channel,
    - activated interlock,
- for each crate –
    - on/off,
    - overvoltage,
    - overcurrent,
    - voltage fault,
    - activated interlock in any module,
    - temperature, bus error, SROM error, and the three different initialization processes of the crate controller – short KILL, long KILL and watch dog.

The crate controller module and the monitor and control unit are shown in Figure 8 and 9.

5 Crate Power Supply Module

Figure 10. Crate power supply module.

The crate power supply module (Figure 10) produces the voltages required for normal operation of all other modules:

- +40 V for the high voltage DC-DC converters;
- A variable voltage about 10 V higher than the upper limit of the bias voltage (U_{BLIM}) for the bias voltage stabilizers;
- +5 V for the digital circuits;
- ±8 V for the analog circuits.

All voltages are read-out by the crate controller, which generates an alarm signal at each supply voltage variation outside of its admissible limits. The crate power supply voltages are displayed on the host computer main monitoring window (Figure 12).

6 Power Supply System Software

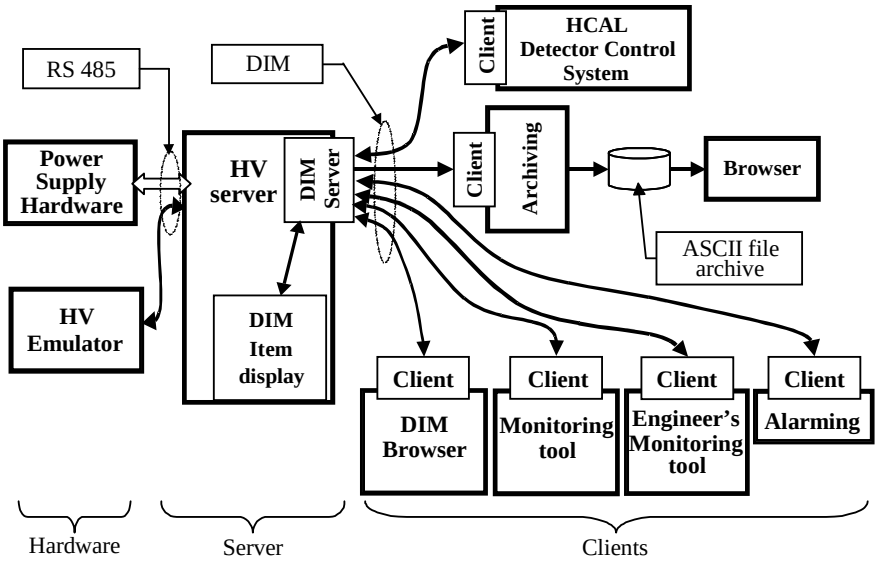


Figure 11. Block diagram of the software package.

A software package has been developed to provide control and monitoring functions for the HPD power supply system. This package is built according to the Client/ Server architecture. The Distributed Information Manager protocol (DIM) [7,8] is used for communications.

The overall scheme of program package is shown in Figure 11. The package contains set of programs as follows:

- server program managing up to 8 branches of RS485 serial links; the server includes –

- tools to set/retrieve the power supply system hardware configuration,
- tools to set and check serial ports,
- facilities to set DIM items names and alias names for a higher level monitoring system,
- publishing of the control information via DIM protocol,
- viewing of the published information for the debugging purposes,

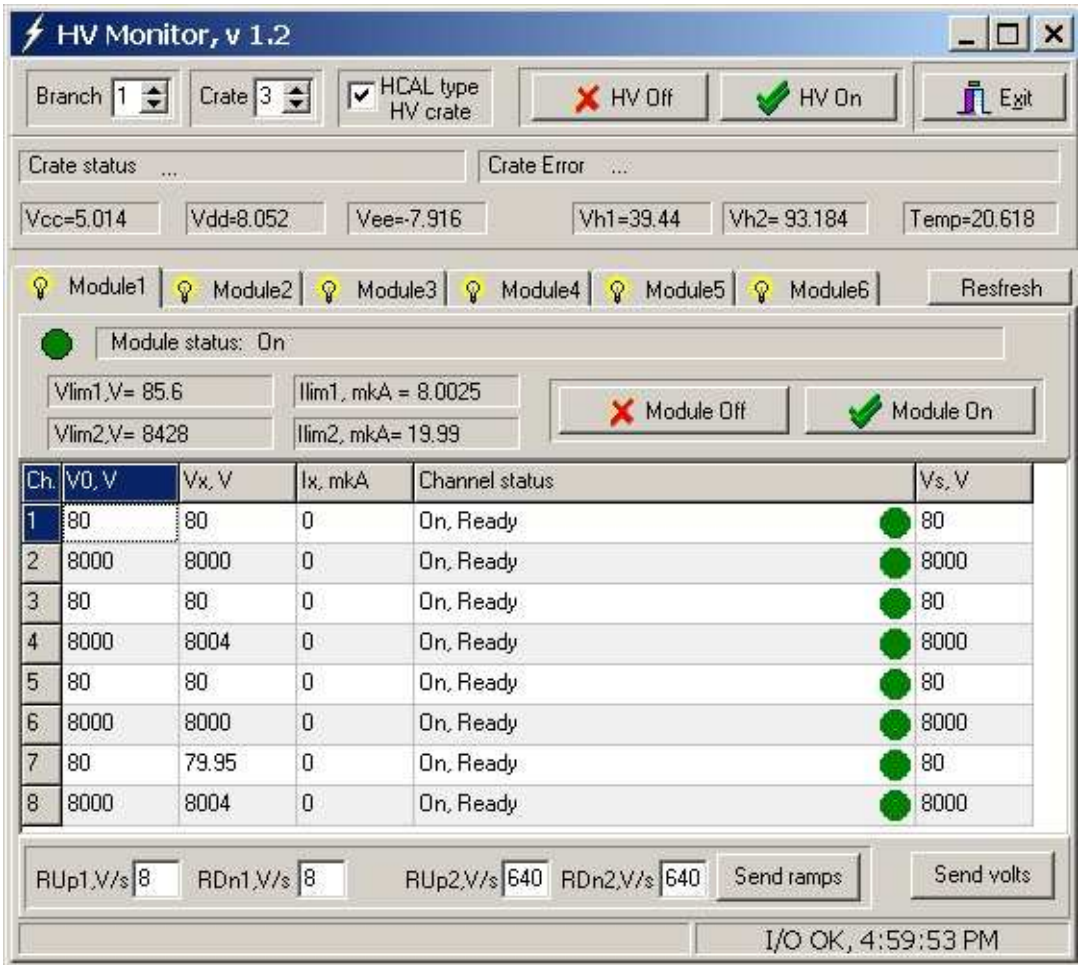


Figure 12. Main window of the monitoring tools.

- client program to control and monitor the power supply system (Figure 12);
- client alarming program to provide acoustic warning signal in case of any undesirable situation; this program also allows to switch off each HV channel in case when there is an overcurrent in the corresponding bias channel;
- client data recording tool to provide archiving of the voltage, current and status values; the information is archived in ASCII files accessible by standard MS Office tools or text editors;
- archive browser;
- debugging tools including –
  - hardware emulator which allows to check the RS485 serial link,
  - DIM information browser.

The server allows to connect as many clients as needed. Clients could work at different computers with Linux or Windows operating systems. The server works under any Windows OS of Windows NT clone.

In the future the HCAL photodetector's Power Supply system will be integrated in the HCAL Detector Control System (DCS) based on the PVSS II Supervisory Control and Data Acquisition system toolkit.

7 Basic Technical Parameters.

The basic technical parameters of the power supply system are shown in Table 1. The performance values marked with an asterisk have been confirmed by measurements.

Table 1 . Basic technical parameters of the system.

PARAMETER	HIGH VOLTAGE	BIAS VOLTAGE
Max. operating voltage, V	12000	200
Max. test voltage, V	14000	200
Voltage resolution step, V	4	0,05
Ramp rate, V/s	1 – 1000	0,1 – 100
Voltage ripple, mV p-p	< 50*	< 1*
Voltage monitoring inaccuracy, %	< 0,1*	< 0,1*
Long term instability, %	< 0,1*	< 0,1*
Max. output current, uA	40	10
Current monitoring inaccuracy, %	< 1*	< 1*
Special	Floating output	Floating output

8 Conclusions

A multichannel power supply system for the CMS HCAL photodetectors has been developed. A few crates of this system as well as the described program package have been used during several beam-tests of CMS HCAL prototypes in CERN. This experience has shown the power supply system to be stable and reliable. A convenient graphical user interface simplifies control and monitoring of the power supply system in stand-alone mode.

9 Acknowledgements

The authors are very grateful to all colleagues who took part in the discussions and tests of the system. Our special gratitude is extended to the FNAL specialists, developed the remaining part of the system – the Read-out Boxes with HPDs and the connections to them. We are particularly thankful to the technical coordinators of CMS HCAL Barrel and Endcap subsystems – Jim Freeman (FNAL-USA) and Victor Krishkin (IHEP-Protvino). They were the organizers of all relevant test beam experiments.

References

[1] CMS Collaboration. CMS Technical Proposal, CERN/LHCC 94-38, LHCC/ P1, 15 December 1994.
[2] CMS Collaboration. The Hadron Calorimeter Project Technical Design Report, CERN/LHCC 97-31, CMS TDR 2, 20 June 2003.
[3] P. Cushman, et al., Nucl. Instr. and Meth., vol. A387, 1997, p. 107.
[4] L. Dimitrov, B. Kunov, Proceedings of the 19th International Symposium on Nuclear Electronics and Computing – NEC'2003, 15-20 Sept. Varna, p. 113
[5] B. Kunov, et al., Proceedings of the 19th International Symposium on Nuclear Electronics and Computing – NEC'2003, 15-20 Sept. Varna, p. 187
[6] B. Kunov, et al., Proceedings of the 12th International Scientific and Applied Science Conference ELECTRONICS ET'2003, 24-27 Sept., Sozopol, book 2, p. 26.
[7] C. Gaspar, Distributed Information Management System. http://dim.web.cern.ch/dim/ .
[8] C. Gaspar, et al., DIM, a Portable, Light Weight Package for Information Publishing, Data Transfer and Inter-Process Communication (pdf). Presented at: International Conference on Computing in High Energy and Nuclear Physics, Padova, Italy, 1-11 February 2000 http://dim.web.cern.ch/dim/papers/CHEP/DIM.PDF.