The Manufacture of the CMS Tracker Front-End Driver.

J.A. Coughlan [1], R. Bainbridge [2], D. Ballard [1], I. Church [1], E. Corrin [2], C.P. Day [1], C. Foudas [2], E.J. Freeman [1], J. Fulcher [2], W.J.F. Gannon [1], G. Hall [2], R.N.J. Halsall [1], G. Iles [2], J. Leaver [2], M. Noy [2], M. Pearson [1], M. Raymond [2], I. Reid [3], G. Rogers [1], J. Salisbury [1], S. Taghavi [1], I.R. Tomalin [1], O. Zorba [2]

[1] CCLRC Rutherford Appleton Laboratory, Oxfordshire, UK
[2] Imperial College, London, UK
[3]Brunel University, London, UK

j.coughlan@rl.ac.uk

Abstract

The Front-End Driver (FED) is a 9U 400mm VME64x card designed for reading out the CMS silicon tracker. The FED was designed to maximise the number of channels that could be processed on a single 9U board and has a mixture of optical, analogue (96 ADC channels) and digital, Field Programmable Gate Array (FPGA), components. Nevertheless, a total of 440 FED boards are required to readout the entire tracker. Nearly 20 full-scale prototype 9U FED boards have been produced to date. This paper concentrates on the issues of the large-scale manufacture and assembly of PCBs. It also discusses the issues of production testing of such large and complex electronic cards.

I. INTRODUCTION

The off-detector readout system for the CMS silicon micro-strip tracker comprises of 440 9Ux440mm VME64x Front-End Driver (FED) boards. Each FED receives heavily multiplexed data from 96 analogue optical fibres, corresponding to 25,000 silicon strips. A description of the FED has been provided in a previous paper [1].

The FED was designed to maximise the number of channels that could be processed on a single 9U board. It digitises the converted optical data in 96 independent ADC channels. The digitised data is then processed in over 30 FPGAs (Xilinx Virtex II™), which extract clusters of hits and thereby substantially reduce the volume of data, which is passed to the central DAQ. At projected CMS trigger rates, the total input data rate on each FED will be approximately 3 Gbytes/s. After zero suppression this is reduced to 200 Mbytes/s on average.

The FED is double-sided in order to accommodate the high density of components with half of the analogue section on the secondary side (Figure 1). In addition to the large, 9U, board size the FED has a number of challenging specifications for large quantity manufacture. The total number of components is approximately 6,000, connected by almost 25,000 tracks, with the highest component density in the analogue section of the board (Figure 2). The majority of the passives have 0402 footprints. There are nearly 40 Ball Grid Array (BGA) devices per board with the larger FPGAs having 676 pins on a 1mm pitch. The boards have 14 layers, including 6 for power and ground. The impedance of both single and differential tracks is controlled. The signal interconnection scheme has been kept as simple as possible, with point to point links, to ease layout and routing.

The interconnections between all the digital devices can be verified with JTAG™ Boundary Scan [2]. This is complemented by DACs on each analogue channel, which permit on board testing of the analogue section without the necessity for optical input data.

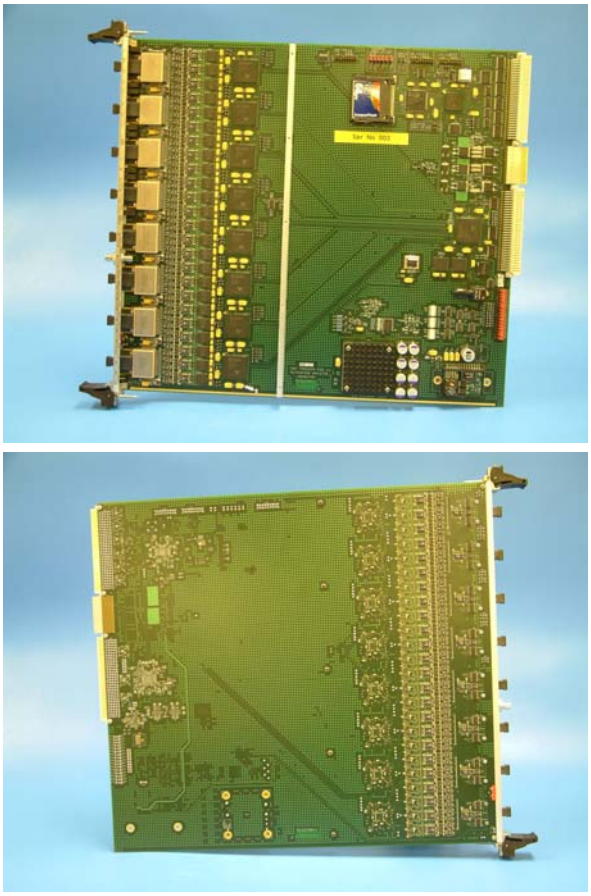

Figure 1: The FEDv1 board primary and secondary sides.

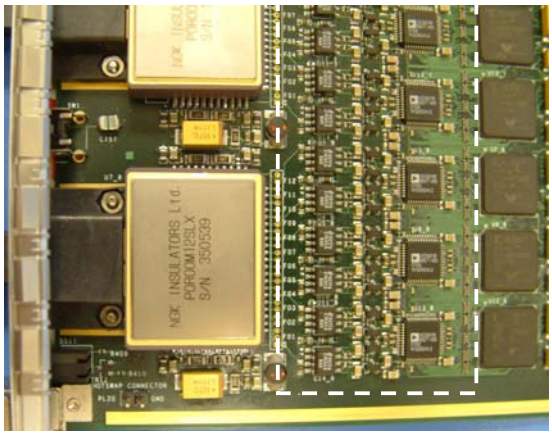

Figure 2: Close-up of part of the FED. The analogue components, indicated by dotted region, are repeated on the secondary side.

Approximately 20 FEDs have been manufactured to date. The first 5 boards were assembled successfully by a company specialising in small quantity prototype cards. However, a subsequent manufacturing batch of 6 boards failed due to poor BGA assembly. The original cause is believed to be due to chemical contamination of the bare PCBs, which had been provided by another firm. However the quality controls in the manufacturing process were not adequate to prevent a number of faulty boards being produced before the faults were detected. Attempts to rework the faulty BGAs were not successful.

Later productions were carried out successfully using one of the candidate companies [3] for the large-scale manufacture, which took responsibility for both PCB manufacture and board assembly. Extensive quality controls were employed during this production run including Automatic Optical Inspection (AOI), X-Ray inspection of BGAs and post-assembly Flying Probe board tests. Boundary Scan and custom VME crate tests were subsequently carried out at RAL. This process is described in the following sections.

The production run of 500 boards is foreseen to take place over a 12 month period beginning in the summer of 2005. A test plan for the large-scale manufacture is now being drawn up. A key objective is to identify and fix as large a fraction of the manufacturing faults as possible during assembly. In order to achieve this, the Boundary Scan and VME single board tests are being adapted, so that they can be performed at the assembly plant by the companies' own test operatives

II. Assembly Process

The major steps in the assembly process, together with the associated quality control procedures, are listed in Table 1. A typical surface mount assembly line is shown in Figure 3.

Due to the size and the technology on the FED boards a support frame was built to ensure that the board and components were not under any stresses during the manufacturing processes. Care was also taken in board handling by using individual Electrostatic Discharge (ESD) transport boxes.

Table 1: Assembly Process

Assembly procedures	**Quality Controls**
Secondary side	
Machine print	Paste Height check
Pick and Place machine assembly	
Re-flow	1st off AOI inspection
Primary side	
Machine print	Paste Height check
Pick and Place machine assembly	BGA placement check with Ersascope™
Re-flow	1st off AOI inspection
	Standard AOI inspection
	Surface Mount manual inspection
	X-Ray inspection of BGAs Ersascope inspection of BGAs
Fitting of 'Press Fit' connectors	
Conventional assembly	Conventional inspection
	Flying Probe test
	Final inspection

Figure 3: Example of a surface mount assembly line (courtesy DDi Technologies Limited).

A populated scrap board, from the earlier failed batch, was supplied to the assembly company, which allowed a detailed profile of the re-flow oven temperatures to be obtained for both sides of the board. Thermocouples were attached at several points on the board (including under the BGAs) and the temperatures in the various zones of the ovens measured and optimised (Figure 4).

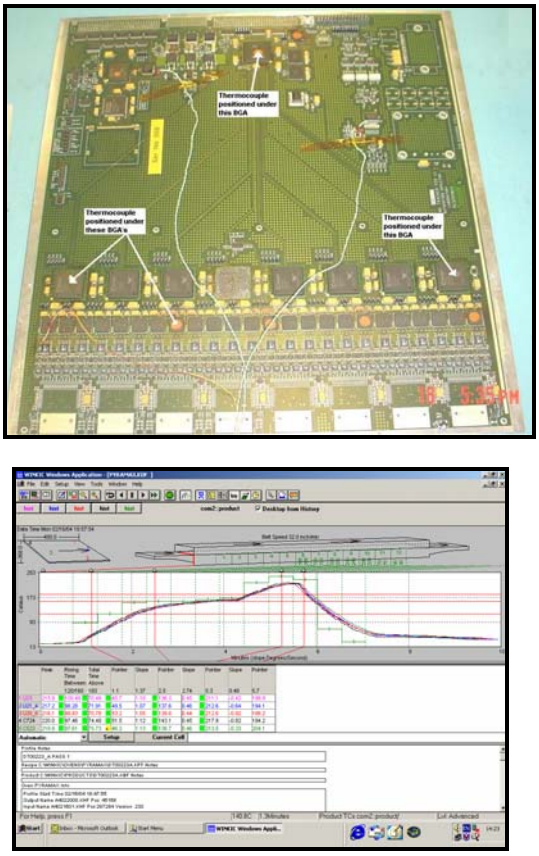

Figure 4: FED scrap board fitted with thermocouples and results from the re-flow oven profiling (courtesy DDi Technologies Limited).

The fabrication data for PCB manufacture and assembly is supplied in Valor™ ODB++ format, which is the de-facto industry standard for the exchange of electronic design information [4]. This has the advantage that only one self contained and complete electronic file needs to be sent to the manufacturer. The information in this file is also used to program the AOI and Flying Probe test equipment.

After surface mount assembly each board is examined with an AOI machine using a series of downward looking cameras. To generate an AOI program a "gold" board is scanned to teach the machine the image data. This is then merged with the information from the ODB++ files. The AOI will detect almost all the component misplacements, incorrect part numbers, poor solder joints and solder bridges which are visually accessible (Figure 5). As the process is automated it can achieve a vastly higher checking rate (100 components per minute) and repeatability level than manual inspection could provide.

Quality control of BGA assembly is carried out on a sample of boards. On the FED boards the BGAs are all located on the primary side. The correct placement of BGAs is checked using 3D X-Ray inspection (Figure 6). The quality of the solder ball re-flow is verified using endoscopic inspection tools such as Ersascope™ [5].

A final check of a sample of fully assembled boards is performed with a fixture-less Flying Probe tester (Takaya 9400). This machine is also programmed with ODB++ and can verify surface accessible connections and component values.

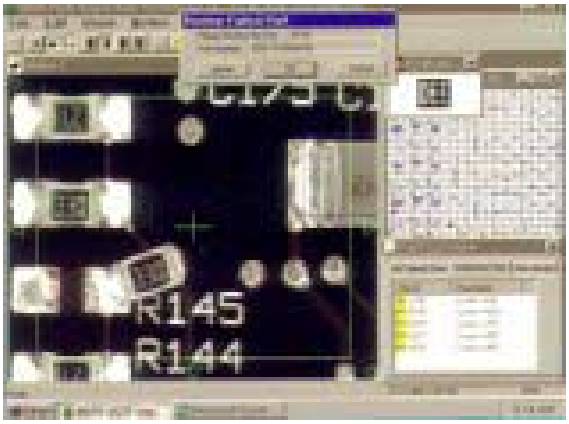

Figure 5: Example (not from a FED) of component misplacement detected by AOI (courtesy DDi Technologies Limited).

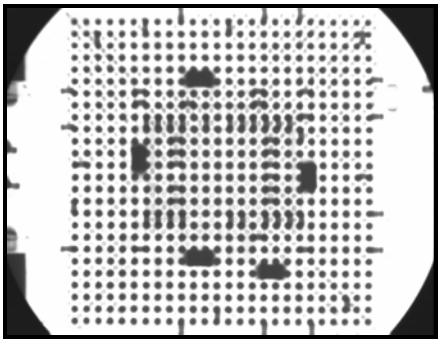

Figure 6: Example from FED of an X-ray image of a good BGA. The dark objects are de-coupling capacitors fitted on the secondary board side (courtesy DDi Technologies Limited).

III. MANUFACTURING ISSUES

The dominant cost of the FED board resides in the larger components; FPGAs and Opto-Rx modules. Given the high number of channels per board it is essential that the acceptance rate for assembled boards be as close to 100% as possible. From previous experience with this and other projects, when serious board failures occur it is often difficult to isolate the cause between the PCB manufacture and the assembly process.

In order to mitigate this risk, the production run of 500 FEDs will be carried out under a "one stop shop" contract, whereby a single company will be responsible for all stages of the production process, namely:

- PCB manufacture
- component procurement (excluding custom parts provided by CERN)
- assembly
- Boundary Scan and standalone board tests (section IV).

All the nets on each bare PCB are tested with flying probe-type test systems. Measurements of the track impedances are also taken.

Following detailed discussions with experts from the manufacturers it was decided to use an Electroless Nickel / Immersion Gold metal surface finish. This provides the best properties in terms of flatness of solder level for BGAs on large boards and long term solder joint reliability based on accumulated field experience.

In mid-2006 the EU is planning to introduce legislation to eliminate the use of Lead (and other heavy metals) in the electronics industry. This would necessitate the use of alternative solder fluxes to the standard Lead/Tin mixtures. Information on the reliability and lifetime of potential substitutes is limited. A further consequence may be the need to switch to new epoxy-glass laminates, which can withstand the associated higher soldering temperatures. For all these reasons it is planned for the FED production to be completed before the new directives are enforced.

IV. Post-Assembly Testing

In order to fully commission several hundred large and complex boards in an acceptable time-scale it is essential to identify and fix as many of the minor manufacturing faults as possible before the board leaves the assembly plant.

The FED has been designed with the needs of testing in mind. All the digital devices on board are located on JTAG chains. A Boundary Scan test permits all digital connections on the board to be verified. In addition, custom loop-back cards permit signals on the VME connectors to be checked (Figure 7).

Figure 7: Boundary Scan crate and loop back cards.

Following the delivery of assembled boards, engineers at RAL will carry out the final commissioning tests with multiple FEDs in crates and with optical inputs operating at full speed data rates.

In order to verify the analogue section of the board each ADC channel has an associated DAC to permit the injection of a slow signal without the need for external optical inputs. The Opto-Rx modules are fully tested by their manufacturer before delivery.

A test suite running under Linux using LabView™ and custom C++ libraries has been developed. This software is designed for single board tests to be carried out by operatives at the assembly plant. These tests also require the FPGAs to be programmed and the data readout via the VME bus.

V. Future Plans

Several FED boards are now in routine use by CMS groups in tracker assembly centres and in test beams at CERN. All of these boards passed full Boundary Scan tests, showing there have been no errors on any BGAs, and are fully operational on all 96 ADC channels.

An EU-wide tender is now in progress to select a manufacturer for the final production of over 500 boards, including spares. The manufacture of about 20 pre-production boards FEDv2 is foreseen for the end of 2004. The full production is planned to commence in mid-2005 and to be spread over 12 months. This schedule will permit the delivery and commissioning of the full complement of fully tested FEDs at CMS well in advance of the tracker detector installation.

VI. Acknowledgements

The authors would like to thank Steve Giffen and Jason Gross (DDi Technologies Ltd) for their kind permission to reproduce photographs and helpful discussions on board assembly procedures and Richard Matson (CCLRC) for his assistance in the JTAG Boundary Scan testing of the FED. The authors also wish to acknowledge the continued support of PPARC.

VII. References

[1] J. A. Coughlan et. al., "The CMS Tracker Front-End Driver.", *Ninth Workshop on Electronics for LHC Experiments*, CERN-2003-006.

[2] C.M. Maunder and R.E. Tulloss, *"The Test Access Port and Boundary-Scan Architecture",* IEEE Computer Society Press, Los Alamitos CA, 1990.

[3] DDi Technologies Limited, *www.eu.ddiglobal.com*

[4] ODB++, *http://www.valor.com/*

[5] ERSA GmbH, *http://www.ersa.de/de/index.html*