Tests of the boards generating the CMS ECAL Trigger Primitives: from the On-Detector electronics to the Off-Detector electronics system

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Abstract

The trigger architecture of the CMS electromagnetic calorimeter is physically organized in two sub-systems: the On-Detector front-end electronics and the Off-Detector electronics sub-system located in the electronics cavern. The trigger primitives of the electromagnetic Level-1 trigger are partially generated by the Front-End boards and completed by the Trigger Concentrator Card belonging to the Off-detector sub-system. Both boards will be produced and tested in 2004 and 2005 for the barrel. This paper puts emphasis on the testing procedure applied to the two boards.

I. Introduction

The Compact Muon Solenoid (CMS) [1] is a general-purpose detector that will operate at the Large Hadron Collider (LHC). This proton-proton collider will reach an energy of 14 TeV in the centre of mass and a high luminosity of 10^{34} cm^{-2} s^{-1} with a bunch-crossing rate of 40 MHz. The CMS electromagnetic calorimeter (ECAL) is a high-resolution calorimeter made of 76832 lead tungstate ($PbWO_4$) crystals and optimized for the discovery of the Higgs boson in its two photons decay mode. With such a detector and the high luminosity expected at LHC, the trigger strategy is very important. The trigger primitives of the electromagnetic calorimeter are basic quantities allowing the identification of electromagnetic showers by the Level-1 calorimeter trigger. They are generated by two different sub-systems located on the On-Detector electronics and the Off-Detector electronics. The On-Detector electronics is composed of radiation resistant circuits located just behind the $PbWO_4$ crystals and the trigger primitives are generated by the Front-End (FE) boards. The trigger primitives are then completed by a dedicated 9U VME board called Trigger Concentrator Card (TCC) belonging to the Off-Detector sub-systems located in the electronics cavern. The two sub-systems are connected by 80 m serial optical links working at 800 Mbits/s. 3072 Front-End boards and 108 TCC boards are necessary to manage the trigger flow of the whole calorimeter.

In 2004, the industrial production of FE boards started and 80 boards per week are expected to be tested. Such a production requires rigorous testing procedures especially for boards located inside the detector where no maintenance is possible. Concerning the Trigger Concentrator Cards, a first prototype of the TCC has been produced and the very first board of the industrial production is expected at the end of 2004.

This paper is organized as follows: in section 2, the ECAL Trigger Primitives are described. In section 3, the Front-End board is presented putting emphasis on the test procedure applied to the boards. Section 4 is dedicated to the Trigger Concentrator Card. Few details on the design of the board are given and the tests realized on the prototype are described. Finally, the test bench that will be used to validate the production will be presented.

II. The Trigger Primitives of the Electromagnetic Calorimeter

A. Level-1 Trigger and Trigger Primitives

The CMS Level-1 trigger [2] reduces the initial 40 MHz bunch crossing rate below 100 kHz by analysing coarsely segmented data from the electromagnetic and hadronic calorimeters and the muon detector systems. The High Level Trigger performs a further data rate reduction in order to reach the final 100 Hz target. The Level-1 calorimeter trigger is able to define up to 4 isolated or non-isolated electromagnetic objects (electron or photon), 4 taus jets, 4 central or forward jets, the total transverse energy and the missing transverse energy. In order to introduce the trigger primitive concept, let us focus on the electron/photon Level-1 trigger algorithm as it is displayed on figure 1.

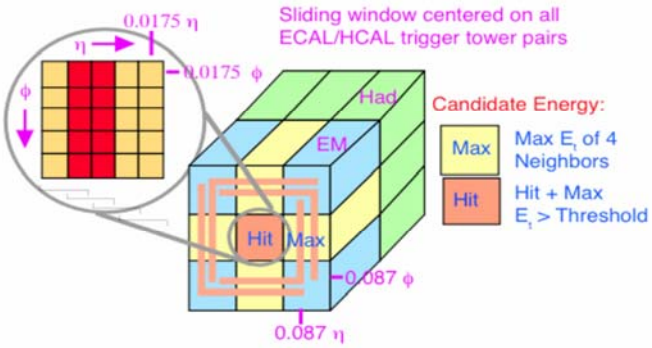

Figure 1: Principle of the Level-1 electron/photon trigger algorithm.

The algorithm uses a 3×3 trigger tower sliding window. A trigger tower in the ECAL barrel is made up of 5×5 $PbWO_4$ crystals, following the HCAL segmentation ($\Delta\eta \times \Delta\phi$ = 0.087×0.087), whereas in the end-cap, the size of the trigger tower varies with the pseudorapidity in order to follow

approximately a projective geometry. The transverse energy of an electron/photon candidate is defined by the transverse energy deposit in the central tower of the sliding window summed with the largest deposit in one of its 4 neighbour towers adjacent by side (see figure 1). Electromagnetic showers being characterized by a compact lateral extension, only candidates with a central tower containing 2 adjacent strips with a significant fraction of the tower energy (typically 90%) are kept (5 crystals in ϕ are called a strip). This criterion characterized by 1 bit is called the Fine Grain (FG) veto bit. Moreover, the associated HCAL energy contribution is required to be below a threshold (typically 5%). Non-isolated electron/photon candidates require passing the previous criteria. In addition, the isolated candidates must have a quiet neighbourhood characterized by at least five adjacent trigger towers among the 8 nearest ones with their transverse energy below a threshold [2]. One can easily identify two basic components in the algorithm described above: the measurement of the transverse energy of a trigger tower, and the determination of the ECAL fine grain veto bit. There is a third component, fundamental and implicit in the algorithm: when the energies of two trigger towers are summed, implicitly it is admitted that the energy of each tower corresponds to the same bunch crossing (same event). Indeed, since the signal coming from each crystal extends over several bunch crossings, one of the first tasks to be achieved is to assign a precise bunch crossing to detector pulses. These 3 components: 1) the E_T of a trigger tower, 2) the fine gain veto bit and 3) the bunch crossing assignment, constitute the ECAL Trigger Primitives.

B. The ECAL Trigger Primitives Path

The generation of The ECAL trigger Primitives is obtained with 2 CMS electronics sub-system (see figure 2).

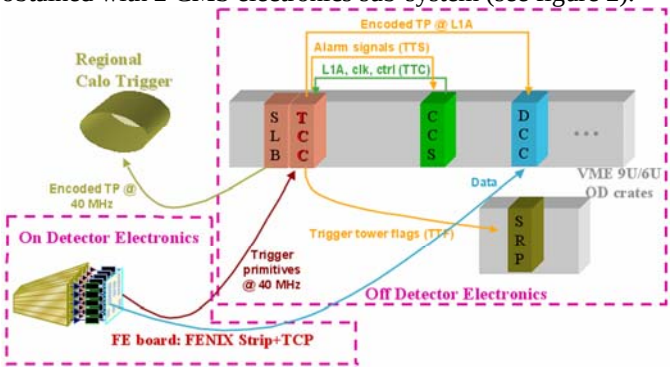

Figure 2: The trigger primitives path from the On-detector electronics to the Off -detector electronics system

The ECAL trigger Primitives are first partially generated by the Front-End board. In the barrel, the readout structure corresponds to the trigger tower structure. Therefore, a Front-End board manages a whole trigger tower (25 crystals). The evaluation of the transverse energy, fine grain veto bit and bunch crossing assignment is performed by radiation-hard ASICs called FENIX configured in strip mode and TCP mode (see for example [3] for more details). The almost complete Trigger Primitives are then sent to the Off-Detector [4] electronics subsystem housed in the underground electronics room. Both systems communicate through 80 meters optical links operating at 800 Mbits/s. The Trigger Concentrator Card, a 9U VME module, receives the Trigger Primitives (TPs) and encodes them using a non-linear scale for the transverse energy. The TPs are finally sent to the regional trigger through the SLB board, a mezzanine card sitting on the TCC and providing the channels time alignment. In the End-Caps, the scenario is slightly changed since the readout structure does not match the trigger structure. Indeed, several Front-End boards are needed to form a single trigger tower. Therefore, each Front-End board computes 5 partial sums of 5 crystals called pseudo-strips and sends them to the Trigger Concentrator Card that completes the Trigger Primitives calculations before sending them to the regional trigger.

III. THE FRONT-END BOARD

A. Description

A FE board reads out 25 crystals by gathering the digital data (16 bits at 40 MHz per channel) coming from 5 Very Front End boards. These 25 crystals correspond to a complete trigger tower in the barrel. In the End-Caps, the 5×5 read-out crystals are called supercrystals and are divided into pseudo-strips made up of 5 crystals with a variable shape. The End-Cap trigger tower is composed of several pseudo-strips and extends over several supercrystals and thus several Front-End boards. The main functions of the Front-End board are:

- To receive the signals from 5 Very Front-End boards and to store the data during the Level-1 trigger latency (3.2 μs maximum).
- To perform the Trigger Primitives calculation and to send the TPs to the Trigger Concentrator Card at 40 MHz after conversion to serial optical signal via a GOH (GOL Opto Hybrid, see previous section).
- To format and send the data (via a GOH) to the Data Concentrator Card (DCC) for the DAQ system when it receives a Level-1 trigger accept signal.

The outputs of each Front-End board then correspond to 1 optical link toward the DCC (DAQ path) and respectively 1 or 5 optical links for the barrel Front-Ends and the End-Caps Front-Ends toward the TCC (Trigger path).

B. XFEST: the eXtended Front-End System Test

In 2004-2005, 2448 Front-End boards will be produced for the Barrel. In 2006, there will be 624 boards for the End-Caps. XFEST, acronym for eXtended Front-End System Test, is a test bench designed to control the FE boards production after a burn-in phase. 80 boards per week have to be tested.

XFEST is designed to perform tests that can last several hours. Considering the very large number of possible input patterns (25×16 bits), it is not possible to cover the whole phase-space in a realistic time. Therefore, one has to choose input patterns as close as what will be encountered in the experiment. Besides, in order not to spend too much time, XFEST is designed to inject the same patterns to several FE boards at the same time. Therefore, the basic idea of XFEST

is to inject realistic patterns in several FE boards in parallel and to compare their outputs to the ones of a reference FE board. The figure 3 displays a schematic view of the XFEST system.

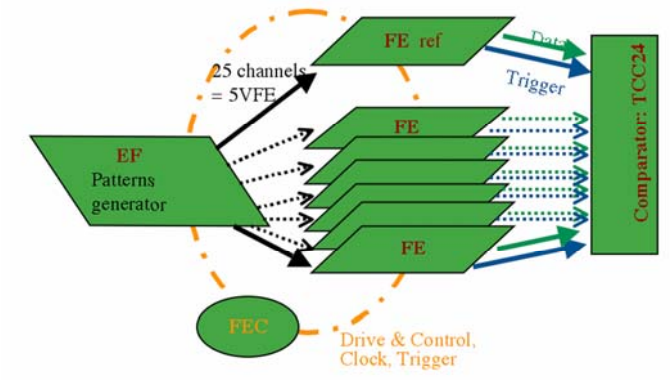

Figure 3: XFEST test bench

There are 3 main components: the pattern generator used to inject the signals to the FE boards, the motherboard distributing the signals (input patterns, control etc…) and the comparator.

1) The pattern generator

A FE board has 25 inputs coming from the VFE boards. As a pattern generator a FE board is used, but configured such as its 25 inputs are used as outputs. This FE board working in reverse mode is logically called EF. More precisely, the EF board is a prototype of the FE board equipped with FPGAs. The FPGAs have been reconfigured in order to emulate VFE patterns. A VFE modelling is shown in the figure 4.

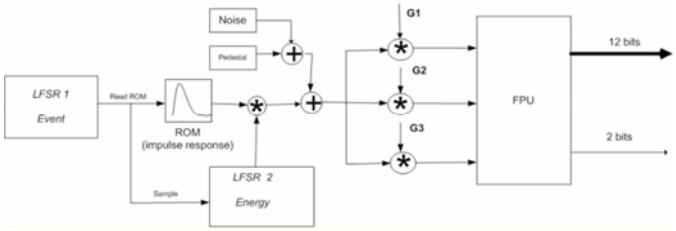

Figure 4: Modelling of signals from VFE

The EF generates pulse signals with a variable amplitude (a sequence of 40 bits LFSR is used) and a (pseudo-)random noise. The multi gain pre-amplifier is emulated with its 3 gains and its 3 pedestals. The shape of the signal is loaded in a ROM. Pile-up events can be simulated by superimposing 2 signals.

2) The XFEST motherboard

The main purpose of the XFEST motherboard is to distribute the same signals produced by the EF board to several FE boards. It also supplies the electric power. The principle of XFEST relies on the comparison of the FE's outputs assuming that all receive the same inputs. Therefore, the motherboard has been designed with a particular care to warrant the quality of the signal for all FE boards along the signal bus: long traces with characteristic impedance, large room between traces to avoid cross talk etc. A prototype has been realized connecting the EF board to 2 FE boards. The Figure 5 shows a picture of the prototype equipped with the EF board, the 2 locations for the FEs being empty.

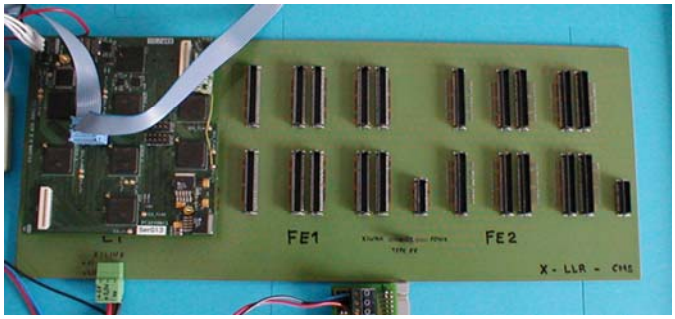

Figure 5: The XFEST motherboard prototype equipped with the pattern generator board (EF).

The size of this prototype is 36×14 cm and the PCB belongs to class 6 with 24 layers. Its thickness is 4.8 mm. The final version of the motherboard will interconnect the EF board with 4 FEs. The size of the PCB is 48×35 cm and its thickness is the same as the prototype one. There are about 400 traces with a 50 Ω characteristic impedance.

3) The comparator

In the CMS experiment, the data stream and the trigger stream from the Front-End boards will be sent respectively to the DCC and TCC boards. In XFEST, a prototype of the TCC board is used to collect both streams. This prototype – a 6U VME board called TCC24 - has 24 input channels and is described more extensively in the section IV-B. It allows the test of 12 FE boards simultaneously (12×2 streams = 24 channels). Its FPGAs (XILINX virtex2) have been reprogrammed to manage both streams in a comparator mode. Therefore, both streams of the FE boards connected to the TCC24 are compared to the ones of the reference FE. In case of discrepancy of one or several boards with respect to the reference, error signals are sent to the VME bus that are caught by the computer controlling the test bench. In addition, the patterns received from the FE boards are stored in the TCC24 buffers (within a small depth) allowing eventually off-line analysis.

XFEST is controlled by a single Linux-computer in charge of:

- The VME controller based on the standard tools of CMS experiment: XDAQ/HAL [5],
- The graphical user interface,
- The driving of FE boards and the configuration of the EF one.

The XFEST control program is implemented as a lightweight standalone daemon that communicates with the outer world using the XMLRPC protocol. The end-user interacts with the daemon using a client program, such as the XFEST graphical client program implemented as a PHP Web site and controlled by a simple Web browser. Finally, in order to test a large number of boards, the possibility to use 3 motherboards for the final production test is considered, allowing the test of 12 FE boards at the same time.

IV. THE TRIGGER CONCENTRATOR CARD

A. Description

The Trigger Concentrator Card (TCC) collects the serial optical data (i.e. almost Trigger Primitives) transmitted from 68 Front-End boards in the barrel (a whole SuperModule) and, in the End-Caps, up to 48 pseudo-strips (5 pseudo-strips per End-Cap FE boards). The TCC is a 9U VME module belonging to the Off-Detector electronics system, which functions are:

- Opto-electronic conversion and deserialization of the input data streams.
- Finalization of the Trigger Primitives by encoding it with a non-linear scale for the total transverse energy (a look-up table is used). The building of the trigger towers from the pseudo-strips and the calculation of the Trigger Primitives precede this step in the End-Caps.
- Time synchronization of the Trigger Primitives (TPs) thanks to the Synchronization and Link Board (SLB), a mezzanine card plugged in the TCC that plays the role of the interface between the Off-Detector system and the Regional Calorimeter Trigger (there are 9 SLBs per TCC barrel). After synchronization the TPs are sent to the Regional Calorimeter Trigger as a serial stream (by a copper link) at 1.2 Gbits/s.
- Storage of the TPs during the Level-1 trigger latency and their transmission once a Level-1 trigger acceptance signal is received.
- Computation of the Trigger Tower Flags (TTF): the trigger towers are classified into 3 categories depending on their transverse energy. The TTFs are sent via an optical link to the Selective Readout Processor (which flags the trigger towers that have to be readout by the DAQ) once a Level-1 trigger acceptance signal is received.

The TCC (barrel version) has 6 processing units (Xilinx virtex2 FPGA) connected to 68 deserializer-circuits (1 per input) with in-between, the SLB connectors. Therefore, the density of traces on the PCB is very high, and to limit the number of layers (10 are used) and so the cost, original solutions such as micro-vias (120 μm diameter drilled by laser connecting 2 layers) and BGA components have been employed. Moreover, the time budget allocated to the TCC on the trigger path is only 7 LHC clock units. This includes all steps from the opto-electronic conversion and deserialization of the input data to the delivery of the Trigger Primitives to SLB boards. Such constraints have major consequences on the design and technological choices. The most significant is certainly the choice of the deserializer circuits' -AGILENT HDMP 1034A- using the CIMT deserialization protocol [6] and having important needs in current. All these technological choices had to be validated on a prototype.

B. TCC24 the prototype

The TCC24 is a prototype corresponding basically to one third of a TCC barrel in terms of circuits: 24 input channels, 2 Xilinx FPGAs etc. However, the layout is as close as possible of final version even if the board is just a 6U VME module. A photo of the board is shown in figure 6 where the deserializer circuits can easily be seen on both sides (12 per side on the left part of the photo).

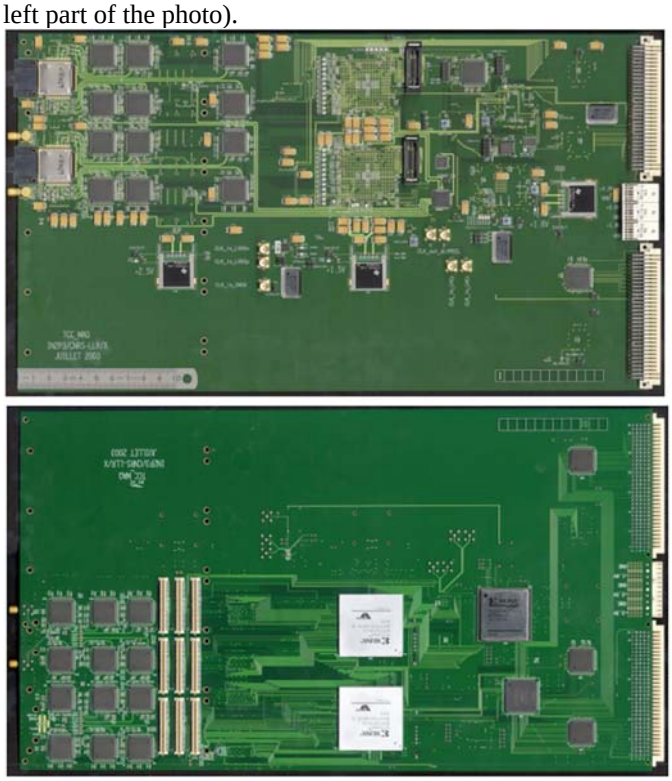

Figure 6: The 2 sides of the Trigger Concentrator Card prototype

The TCC24 has been extensively tested. The power consumption measurements are consistent with our expectations and the extrapolation to the final board gives a total power consumption of about 130W. The latency has been evaluated by injecting patterns in the TCC24 and measuring the delay in different part of the board. A digital oscilloscope with large bandwidth and active differential probe were used to perform such measurements. The measurements give less than 3 clock units spent in the deserialization process and a total of less than 6 clock units (below the time budget allocated to the TCC). The previous test needs a device able to inject patterns in the TCC24. This device is a 9U VME module called TCC-Tester and initially developed for the Test bench of the DCC board. Details can be found in [7]. The FPGAs of the TCC-Tester have been programmed in order to send continuously patterns (previously loaded in memories by VME accesses) to the TCC24 at 40 MHz. The TCC-Tester is able to emulate the Front-End interface with the TCC using 72 independent serial optical links working at 800 Mbits/s with the CIMT protocol as in the CMS experiment. This board has been used to perform Bit Error Rate (BER) measurements. The experimental set-up was the following: The TCC-Tester sent to the TCC24 deterministic patterns. The FPGAs of the TCC24 were doing the on-line comparison at 40 MHz between the received pattern and the expected one. In case of discrepancy, an error flag was sent to a logical analyser that counts the total number of errors. Several series of tests have

been performed giving consistent results. For example, one channel has been tested continuously during 145h and no error was found. Therefore, a lower limit on BER can be set to 3.10^{-15}. The potential influence of cross talk among channels on BER has been investigated by injecting in 18 channels (at the same time) known patterns. No error was found during 16h10' (duration of the test) setting a lower BER limit to 2.10^{-14}. Indirect measurements of BER using eye-diagram or jitter measurements approaches give consistent results.

C. Tests for the TCC boards production

The first TCC barrel version is expected in October 2004. A total of 42 boards will be produced and tested during the second half of 2005. Several kinds of tests are planned to control the production. The sequence of tests is the following:

1. When a board is received, JTAG tests are first performed allowing for boundary scan. This test rejects quickly defective boards.
2. Built-in self-tests are performed to check the quality of the firmware of each board. A pattern is auto-generated by the TCC itself (from its FPGAs) and treated by its firmware. The result (Trigger Primitives, Trigger Tower Flags etc) is compared internally to a reference output stored in one of the board's ROM.
3. Short tests lasting few seconds are performed to extensively control one channel from its optical input to the board outputs. The TCC Tester board injects data and the output patterns are compared to a detailed hardware simulation of the TCC based on the SystemC framework [8]. The acquisition is performed by a Logical Analyser (all TCC boards are equipped with Logical Analyser connectors) and a comparison bit to bit with the results of the simulation is performed.
4. Once a single channel is validated (previous test), long tests lasting several hours are performed to control all channels. It is not possible to use the same approach as in the previous test because of the huge amount of data that has to be injected and controlled (at 40 MHz). Therefore, tests based on channels comparison are performed following the same approach as the XFEST one. Here, the TCC Tester injects the same patterns in all channels of the TCC. The output patterns are then compared internally by the TCC processing units to the one corresponding to the reference channel. If a discrepancy is noticed, an error is sent to the VME bus that is caught by the computer controlling the test bench. In this mode, the TCC Tester generates pseudo-random patterns using LFSR.

A single computer running Linux controls the TCC test bench. Access to the VME uses the XDAQ/HAL interface [5]. The graphical user interface is based on the ROOT framework [9].

V. CONCLUSION

The two boards in charge of the generation of the ECAL Trigger Primitives, the Front-End (FE) board and the Trigger Concentrator Card (TCC), will be produced in the next months. First results on a TCC prototype have been shown validating the design of the final board. Test benches controlling the production of boards have been presented. They use similar approach and when possible even share the same hardware.

VI. REFERENCES

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