Optical Multiplexer Board for TileCal Data Redundancy.

J. Torres, J. Soret, V. González, E. Sanchis, J. Martos, J. A. Gómez, J. Castelo

Dept. Ingeniería Electrónica, Universidad de Valencia - ETSE
Dr. Moliner 50, 46100 Burjassot (Valencia), Spain
Jose.Torres@uv.es

Abstract

This work describes the present status and future evolution of the Optical Multiplexer Board (OMB) for the ATLAS Tile Calorimeter. The developments currently under execution include the adaptation and test of this card to TileCal needs and the design and implementation of the CRC (Cyclic Redundancy Codes) algorithm for ATLAS data.

The adaptation includes a new module with 4 inputs and 2 outputs which receive two fibers with same data from Front End Boards. The importance of this card is to decide what fiber has not transmission error and send it to Read Out Driver (ROD). Furthermore, it works like ROD Injector in order to test ROD MotherBoard.

I. Introduction

At the European Laboratory for Particle Physics (CERN) in Geneva, a new particle accelerator, the *Large Hadron Collider (LHC)* is presently being constructed. In the year 2008 beams of protons are expected to collide at a center of mass energy of 14 TeV.

In parallel to the accelerator, two general purpose detectors, *ATLAS* and *CMS*, are being developed to investigate proton-proton collisions in the new energy domain and to study fundamental questions of particle physics.

This new generation of detectors requires highly hardened electronics, able to deal with a huge amount of data in real time. The work we present here is included in the studies and development currently carried out at the University of Valencia for the Optical Multiplexer Board of the hadronic calorimeter TileCal of ATLAS.

II. TileCal System

TileCal is the hadronic calorimeter of the ATLAS experiment. It consists of 10000 channels to be read each 25 ns. Data gathered from these channels are digitized and transmitted to the Data Acquisition System (DAQ) [1] following the assertions of a three level trigger system.

In the acquisition chain, place is left for a module which has to perform pre-processing and gathering on data coming out after a good first level trigger before sending them to the second level. This module is called the Read Out Driver (ROD).

TileCal is a redundant data acquisition system. Two optical fibbers carry the same data from front-end electronics [2] to ROD. This is necessary because of radiation phenomena could cause malfunctions inside front-end electronics, and bit and burst errors over data ready to be transmitted to ROD card. Unfortunately, ROD card has only one input connector for each data, because the original design responds to initial specifications.

Our primary target is to improve error tolerance, designing a pre-ROD card, called Optical Multiplexed Board (OMB), able to analyze two fibers, both of then carrying the same data, to provide the correct one to the ROD input.

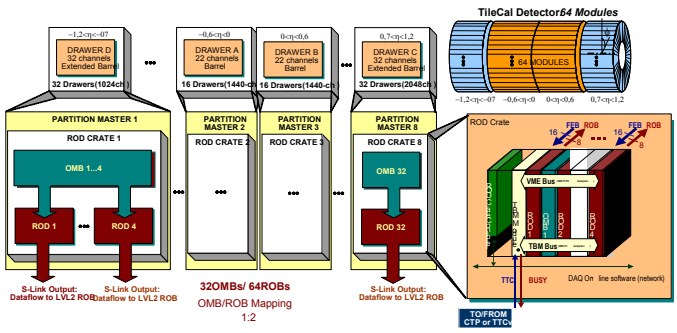

Figure 1: TileCal System Diagram.

The interest of this project was justified in February 2003, when a preliminary study appeared. This proposal shown a solution for OMB based on exhaustive on-line analysis of the data carried by both of the fibers, using FPGAs for implementation. This architecture was called as "MiniROD", because it follows a ROD-like design.

Universidad de Valencia – IFIC (Spain) team showed the greater interest to deal with this project, to make a first prototype to study technical viability. In particular, the main goals are:

- Fiberoptic switching to take advantage of redundancy.
- Obtain real (production) costs.
- Have a development platform (hw - sw).
- Try different alternatives for data error analysis (CRC, etc.).

A new functionality for OMB was proposed, it was suggested a function mode called "Data Injector Mode", to use the OMB like data pattern injector towards ROD for test and verification uses

This project started in October 2003. The construction of an OMB first prototype is finished.

III. Optical Multiplexer Board Description

Optical Multiplexer Board prototype has been designed to readout redundant output data from FEBs [3] and send correct data to RODs. The mother board prototype is a 6U VME64x slave module which has two channels. In addition, it works like ROD Injector in order to test ROD Motherboard.

The layout of the board is shown in Figure 2.

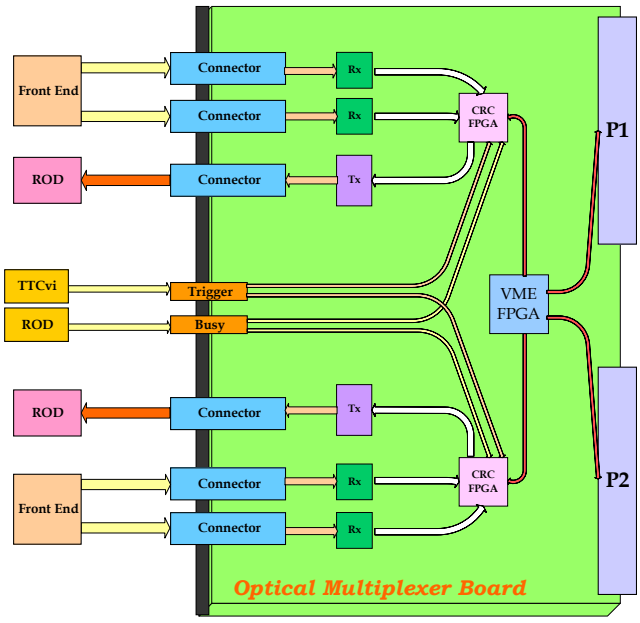

Figure 2: Optical Multiplexer Board Block Diagram.

The Optical Multiplexer Board includes four optical inputs connectors and two optical outputs connectors integrated in the PCB. The input channels are capable of reading 4x16 bits at 40 MHz and allow us to test different input technologies. The output will also run at 40 MHz with a data width of 16 bits [4].

On the board there are also four input G-Link chips, two output G-Link chips, two CRC FPGAs and one VME FPGA. These lasts are implemented on ALTERA devices. Furthermore, for Data Injector Mode, OMB has two more inputs. Trigger and Busy external signals are included in this prototype to send correctly internal data in order to test ROD functionality [5].

A short description of the main functions of the G-link and FPGA chips in the OMB board is given in Table 1.

Table 1: OMB principal components.

Component	Main Function	Chip
6 G-Link Chips	Deserialize the incoming data Serialize the output data	HDMP-1034 HDMP-1032
2 CRC FPGAs	Send correct data to ROD ROD Injector Data	CYCLONE EP1C12
1 VME FPGA	Interfaces OMB to VME	ACEX EP1K100

The main description for the OMB is:

A. Input Description:

Four optical fibers coming from the FEBs are the input to the OMB, and two optical fibers to the ROD are the output from the OMB.

The so-called G-link chip (HDMP-1034) is a deserializer chip and is used in the input stage of the OMB board. The serializer (HDMP-1032) is used in the output stage of the OMB board [6]. The HDMP-1032 transmitter and the HDMP-1034 receiver chips are used to build a high-speed data link for point-to-point communication. They are monolithic silicon bipolar chips.

Parallel data loaded into the transmitter chip is delivered to the receiver chip over an optical fiber, and is reconstructed into its original parallel form. The HDMP-1032/1034 chipset handles all the issues of link startup, maintenance and simple error detection. It transmits 16 bits of parallel data in dual-frame mode.

B. CRC FPGA Description:

Two CRC FPGA CYCLONE EP1C12 are used in the OMB board. The main reason for the choice these chips is the low cost of this FPGA. The incoming data from two different G-link receiver chips is routed to one CRC FPGA [7]. The different and redundant incoming data are analyzed and CRC FPGA decides which the correct data is. CRC FPGA routes the correct data to one G-link transmitter chip.

C. VME Interface of OMB:

The OMB module is considered a VME slave module. All actions and commands are controlled by the CPU of the crate and the communication follows the VME64 standard. The VME interface of the OMB is implemented in an ACEX EP1K100, the VME FPGA.

Both block transfer and read/write cycles are implemented as well as a broadcasting writing mode. The data bus is D32. The addressing is A32 for data transfer and A24 for CR/CSR.

The VME FPGA exchanges data between the VME CPU and two CRC FPGAs.

D. Data Distribution in OMB:

There are two different function modes in OMB, CRC process mode and ROD Injector Data mode. Figure 3 show how the distribution of the data is done in CRC process and Figure 4 show how the distribution of the data is done in ROD Injector Data. In ROD Data Injector mode receiver G-Links are not used.

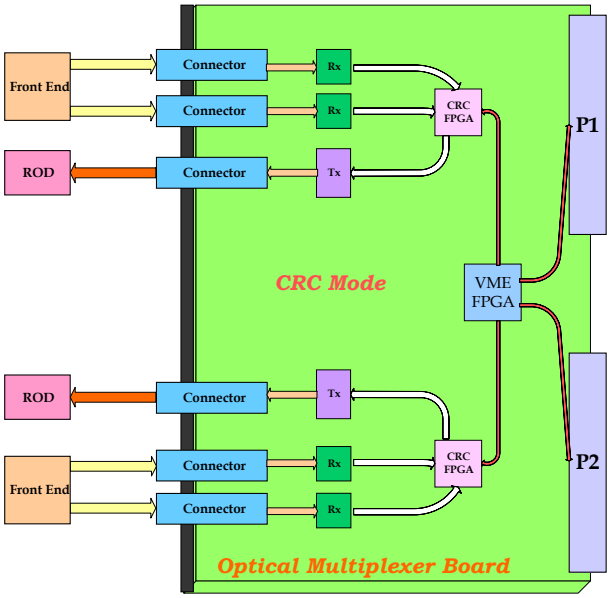

Figure 3: Data Distribution in CRC Mode.

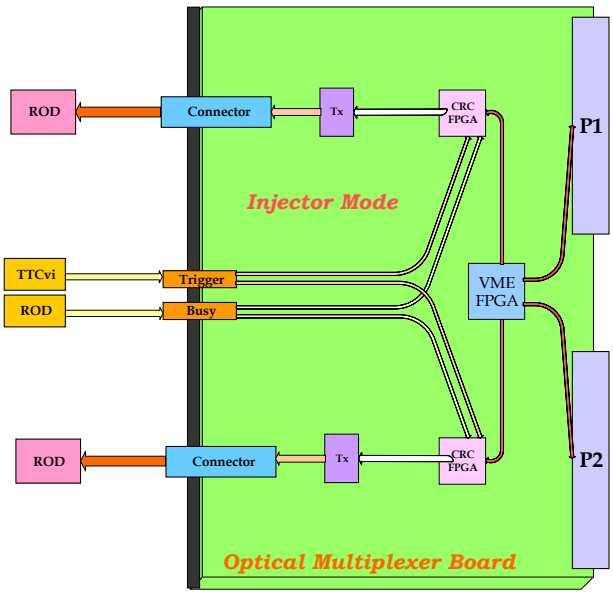

Figure 4: Data Distribution in Injector Mode.

E. Power Distribution in OMB:

There are two modes to generate main power supply (3.3V) in OMB board:

- Obtaining 3.3V from the VME back plane.
- Obtaining 5V from the VME back plane and converting that into 3.3V with a DC/DC converter (PT5801).

The +5V from the VME back plane is used by the trigger/busy logic and is used to obtain +2.5V necessary for VME FPGA. ADP3330-2.5 is the DC/DC converter used to obtain this voltage.

The +12V, -12V and -5V from the VME back plane is used by the trigger/busy logic too.

IV. Present Developments

At University of Valencia there are three development fronts undergoing.

The main is related with the tests and developments for the OMB board, the second deals with the software issues at the OMB board and the third goes towards the design and implementation of a 9U OMB final prototype.

Let's review now the current status on each of these directions.

A. *Tests and Developments for OMB:*

The tasks on the OMB board currently going on are of next kinds:

- Layout and routed board: This is already finished, next figure shows the PCB layout.

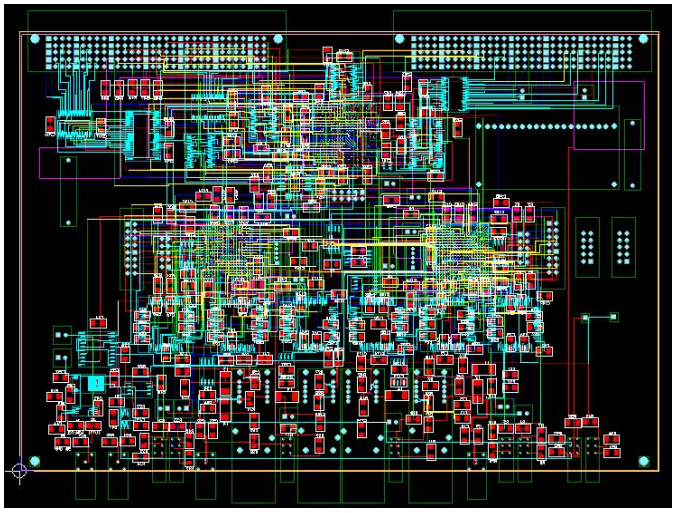

Figure 5: OMB Layout.

- OMB construction: This is already finished, next figure shows the OMB real board.

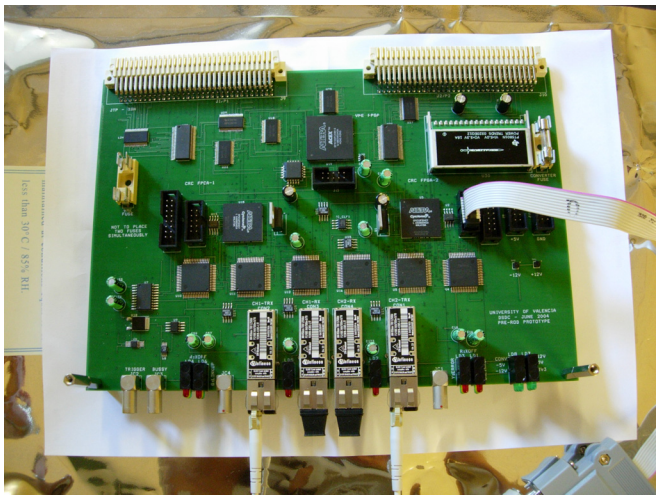

Figure 6: Optical Multiplexer Board.

- Test of the OMB components: Not yet finished.

B. *Software for OMB:*

Parallel to these activities we are also involved in the design and development the software included at FPGAs.

- CRC FPGAs: Going on. This work refers to the implementation of the algorithms to process incoming data.
- VME FPGA: We need to program this protocol to connect at ROD libraries.

C. *9U OMB Final:*

For the final OMB prototype we are currently designing a new PCB based on 9U VME 64x [8]. These will imply more channels per board and a TTC block. Our working block diagram for a final TileCal OMB prototype is shown in next figure.

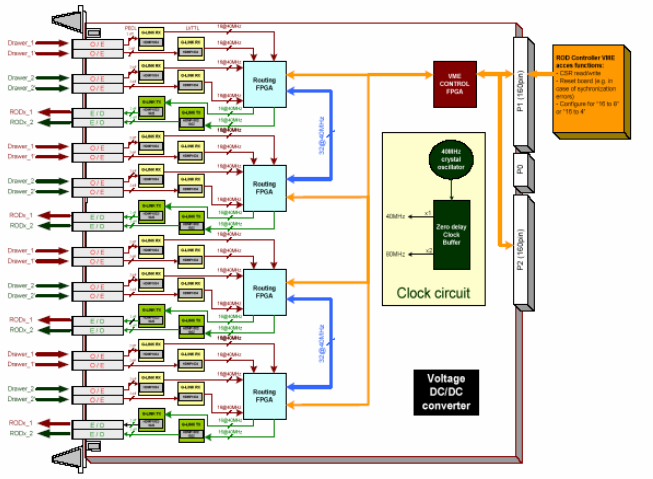

Figure 7: 9U Optical Multiplexer Board.

V. REFERENCES

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