Stand-alone Cosmic Ray Trigger Electronics for the ATLAS Tile Calorimeter

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Abstract

A 192-channel stand-alone trigger system has been developed for the ATLAS Tile Calorimeter (TileCal). It allows early commissioning of the calorimeter in the ATLAS underground experimental area using cosmic rays before the full ATLAS trigger system is available. Once the barrel calorimeter as assembled, it is desirable to test the operation of the calorimeter, associated readout electronics, and data acquisition system and to monitor the long-term stability of the entire TileCal detector system. A cosmic ray muon trigger in conjunction with laser, charge injection triggers, and cesium source scans test the full range of functions of the TileCal system.

The trigger system includes two 96-channel coincidence boards and two tower signal sorting modules, which are built on a single width VME 9Ux400mm cards and a 3-width 9Ux240mm VME transition module respectively. It is designed to trigger on cosmic ray muons traversing back-to-back towers in the calorimeter.

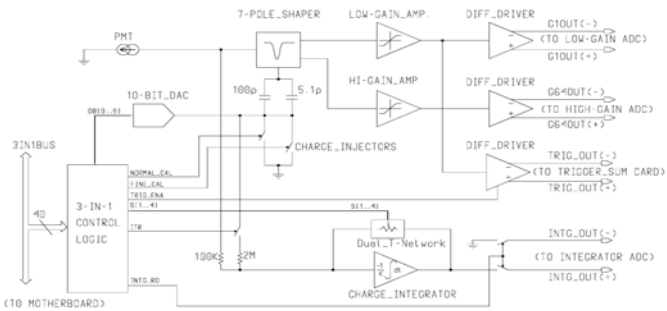
Each sorting module receives 96 channels of front-end differential signals via 80-meter cables from 48 top towers and 48 bottom towers of the TileCal. Based on the geometry of trigger tower, the signals are sorted by the passive sorting modules and are sent to the associated coincidence boards. A very low noise differential amplifier with limited bandwidth and a fast discriminator with programmable threshold are used for each input analog signal on the coincidence board. The entire digital logic system, including input pulse width stretching, reconfigurable two-fold coincidence matrix, tower signal scalars, trigger scaler, trigger pattern FIFOs, tower signal enable/disable functional circuits, threshold DAC settings, as well as VME interface logic, is implemented in one FPGA on board.

The system design and performance tests are given in this paper.

I. Overview of TileCal Electronics

A. TileCal Front-end Readout Electronics

The TileCal is composed of one barrel with 64 modules and two extended barrels with 64 modules each [1]. The system contains about 10,000-channels of readout electronics. The TileCal electronics is designed to measure signals from energy deposition in the calorimeter cells. The induced particle energy is in a range from about 20Mev to 1.3Tev. Each calorimeter cell uses a pair of photomultiplier tubes (PMT) to collect light signals from the TileCal scintillating tiles. At the low-energy end (20MeV), the PMT output charge is only few tens of femtocoulombs, while at the high-energy end (1.3Tev); it reaches up to as high as 800pC. A total readout dynamic range of 16-bit is needed. The complete front-end electronics for each PMT is built on a 7cm by 4.7cm PCB, the so called 3-in-1 card [2], which is mounted inside the PMT block [3]. A novel 7-pole shaper with a bi-gain readout method has been adopted. The block diagram of the 3-in-1 card and of high-gain and low-gain output waveforms are shown in Figure 1.



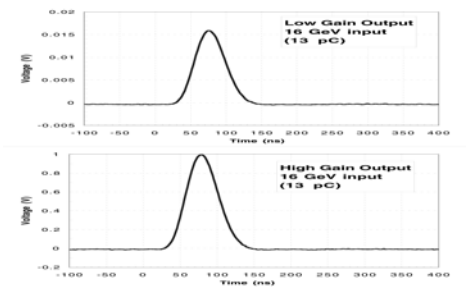


Figure 1. The functional diagram of the 3-in-1 card and the typical low-gain and high-gain output waveforms.

The 3-in1 card has three goals:

(1) Fast analog signal processing for the data acquisition system

Each 3-in-1 card receives a fast signal [5] from its associated PMT and shapes it by a 7-pole shaper to a Gaussian-like pulse with a 50ns full-width-at-half-maximum. In order to achieve 16-bit dynamic range, a bi-gain system with a high-gain to low-gain ratio of 64:1 is used. The high-gain channel handles input signal less than 12.5pC, which corresponds to particles with energy less than about 20Gev. Clamping amplifiers are used to prevent both channels from saturating when overdriven; otherwise, the system dead time could be significantly prolonged. The digitizer samples the signals at a rate of 40MSPS [6] for both gains. An event frame of 7 to 16 samples is collected from the high or low gain branch depending on the amplitude of the pulse. The phase of the digitizer clock can be adjusted in 100ps steps. Full luminosity ATLAS running will use 7-sample event frames, which corresponds to a 2-sample pedestal and 5-sample peak measurement. For the purpose of system calibration, two charge injection circuits with the combined dynamic range of 16-bits are also built on the board.

(2) Charge integrator for calibration and monitoring system

A programmable 6-gain charge integrator on the 3-in-1 card is employed to measure either the minimum-bias current during normal collision runs or a cesium source induced current during the source calibration. The integrator transforms a very small current into a measurable DC voltage which is digitized with a 12-bit ADC.

(3) Analog trigger outputs for trigger system

The 3-in-1 card low-gain channel supplies an additional pair of linear differential signals as the analog trigger outputs. It can be disabled by system commands in case of failure of the PMT or the front electronics.

B. Electronics inside of the electronics drawer

There are a total of 256 electronics drawers that contain the TileCal front-end electronics. Each electronics drawer is housed in the backbone girders of TileCal modules. Electronics inside each drawer is shown in Fig. 2.

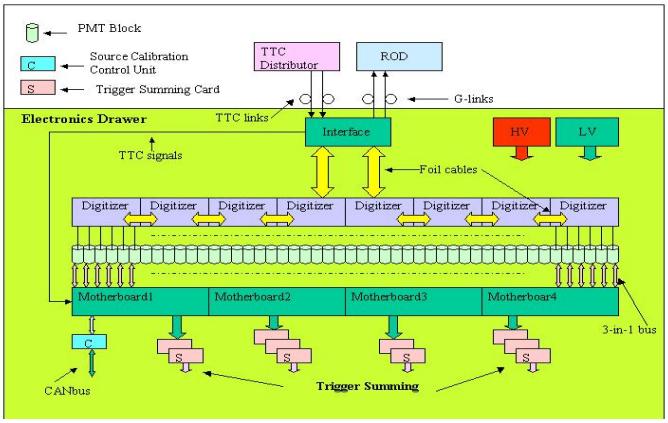


Figure 2. Electronics inside each electronics drawer.

The electronics drawer is equipped with following functional circuit boards:

- Up to 48 PMT blocks, each with one PMT and voltage divider, and one 3-in-1 card.
- 4 motherboards that provide services to the front-end electronics [7].
- 8 digitizer boards that digitize up to 96 channels of high-gain and low-gain signals from the 3-in-1 cards.
- One interface card [8] which provides a link between the electronics drawer and an off-detector readout driver module (ROD). The transmitting rate is 860Mbps. A redundant design is adopted to increase system reliability.
- 9 analog trigger adder boards that are plugged onto motherboards to generate TileCal tower 1 trigger signals for the off-detector LVL1 trigger electronics system [8].
- One integrator ADC card consisting of a microprocessor, CANBUS controller, and 12-bit ADC. The ADC card is plugged onto the motherboard. It selects and digitizes one of 48-channels of integrator outputs and sends its output data to the monitoring system via CANBUS.
- One set of high voltage distributors for the PMT voltage dividers.
- Low voltage power supplies mounted just outside the drawer for this electronics [9].

II. Cosmic Rays Trigger Electronics System Design

Figure 3 shows the pictures of the coincidence board and the sorting module.

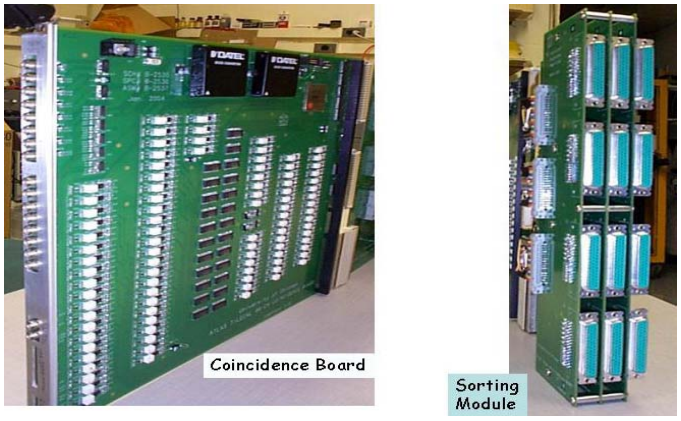


Figure 3: Picture of the coincidence board and the sorting module.

A. Sorting Module

The TileCal cell structure is shown in Fig 4. The adder cards sum up to 5 PMT signals to produce a tower trigger signal. For the barrel, the trigger signals are listed in Table I. The central 8 tower signals will be used for the stand-alone trigger electronics.

TileCal BARREL			
η Value	PMTs by cell	PMT Positions	Adder Position
0.0-0.1	A1R A1L BC1R BC1L D0R	5 2 3 4 1	4
0.1-0.2	A2R A2L BC2R BC2L D1L	9 6 7 8 14	7
0.2-0.3	A3R A3L BC3R BC3L D1R	11 10 13 12 15	10
0.3-0.4	A4R A4L BC4R BC4L D2L	19 16 17 18 26	15
0.4-0.5	A5R A5L BC5R BC5L D2R	21 20 23 22 27	21
0.5-0.6	A6R A6L BC6R BC6L D3L	25 24 29 30 40	28
0.6-0.7	A7R A7L BC7R BC7L D3R	31 28 35 36 43	31
0.7-0.8	A8R A8L BC8R BC8L	37 34 41 42	34
0.8-1.0	A9R A9L B9R B9L A10R A10L	39 38 45 46 47 48	42

Table I: PMT signals summed for each tower trigger signal from the barrel modules.

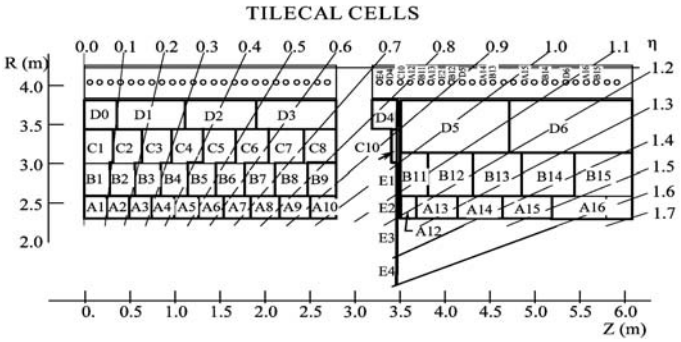


Figure 4: Geometric layout of the TileCal trigger towers.

The sorting module is built as a passive 3-width module with one 9Ux240mm board and two 9Ux100mm boards. It is plugged into the rear of the VME chassis. The sorting module receives signals from the trigger towers of 12 barrel calorimeter drawers, six above the horizontal plane and six below. The signals from each drawer are supplied on an 80-meter-long multi-conductor cable containing 16 individually shielded twisted pairs. Each cable is terminated with a 50-pin connector. The relation between the trigger tower rapidity (η value), its calorimeter cells, and the photomultiplier positions are shown in Fig. 4. The signals are sorted and sent to the coincidence board via the VME P5, P6 connectors.

Another major feature of the sorting module is the avoidance of the ground loops between the detector and the trigger electronics systems. On the detector side, the individual signal shields and the common cable shield are all connected to the signal ground directly. At the sorting module side, the individual insulated signal shields are connected to local electronics ground via a 0.1uF ceramic capacitor and with an option of 1kΩ resistor in series. However, the common cable shield is required to be connected to VME chassis. The local electronics ground and VME chassis are connected to rack ground. Very good noise immunity is obtained by these configurations.

B. Coincidence Board

The 96-channel coincidence board is built on a single-width VME 9Ux400mm board and receives differential signals from the sorting module via its P5, P6 connectors. Due to signal loss over an 80-meter long cable, the typical signal amplitude for a muon is only ~20mV at the input of the coincidence board. The schematic of one of 96-channel amplifier-discriminators is shown in Fig. 5.

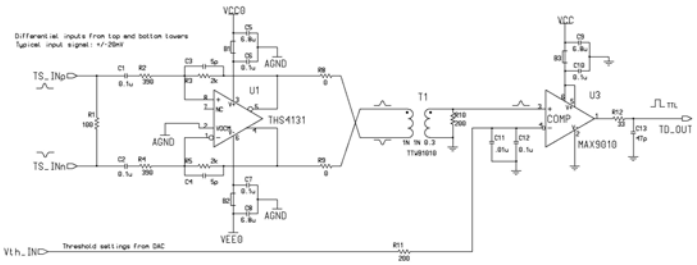


Figure 5: One of the 96 amplifier-discriminator channels.

A high speed, low noise, low power fully differential op-amp THS4131 is exploited to receive and amplify signals from the long cable. The THS4131 op-amp has balanced outputs that provide an excellent common-mode noise rejection for the circuits. The input differential signals are AC coupled to the THS4131 amplifier which is operated with a voltage gain of 5. The amplifier bandwidth can be set by adjusting the time constants R3C3 and R5C4 in differential feedback networks. Limiting the amplifier bandwidth is a very significant factor in minimizing the noise level. A 1:1 pulse transformer couples the differential outputs of the amplifier to a single-end signal. The latter is sent to MAX9010 discriminator input. The transformer coupling provides excellent common mode noise rejection for the discriminator.

The MAX9010 is a high-speed voltage comparator that has precision differential inputs and TTL output. It has maximum propagation delay time of 10ns and a wide common-mode input range. This makes it a good device as a rising edge discriminator for this application. Another important feature for the device is the lack of oscillation when the comparator is in its linear region. Most high-speed comparators require minimum slew-rate for the input signals. If the input signal does not transverse the linear region within the propagation delay time of the comparator, the output can be unstable. The MAX9010 has no minimum input slew-rate requirement, so that the hysteresis circuitry to overcome instability for this discriminator is eliminated. Even though we have a relatively low slew-rate input signals, very stable discriminator outputs are obtained. The TTL outputs of discriminators are sent to an FPGA for further digital processing. The entire digital logic is implemented in one Altera EP20K160E356X that is shown in Figure 6.

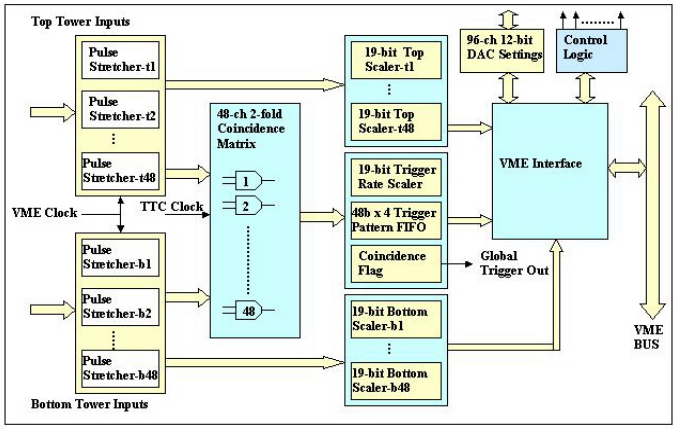


Figure 6: The digital system implemented in Altera EP20K160E356X.

The circuitry implemented in the FPGA on the coincidence board includes:

- 96-channels of pulse stretchers that receive discriminator outputs and stretch the pulses to a minimum width of 37.5ns before sending them to the coincidence matrix and the tower signal rate scalers.
- 48-channels of 2-fold coincidence matrix that processes 48 top tower signals and 48 bottom tower signals in the 2-fold coincidence logic.
- 96-channels of 19-bit tower signal scalers that monitor each tower signal rate. An additional overflow bit is provided for each channel.
- A 19-bit trigger rate scaler that counts the total trigger rate for the 48-channels of 2-fold coincidences.
- A 1-bit coincidence register that stores any of the 48-channel of 2-fold coincidence outputs. This signal is converted to a NIM level signal and routed to the front panel as a global trigger signal.
- A 48-bit wide by 4-bit deep FIFO that stores up to 4 coincidence patterns before being readout by the computer.
- A 12-bit DAC setting register that loads the 96-channels of 12-bit DACs. Each DAC output sets the threshold of one discriminator.
- 8 pairs of front panel NIM level I/O signals that are used as the system diagnostic test.
  For example, the discriminated tower signals can be routed to the outputs in groups of 8 under program control.
- VME interface and other control logic.

The FPGA can be reprogrammed insitu from a laptop computer if the configuration is required to change.

PCB layouts have been reviewed to validate signal integrity. Because the coincidence board is located in a VME crate and because many analog and digital components are placed on the same board careful component placement and board layout are required to achieve low noise performance. Separated analog and digital power supplies and grounds are necessary. Two dual voltage DC-to-DC modules are employed to convert the system 5V power supply to +/-5V analog power supplies. Each DC-to-DC module supports 48 channels of analog circuits. Decoupling with a chip ferrite bead in series, and a 0.1μF ceramic capacitor to ground is also used on each analog supply terminal. The 0.1μF ceramic capacitor is placed as close as possible to the analog supply terminals to get the most effective decoupling.

The analog and digital signals are routed in different layers to prevent crosstalk. All input differential analog signals are grouped and routed with a matched differential impedance of the input cables. Each pair of differential signals is terminated at the amplifier's inputs.

III. System Test Results

Figure 7 shows test beam data for muons in three η ranges. The distributions peak at 2 to 2.5GeV depending on the η value. A trigger threshold of about 1GeV should give good efficiency at all η values. This signal level is at the extreme low range of the TileCal trigger's dynamic range. Studies made with the stand-alone trigger system and with the TileCal front-end electronics using the charge injection system have proved that triggering at this low signals level is feasible.

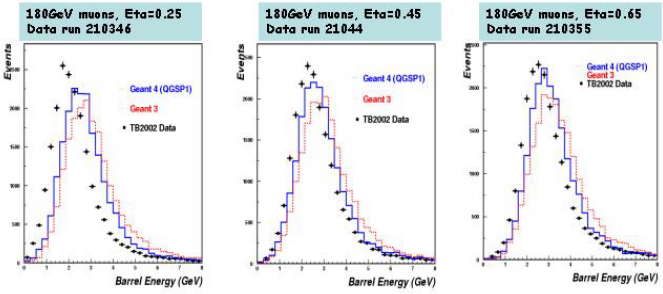


Figure 7: Muon signal distribution vs. energy for towers in the TileCal barrel.

A large signal was injected into a normalization channel, and 1GeV signals were injected into 2 channels in coincidence. The normalization channel scaler was compared to the trigger scaler to produce Fig. 8. As the thresholds are lowered on the muon signal channels, the trigger efficiency rises to 100% at about 50mV. As the thresholds are decreased further, the efficiency stays constant till about 25mV where noise begins to enter. With no signals connected, the noise threshold is at about 5mV on all channels. The standalone trigger system and the TileCal front-end electronics have adequately low noise to allow efficient triggering on single muons.

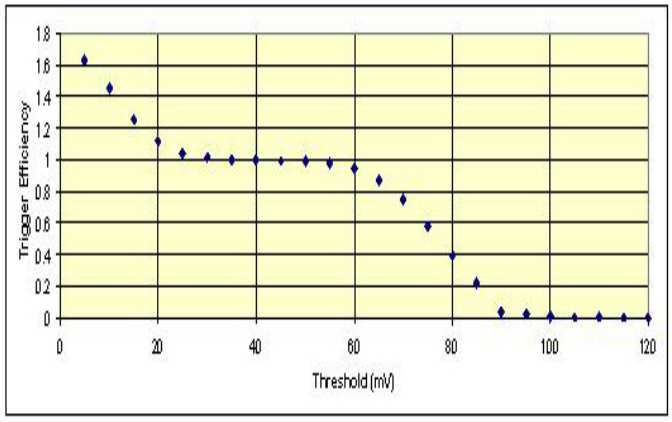


Figure 8: Trigger efficiency vs. discriminator threshold voltage.

IV Conclusion

A 192-channel stand-alone cosmic ray trigger system has been built and tested. If the noise level with the detector is similar to that seen in the test beam and on test benches, we will be able to trigger efficiently on single muon events.

V. References

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