Multiprocessor system controlling power supply distribution for the ALTAS SCT*

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Abstract

A system of many thousands of DC isolated power supplies for ATLAS Semi-Conductor Tracker (SCT) controlled by about 14 000 microprocessors forms a large system which temporal properties are essential for reliability. This system passes now various integration tests. Highlights of the system architecture are presented and details of communication aspects for the high voltage (HV) subsystem are described.

I. Introduction

4088 ATLAS Semi-Conductor Tracker detector modules and their readout electronics are supplied with various low voltages (LV) for analog and digital circuits of readout chips, for electronics to transfer digital data and with high voltage (HV) 0 – 500V detector bias. The postulate of maximum flexibility in selection of an optimal shielding and grounding scheme resulted in the design of highly modular power supply (PS) system following the modularity of the SCT detector [1].

The system has hierarchical structure. Every low voltage module is controlled by two micro-controllers. Similarly, functions of every HV (bias) voltage module are controlled by its own processor. These modules form small groups (boards). Groups of four, in the case of LV and groups of eight, in the case of HV, see Figure 1. Each group has its own master, a microprocessor which handles control and communication functions for the board. The boards, in turn, form the higher level in the hierarchy: the crates, groups of boards. Each crate consists of six HV boards and twelve LV boards. Each crate again has its own microprocessor which mediates the communication between boards on the one hand side and the higher level of the detector control system (DCS) on the other one.

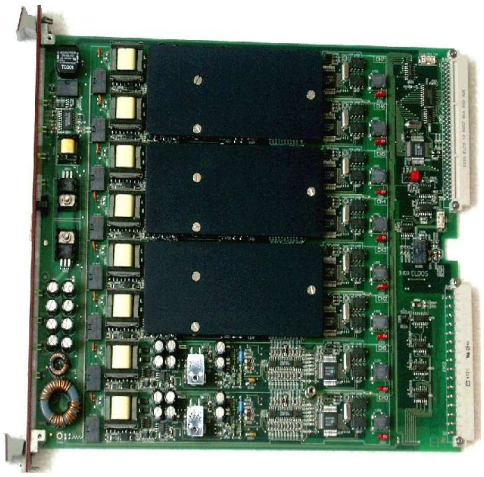

Figure 1. Board with 8 modules of the HV SCT power supplies.

Basic design principles of the SCT power supply and distribution system has been presented elsewhere [2]. A detailed and complete description of the whole PS system is in preparation. In this contribution the HV subsystem is described with particular attention paid to firmware of the card and module controllers and to communication aspects.

A microprocessor in every module permanently controls and monitors module parameters with the help of 12-bit DACs and ADCs. These functions may eventually be interrupted by masters requesting either new settings or fresh reports. Modules act concurrently but, within groups, share communication

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lines: opto-coupled serial links in the case of module-board communication, custom parallel buses in the case of board-crate communication and the CANbus on the level of communication between crates and DCS. These control, monitor and communication functions form a complex and interesting play of synchronous and asynchronous processes.

II. Single Module Firmware

Every HV power supply module provides output voltage from the range of 0 to 500V which, in normal conditions, should be set with one of four predefined ramping speeds (50, 20, 10 and 5 V/s). Input parameters defining the working conditions of the module contain, in addition, an overcurent trip limit which may be selected from the range of 100nA to 5mA, the maximum allowed current load.

Every HV module is controlled by the ADµC812 8-bit CISC processor (8051 instruction set compatible) clocked by 8 MHz clock, making one machine cycle equal to 1.5µs. The ADµC812 is fully integrated 12-bit data acquisition system incorporating self-calibrating multichannel ADC and dual DAC. These processors are programmed in assembly language. Programmes are loaded into their internal program flash memory of 8 kBytes.

After power-on the HV module controller programme initiates its variables, clears buffers and sets working modes and parameters for its internal devices (UART, ADC, DAC and timers). Then, enters an endless loop that executes the following functions:

- measures output current,
- checks the output current against the over-current trip limit,
- measures the output voltage and checks against the over-voltage conditions.

This loop is extended with:

- functions that control the ramping when programme is in the state of setting new parameters,
- functions for module report transmission on request from the card controller.

This loop may be interrupted with following events:

- serial UART reporting receive/transmit actions,
- timer0 or timer1 completion.

ADC is not used in an interrupt mode since a single conversion is faster then any simple interrupt service routine. ADC is initialized to work with an optimal 2 MHz master clock, at which a single conversion takes 8µs. ADC and DAC use the common 2.5V internal voltage reference. UART interface is set to mode2, 9-bit transmission, 1 stop bit and 0.25 MHz baud rate.

Card and module controllers communicate via serial transmit/receive lines and UART interfaces. There are three forms of messages:

- 13-byte "new settings" message transmitted from the card controller and received by the module controller (Table 1),
- 2-byte message, transmitted by the card controller request for report addressed to a particular module,
- 6-byte report transmitted from a module and received by the card controller (Table 2).

Table 1: "New settings" message

Byte	Meaning
1	Number of bytes to follow (0x0C)
2	Command code
3	4 high bits of requested voltage
4	8 low bits of requested voltage
5	4 high bits of current trip limit (probe 0)
6	8 low bits of current trip limit (probe 0)
7	4 high bits of current trip limit (probe 1)
8	8 low bits of current trip limit (probe 1)
9	4 high bits of current trip limit (probe 2)
10	8 low bits of current trip limit (probe 2)
11	4 high bits of current trip limit (probe 3)
12	8 low bits of current trip limit (probe 3)
13	Ramping rate code

The UART interface interrupt service routine of the card controller spends about 20µs reading one byte. Consequently, module controller needs about 40µs to service one incoming byte. One has to take care that the byte writing rate of the faster (card) processor does not exceeds the reading capabilities of the module processor.

Table 2: Module report message

Byte	Meaning
1	Number of bytes to follow (0x05)
2	Module status word (Table 3)
3	4 high bits of the voltage readout
4	8 low bits of the voltage readout
5	4 high bits of the current readout
6	8 low bits of the current readout

At the selected baud rate the transmission of one byte takes 44µs and e.g. transmission of the module report message takes about 380 µs.

Table 3: Module status word

Bit	Meaning
7	Over-Voltage flag (OV)
6	Over-Current flag (OC)
5	reserve
4	Voltage unstable, ramping in progress
3	Module switched off by card controller
2	reserve
1	MS bit of the probe resistor code
0	LS bit of the probe resistor code

To maintain a decent accuracy of the output current measurements in the whole range from 100nA to 5mA the programme has built-in a self-selection of one of four probe resistors (62005, 12005, 2405 and 435 Ohm). Actual probe number is recorded in two low significant bits of the module status word. This allows later to convert 12-bit ADC readout to nA. In the case of over-current detection, the module controller takes these immediate actions:

- reduces output voltage to zero
- blockades the HV output line of the submodule
- sets the corresponding flag in the submodule status word

The module remains under control of the card controller and responds to its commands. The card controller will switch this module off as soon as it receives its report.

The output voltage measurement is designed in such a way that the maximal ADC readout (0FFF in hex) correspond to 511V (1 bit corresponds to 125 mV). Such a readout is normally not expected and causes setting of the Over-Voltage flag in the module status word, like any other readout showing that the output voltage exceeds the required value by more than a predefined tolerance.

One typical uninterrupted pass of the endless loop of the module controller programme takes about 160 µs. Single passes my be extended to several hundreds of µs, depending on various conditions. All monitoring and control functions are maintained also when module is in the voltage ramping stage since even for the fastest ramping (50 V/s) one step is done only every 2.5ms.

The general principle of the communication of the module with the card controller is: stay silent. The module never initializes communication actions. It collects the output voltage and current measurement data, updates the appropriate bits in its status word and sends updated buffer status only on request from the host, the HV card controller.

III. Card Controler Firmware

Like the HV module controller, the HV card controller is also built on the base of the Analog Devices's ADµC812 processor. The card controller are clocked at 16 MHz, making the machine cycle equal to 0.75 µs.

The card controller provides the communication bridge between the crate controller and eight HV modules located on the card. The communication with the crate is done via 8-bit address/data bus using a custom communication protocol. The communication with the 8 HV card modules are via a serial UART link. The card controller mediates in the following control and monitoring functions:

- switches ON or OFF given channels,
- reports the card status,
- transmits new parameters to the given channel,
- reports the status and measurements of the given channel.

All the above actions are taken in response to an operator request. Besides, it may automatically switch off one module or group of four modules whenever OV or OC flag is set in module's status word or when the interlock latch is set.

The programme runs an endless loop which checks the list of present requests and cyclically interrogates all active modules for the current status and measurements. It keeps the actual values of these measurements in individual buffers of each of eight modules. It is then ready to transmit the buffer on request of the crate controller without delay.

IV. Custom Crate Controler Bus Communication

The crate controller for the SCT Power Supply System is build upon the ELMB[3] card. The ELMB's main controller is the Atmega128L 8-bit RISC processor. It has 128-Kbyte self-programming Flash Program Memory, large enough to be comfortably programmed in C-language.

The Crate Controller program has two main groups of functions:

- communication with the LV and HV cards in the crate to pass the control and monitor commands via a custom parallel 8-bit bus and a custom communication protocol,
- communication with operators of the Detector Control.

This second group of functions will not be discussed in the present contribution.

Low level communication protocol has identical elements for all functions both, for LV and HV cards. Differences are only in number of data bytes send or read by the ELMB's micro-controller ATMega128. This custom communication protocol uses 8-bit parallel address/data bus and several control signal lines, physically located on the backplane of the crate. The protocol is under master control of the ATmega128 crate controller which communicates with card controllers on HV and LV cards.

There are following low level communication functions:

- write (set) HV board,
- write (set) HV module,
- read HV/LV board (HV: status, byte of active channels, firmware version number),
- read HV module,
- write (set) LV board,
- write (set) LV module,
- read LV module.

Ignoring for the moment distinction between HV and LV we see *four* basic functions: SET BOARD, SET MODULE, READ BOARD and READ MODULE.

All these (read/write) functions are build from *three* basic building blocks, i.e. basic elements of the custom communication protocol:

- Send Board Address (SBA)
- Send Data Byte (SDB)
- Read Data Byte (RDB)

Each crate controller communication function refers to one and only one board at a time. Every function then starts always with sending one byte, the address of the board (5 low significant bits) associated with 3 most significant bits SBR ("set", "board", "reserve"). SBR bits announce, which of the *four basic function* is going to be further processed.

Send Board Address (SBA) element is always the first element of every function. The basic steps of the protocol are:

- address of the board and SBR bits are ready on ADDR/DATA lines,
- Address Strobe (AS) is send over the bus. This signal is generated by ATmega128 and received by *each* board in the crate as External Interrupt 0, the signal of the highest priority. All boards are always sensitive to that signal i.e. this interrupt can never be masked.
- One (and at most only one) board which is addressed respond with the acknowledge (ACK) signal, and *only* this board enables External Interrupt 1 service which make this board, and *only* this board ready for receiving data bytes which follow. ACK signal is received by ATmega128

which takes out the AS. The protocol is a bit reacher. There are technical control signals which e.g.: control the chip enable functions for line drivers, the read/write (R/W) signal to control the direction of the data flow: from the Crate Controller to the Card Controller or vice versa. (The R/W is set to *write* at the time of sending the address (SBA) since ATMega128 *writes* the address to the bus, sending it *to* the Card Controller). Functions have also built in detection of the *time-out* exception when waiting for ACK.

Send Data Byte (SDB) element (the Crate Controller sends byte *to* the Card Controller):

- data byte bits are ready on ADDR/DATA lines,
- Data Strobe (DS) is send over the bus. This signal is generated by ATmega128 and is transmitted as the External Interrupt 1 signal to all boards but serviced by this board (and only this) which identified itself at the address transmission time and which has set its interrupt enable flag for the external interrupt 1,
- the data byte is received and this is confirmed by sending ACK signal by the Card Controller *to* the Crate Controller,
- in response to that the Crate Controller takes out the DS.

During SDB the R/W signal is set to *write* (low level) since it is still the Crate Controller which *writes* data *to* the card.

Read Data Byte (RDB). However in this case the data byte is send *from* the card controller *to* the crate controller, it is still the crate controller which drives the communication:

- Data Strobe (DS) is send over the bus. It is again serviced as external interrupt 1 by the addressed card, the only one which still has ext. interrupt 1 enabled,
- in response to the DS the card controller sets the data lines and
- sends the ACK signal communicating that data are ready,
- the crate controller reads the data, and takes out the DS,

During this operation the R/W level has been turned to the *read (high)* level by the master (i.e. by the crate controller),

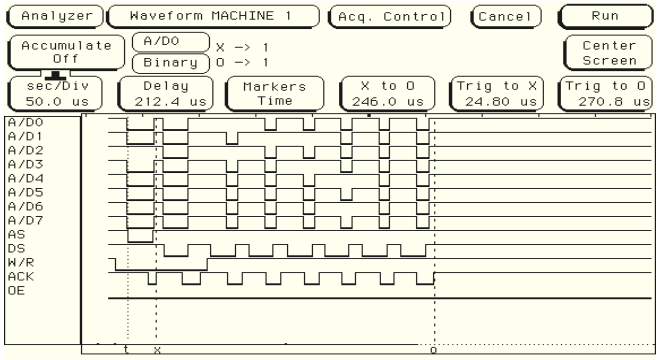

Figure 2. Example of temporal relations of signals for the *read module* function.

All read/write functions are built from these three elements.

Examples:

Read HV board: SBA RDB RDB RDB

Read HV channel: SBA SDB RDB RDB RDB RDB RDB

The last example shows a composition of three basic blocks for reading the report from a given module The crate controller sends board address to all boards in the crate and then the data byte specifying the module number. That byte is received by selected board which replies with 5 data bytes. After sending first two bytes (SBA and SDB) the crate controller changes direction of the data transfer with help of the R/W signal (see Figure 2.).

The composition for the "set HV channel" function looks like: SBA SDB SDB SDB SDB SDB SDB SDB SDB SDB SDB SDB SDB SDB ....

SCT power supply system has developed into large system consisting of about 14 000 microprocessors. Temporal properties of such large real time system must be carefully tested, analyzed and debugged.

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