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P. Jarron et al.

Sical-Amplex status report

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I. Situation of Sical-Amplex chip

Amplex3-B version has been measured at Saclay. Dynamic range, noise, crosstalk are in the specifications. Calibration circuit works correctly. The value of the calibration capacitor measured on few chips at Pisa and Saclay is 2.03 pF (2.12) ± 0.36% (0.35) r.m.s. Therefore, the precision is sufficient to have only one value of calibration capacitor by 16 channel-chip. The fast-or(analog sum) is limited in dynamic range (1 V) because of the current limitation of the output amplifier.

The linearity in hold mode is good up to 4.5V output swing, whereas the linearity in track mode is poor above 3.5 V. The reason of this discrepancy is not yet understood. We have to do at CERN in December more precise and statistical linearity measurement to clarify if the good linearity in hold, which is actually the experimental condition, will be reliable and stable with process variation.

Last september a new Sical-Amplex version has been submitted to IMEC (Leuven-B) for Multi-Project-Chip fabrication with a better output amplifier to increase the swing of the fast-or to 4 V (12000 MIPs on 16 pads). The inverted control logic of the analog multiplexer has been also corrected. IMEC has taken in charge the cost of this new prototype because of the multiplexer error they did in the previous AMPLEX3B design. The prototype avalaible middle of december will be tested at Saclay and CERN for final acceptance before production. CERN (J.C. Santiard and M. Glaser) expect to make ready in December a preliminary version of the test bench foreseen to be used in 91 for the final acceptance test of packaged chips.

II. Budget of Sical Amplex production

There is still an uncertainty about the final production. The chip is designed in double-poly double metal process. Since only few metal-2 bridges are actually used in addition to poly-1 bridges, it is possible to convert the design from metal2 to metal1. This will save about 25% of the cost of the production. We agreed with C. Das /IMEC that he will provide us soon Sical Amplex chips type 3-B in metal1 which can be tested before the end of the year to verify if we can use metal1 process.

The size of the chip is 4 mm x 4.36 mm and each wafer contains 340 chips. The best estimate of the yield is 60%, thus we expect 200 good chips(without fatal defect) per wafer to be packaged. Assuming that further imperfections of the technology, capacitor mismatch, packaging yield and gain selection will reduce again by 50% the yield after testing of packaged chips, we ultimatly expect 100 good packaged chips per wafer.

Before packaging, about 50 samples will be sent by IMEC to CERN and fully tested at CERN to ensure the quality of the production.

The standard engineering run of 20 wafers should provide 2000 good Sical Amplex chip which seems to be more than sufficient for the Sical project. We propose to organise the wafer probing and packaging in two production runs of 1000 good chips. Normally a 1000 chips production would be just sufficient for the Sical calorimeter. Therefore, the second production is the reserve in case of unexpected bad production yield or larger gain and capacitor mismatch.

We are waitting an offer from IMEC end of November. In a mean time based on a previous IMEC offer and a discussion with C. Das, the following table approximatively quote the production cost and the testing cost.

1 Fabrication ***at MIETEC Bruxelles Belgium***

⇒ Engineering run of 20 wafers in 3 μm CMOS double poly, **single metal** technology of MIETEC, DRC checking, tape conversion and mask set......68 000 SFr

⇒ Same with **double metal** option..81 600. SFr

⇒ Production of 10 extra wafers..18 000 "

2 Testing ***at IMEC Leuven Belgium***

⇒ Analog probecard with two 6-bit flash ADC........7 800 SFr

⇒ Test program..2 800 "

⇒ Testing of 1 lot of 1000 functional good chips....12 000 "

⇒ Testing of 2 lots of 1000 functional good chips..........................24 000 "

3 Packaging ***at Anam-Kor(ITEQ) Glasgow Scotland***

⇒ Packaging of 1 lot of 1000 chips........................6 600 "

⇒ Packaging of 2 lots of 1000 chips...13200 "

4 Testing and classification of packaged chips ***at CERN-ECP-MIC***

⇒Test bunch hardware cost..5000 "

Test program : M. Glaser

Test procedure : J.C. Santiard

Calibration procedure : C. Cerri, Sanchez.

Manpower for testing : help from ALEPH collaboration ?

Minimum grand total.........................97 200

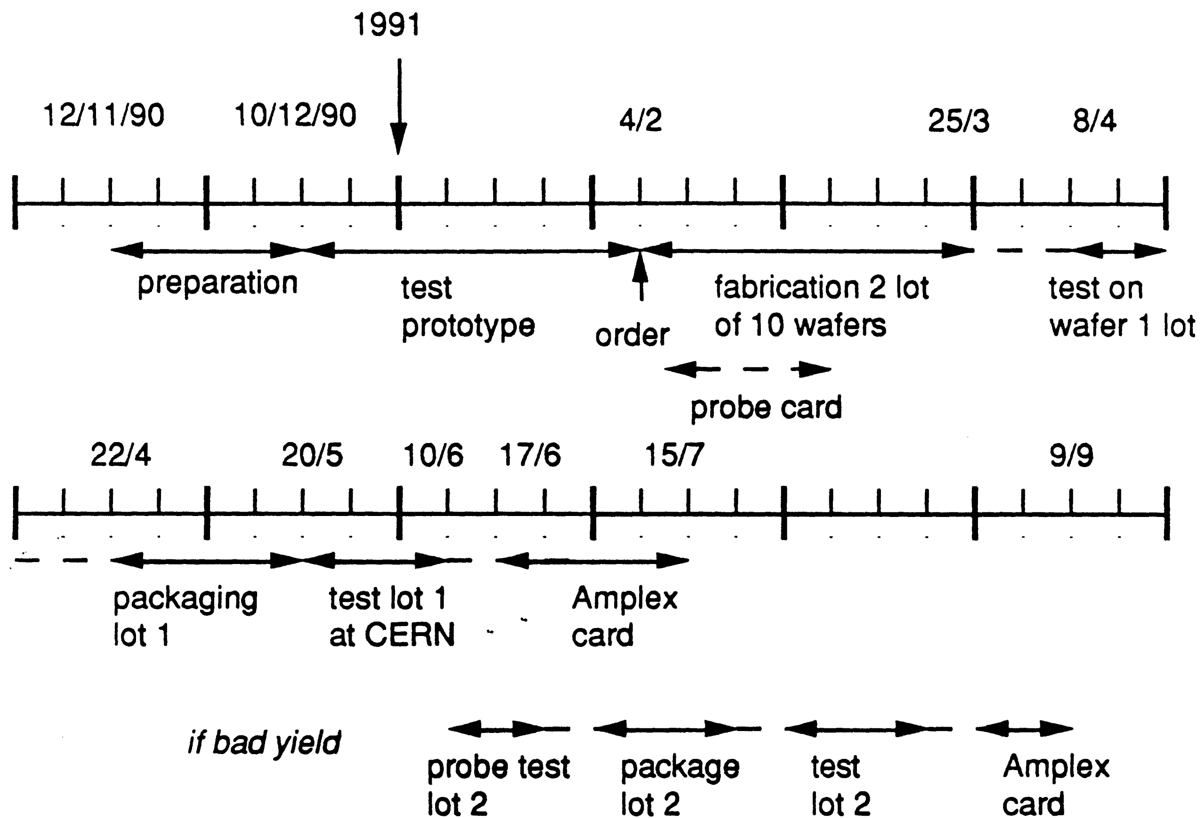
Maximum grand total..152 000"

III. Time schedule of the Sical Amplex production

The "go" of the production will be after the full test of the december prototype chip expected to be complete by the end of january 91. If the prototype has a bug which is very improbable, a prototype has to be submitted again end of january. The schedule given later does not account for that. It will delay all the project by 4 months.

The chip fabrication at MIETEC takes:

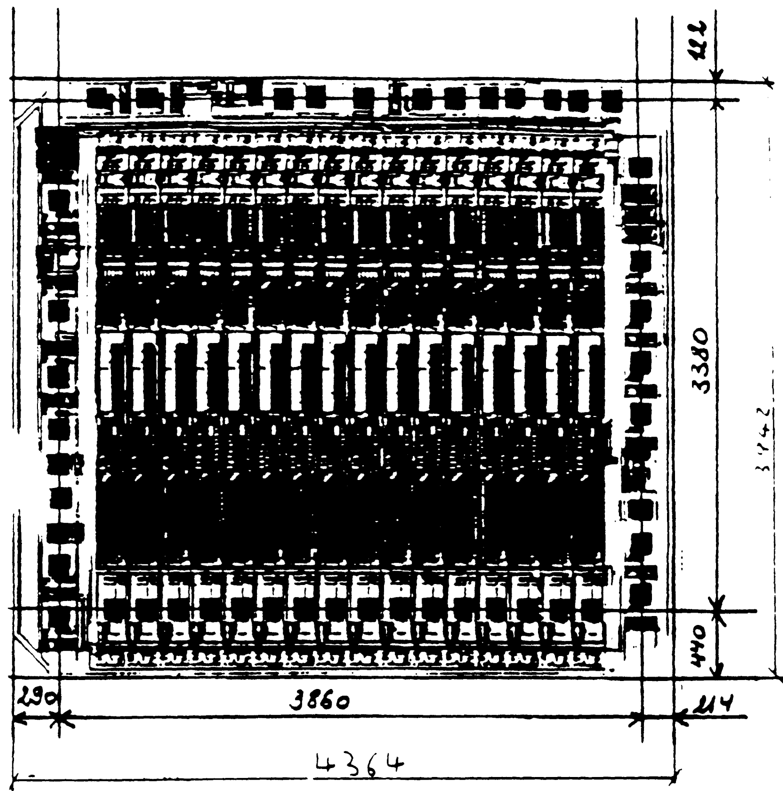
- 9 weeks for double poly double metal process
- 7 weeks for double poly single metal process
- 5 weeks for rush production with an overcost of 16 000 SFr



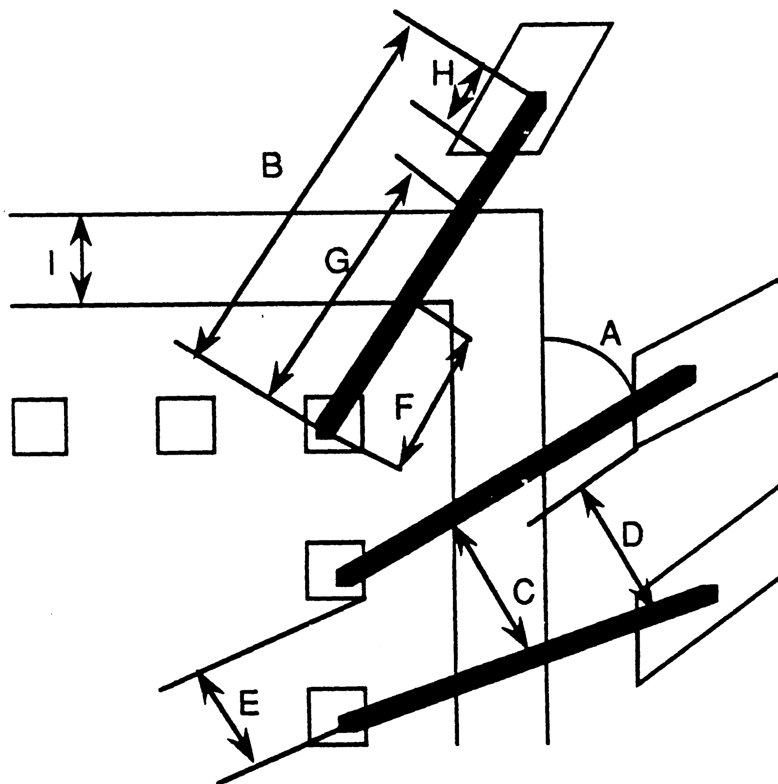
IV. Packaging

The checking of the pad assigments have shown that there is a difficulty to use the foreseen 48 pins chip carrier. The 16 input pads are disposed on one side and cannot be bonded according to the industrial packaging production rules. Other packages are studied; a 64 pin package could be compatible with the existing chip prototype. This solution avoids to redesign the peripherical layout of the chip.Unfortunatly this package 18.29 x 18.29 mm larg seems uncompatible with the size of the AMPLEX card. An other 48 pins package with a smaller cavity (6.2x6.2 mm) seems now a good alternative.

Figure 1



-PARAMETERS for wire bonding (AMKOR ANAM)



-Dimension A:	Bond angle
-Dimension B:	Bonding wire length
-Dimension C:	Clearance between two adjacent wires
-Dimension D:	Clearence from wire to adjacent lead
-Dimension E:	Clearence from wire to adjacent bond pad
-Dimension F:	Bonding wire length from pad to die edge
-Dimension G:	Bonding wire length from pad to die attach pad edge
-Dimension H:	Bonding wire length running over lead
-Dimension I:	Clearance from die to die attach pad edge

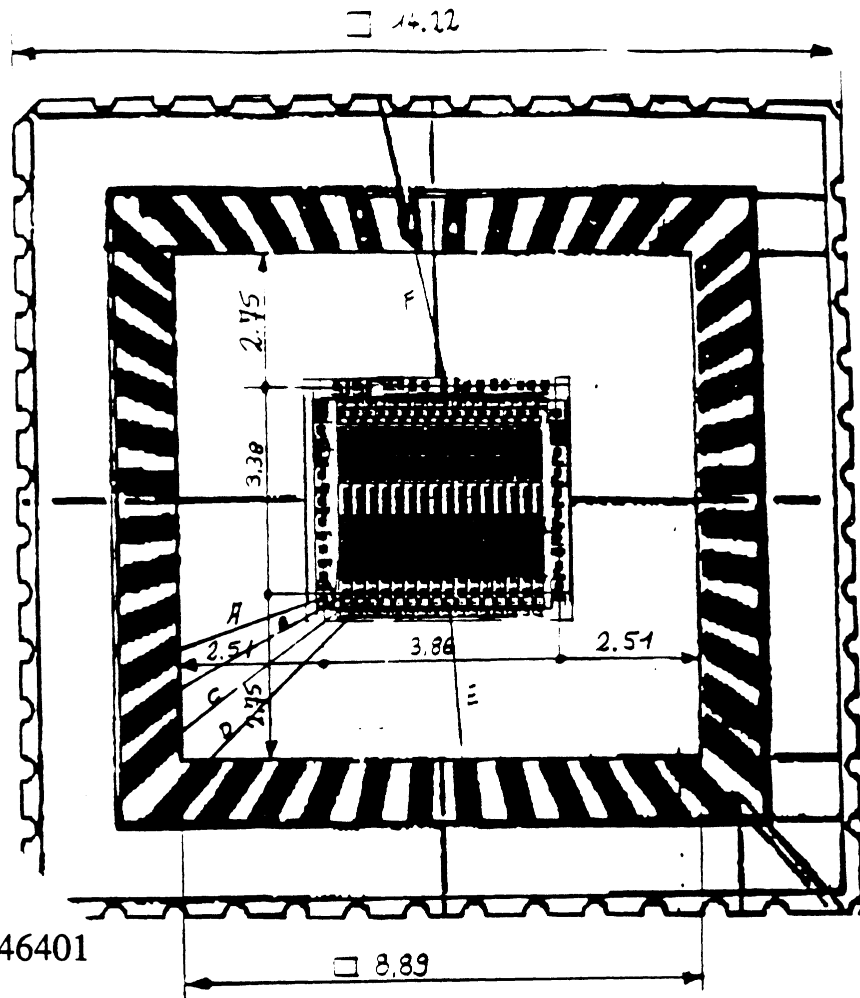
-FIRST solution

48 pins ceramic chip carrier
carrier chip part number GEN/SU88248YZ
cavity size 8.89 x 8.89 mm
made by SEMI DICE
change 1 HFL = 0.75 SFR
price for 2'000 pieces 10'500 SFR 5.25 SFR/pcs
delivery time 4 weeks

Metal lid
lid part number ELE/E5512
made by SEMI DICE
change 1 HFL = 0.75 SFR
price for 2'000 pieces 5'655 SFR 2.82 SFR/pcs
delivery time 4 weeks

Dimension	CRITERIA		CALAX		Status
	min	max	min	max	
A	30'	90'	33'		OK
B	0.88	2.91	2.35	3.98	BAD
C	0.076		0.16		OK
D	0.127		0.025		BAD
E	0.127		0.108		BAD
F		0.381		0.56	BAD
G		1.016		3.78	BAD
H	0.127		1.25		OK
I	0.254		2.14		OK

Figure 2



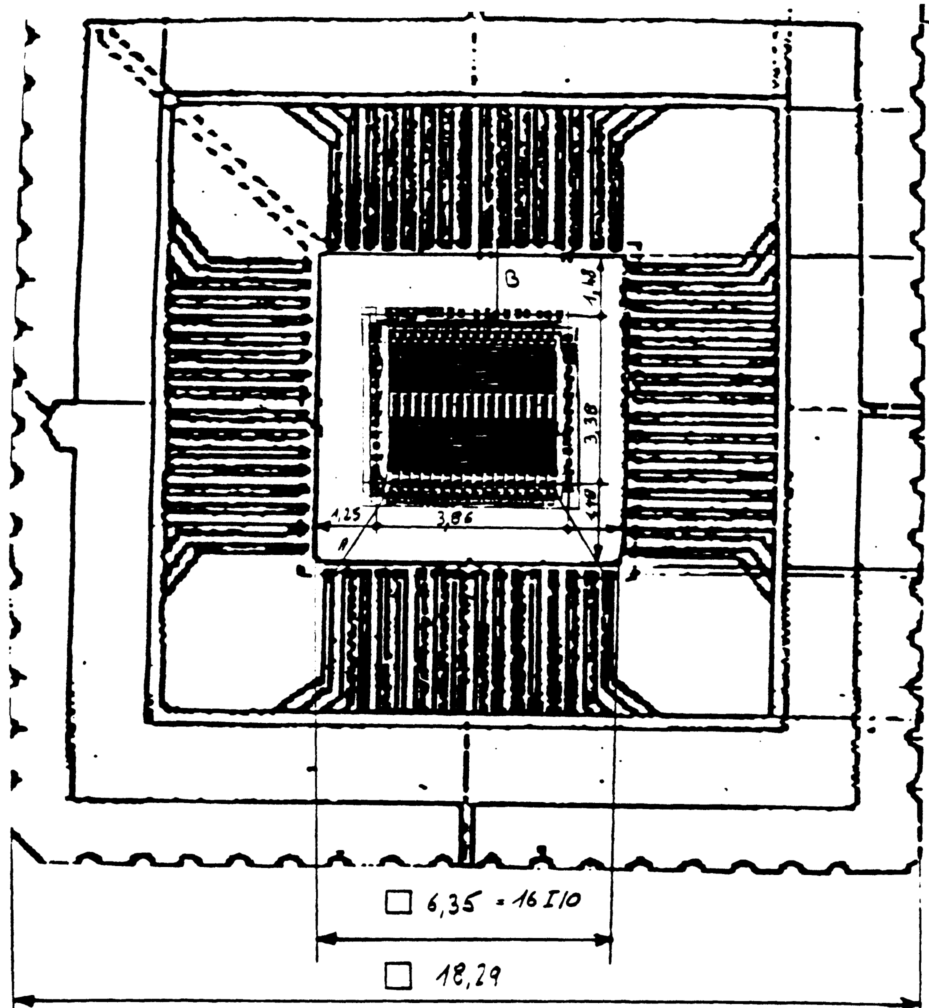
-<u>SECOND solution</u>

64 pins ceramic chip carrier
carrier chip part number CC46401
cavity size 6.35 x 6.35 mm
made by KYOCERA
price for 2'000 pieces ....- SFR ....-SFR/pcs (answer 13/11/90)
delivery time ... weeks (answer 13/11/90)

Metal lid
lid part number HR C761-21-25mt(100MNI)S
made by SEMI ALLOYS
change 1$ = 1.25 SFR
price for 2'500 pieces 3'581 SFR 1.43 SFR/pcs
price for 4'000 pieces 5'730 SFR 1.43 SFR/pcs
price for 5'000 pieces 4'930 SFR 1.23 SFR/pcs
delivery time 4 weeks

Dimension	CRITERIA		CALAX		Status
	min	max	min	max	
A	30'	90'	58'		OK
B	0.88	2.91	1.6	2.3	OK
C	0.076		0.18		OK
D	0.127		0.2		OK
E	0.127		0.108		BAD
F		0.381		0.56	BAD
G		1.016		1.5	BAD
H	0.127		1.25		OK
I	0.254		1.25		OK

Figure 3



The first solution with the foreseen 48 pins chip carrier, the bonding length is too long to guaranty no short circuit between adjacent bondings. The bonding between pin 4 (strobe-cal) and pin 5 (IN1) are too close. The second solution with a 64 pin package is O.K. if the AMPLEX card accepts the larger dimensions. A third solution is now envisaged with a 48 pins package NTK with a smaller cavity (6.2 x 6.2 mm). We are waitting the agreement of AMKOR-ANAM.

V. Test procedures

Two kind of tests have to be performed : one at IMEC , on the wafers , before packaging ; the other one at CERN to measure accurately the chips characteristics .

1- IMEC wafer probing tests

The procedure to test the AMPLEX sical chip on the wafer must be simple and efficient . This operation has to include the digital part of the circuit and a rough measurement of the amplification function of all channels , including the analog FAST-OR .

The goal of this wafer probing is to reject chips that are not working and those having characteristics too far from the specifications.

Two sequences of tests are needed :

- The amplification function will be tested on two points through the calibration input :
  - 0 Volt input , to know the pedestal value.
  - 1.64 Volts input gives a value in the highest part of the linear range .

These tests will be performed with two measurements windows ; 1.6v ± 0.1v ; +3v ± 10%. By checking , for each selected input ,all outputs one can infer on the general

functionality of the chip. A test of the droop-rate can be done by just delaying the measurements time (5ms)

- The analog FAST-OR will be tested by applying a signal at the test input with all the inputs ON and testing the output with all the outputs ON .In this case ,the total amplitude is equivalent to the amplitude given by one channel in the normal operation mode .

2- CERN tests

These tests have to measure carefully the characteristics of the chips in order a classificatic in categories of gain and calibration capacitors if necessary. It is scheduled to start by the end of december, on the new prototypes with a statistics of 50 chips a preliminary evaluatio of the specifications ; but it is only after having tested several wafers that we will be able tc define a set of characteristics allowing classification of the chip.

We have to build an automatic test bench providing an analog signal delivered by a 12 bits D to A conversion and a digital pattern. To perform accurate the measurement of analog informations a 12 bits A to D conversion will be used. This equipment has to be connected to a PC computer which can pilot the tests procedure and keep tracks of the resul

We will use the same test bench as for the old AMPLEX : PC computer, ASSYST sofware and LAB MASTER 12 bits hardware system. Some improvements should be done to perform the linearity measurements and to test the calibration capacitor circuit.

Systematic tests of the packaged chip

- 1. **gain, linearity and dynamic range** will be measured with 3 values of charge injection
  0 mips , 500 mips , 1000 mips hundred times each .
- 2. **noise** : due to the large dynamic range , an additional gain of 10 must be used to perform this measurement with a good precision .
- 3. **calibration capacitors** : will be measured on one value of injected charge .
- 4. **peaking time** : this parameter will be determined by sweeping the T/H signal by step of 10 ns ,10 times around the expected value .
- 5. **droop-rate** : one measurement (500 MIPS) will be done after 5 ms and compare to the one made for the linearity .
- 6. **gain/det.** : the gain variation will be measured with 2 values of Idet. ,50 nA and 100 nA, and compare with the one made at 0nA .
- 7. **fast-or** : will be checked by measuring the sum of the 16 channels.

The precise rejection windows and mean values of these mesurements and the chip classification will be more precisely determined after the measurement of the december prototype.

The other specifications given in the specification table will measured on few samples to verify the overall quality of the chip fabrication.

VI. Calibration

The calibration circuit implemented in the AMPLEX 3B chip is working correctly, and c the base of measurements done on few samples.The digital part does not present problems b

the data output which has been omitted. Therefore, it would be not possible to connect the control in daisy chain. This is not a problem for SICAL but it can be a limitation for other uses .
The analog part is working quite well. The serie resistance of the analog switches have a valu of Ron = 550 Ω with a small dispersion of 2 %. The calibration capacitors are well matched in the same chip (Ccal = 2.131 ±0.0075 pF or ±0.36%) while measurements on different chips are under way. We have found an unexpected capacitive crosstalk (27 - 108 fF) or (1.2 % - 4.8 %) smoothly distributed in all channels, further we have measured a feed-through in the analog switch in the range of (0.1 - 1.2 %).
The two effects mentioned above , even if they are not dramatics , reduce the possibility to measure directly the crosstalk. Some modifications could be foreseen inside the chip and implemented, specially if a prototype would be submitted again to IMEC for other important bugs

VII. Specifications sheet

Specifications	Absolute Value	Chip/dispersion	class/disp.
1- NOISE	1500 el. + 40 el./pF ≈ 0.14 Mip at 40 pF	---	---
2- GAIN	0.229 µV /el. ≈ 5.15 mV /Mip	± 2%	± 5%
3- LINEARITY (hold) (full dynamic range)	---	(±2% or ±1%)	---
4- DYNAMIC RANGE	4.45 V ≈ 1000 Mip at 35 pF	---	---
5- CROSSTALK	-2 %	±0.5%	---
6- C. CALIBRATION	2.1 pF(±15%)	±0.5%	?
7- MULTIPLEXER SPEED	500 Khz	---	---
8- PEAKING TIME	300 ns*+ 1.4 ns / pF	±10 nS	?
9- DROOP RATE	1mV / ms	---	---
10-TEMPERATURE STABILITY	0.1% / deg. (?)	---	---
11-INPUT IMPEDANCE	≥ 500 Ω 6000 pF	---	---

12-SETTLING TIME T/H	600 ns	---	---
13-GAIN / Cdet.	-0.35% / pF	?	
14-GAIN / Idet.	0.025% / nA		

(*)The peaking time is measured by scanning the track and hold. It defines for the Sical calorimeter the hold delay. The peaking time has two componants. A pure transmission dela of 100ns and a time to reach the pulse height of 300 ns. The actual time to delay the hold edg is 400ns and not 300 ns.

LAST NEWS.

The new package found by J Pascual has been accepted by AMKOR ANAM. It is a 48 pins ceramic chip carrier, compatible wit the previous one.