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TRIGGER SUPERVISOR SPECIFICATIONS

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GENERALITIES

I.A Introduction

The ALEPH Trigger Supervisor was specified in the ALEPH note DATACQ 85-21: Hardware Functional Specifications for Data-Acquisition. These specifications were expanded by the introduction, early 88, of the Cosmic mode of operations, where the calorimeters impose extra dead-time during refreshes.

The Trigger Supervisor was implemented as an ALEPH Event Builder (STR 501) coupled to a specific module containing the fast logic needed to transmit trigger signals. This document describes this module, called TS in the following.

I.B Functions of TS

The TS has three main functions: Blocking of events when the data-acquisition is not ready: the fast logic. Error detection and On-line dead-time monitoring.

I.B.1 FAST LOGIC

The definition of READY depends on the operating mode. In addition to the operation modes needed for data-acquisition, one has defined test modes.

I.B.1.a Normal operations

The main function of TS is to generate the signals used by the various detectors to control read-out. The TS elaborates an overall READY for the detector from the BUSY/GBXAK signal (from the ROCs, the Read-Out Controllers of the ALEPH sub-detectors) and from other conditions (i.e. REFIN). When the detector is ready, the next beam crossing is an event candidate (EGBX and GBX signals). Trigger levels are checked to see if the crossing has produced a good event. If not, the detector is reset (L1NO and L2NO signals). If yes, a data-acquisition cycle is initiated (L1YES and L2YES signals). At the end of the event read-out, the ROCs inform the TS of the end of the BUSY state.

The fast signals generated by the TS are: EGBX, GBX, L1NO, L1YES, L2NO, L2YES and GREF. The protocol for most of these levels was defined in DATACQ 85-21. These levels are generated from Timing Unit signals, Trigger Logic levels and the BUSY/GBXACK answer from the ROCs.

I.B.1.b Special Modes

For some applications of the TS, the normal operation mode is not convenient. So special modes were defined to cope with these needs.

I.B.1.b.1 Automatic Mode

This is a debug mode, useful only when setting-up the DAQ. In this mode the TS ignores the BUSY/GBXACK responses from the ROCs: GBXACK and BUSY are replaced by one internal signal.

I.B.1.b.2 Trigger Bypass Mode

This is a mode where the TS is running without Trigger Logic (i.e. cosmic mode, pulser calibrations, Trigger Logic set-up). When this mode is selected, the levels from the Trigger Logic (LVL1, LVL2, TMT) are ignored and replaced by a model. The TRIGGER MASK information is also ignored

I.B.1.b.3 Timing Bypass Mode

The normal mode of operations for the TS requests 4 timing signals (EBX, BXIN, L1STR and L2STR) with the proper sequence. In some applications of the TS (mainly as sub-detector TS), it is not convenient to generate these signals. The TS has been fitted with a low quality pulse generator to emulate 0 to 4 of the last timing signals. The use of this mode without Trigger Bypass Mode should be carefully studied.

I.B.1.c Internal Test Mode

These modes are used to test the hardware of the TS.

I.B.1.c.1 Static Mode

With this mode, it is possible to set all outputs of the TS, directly by writing a register where one bit is associated to each output. This is useful when checking the signals transmission.

I.B.1.c.2 Time-out Test Mode

To test the operation of the time-out hardware, it is possible to enable one of the time-out counters to run up to expiration. The time-out condition is handled in the normal way.

I.B.1.c.3 Counters Test Mode

The procedure to check the operations of the TS counters is: First, a Master Counter is pre-loaded. Then, all counters are incremented simultaneously (at about 2 MHz) until the Master Counter overflows. Then, the other counters should contain a known value.

I.B.2 ERROR DETECTION

In DATACQ 85-21, the TS was requested to check the validity of BUSY/GBXACK. We have extended the verification to all the TS timing inputs.

When an error is detected, the TS stops, asserts the HOLD output and interrupts the STR501. The levels generated by the TS at this time are held until a reset action is taken in the data-acquisition software. The detectors should be prepared to accept these sequences.

I.B.2.a Protocol violations

A protocol violation occurs when BUSY or GBXACK are inconsistent or don't follows the protocol described in DATACQ 85-21.

The verification of BUSY/GBXACK checks the following:

- BUSY should be on when GBXACK is on.
- GBXACK should be off when BUSY is off.
- BUSY should be off from end-of-busy to EGBX.
- GBXACK should be on from GBXACK to the last Trigger Logic decision (L1NO or L2STR).

I.B.2.b Time-outs

Each expected signal is guarded by a watchdog. Expiration of a watchdog produces the corresponding time-out error. The seven watchdogs are:

- GBX	to	GBXACK	2 µs
- EGBX	to	BXIN	4 µs
- L1NO	to	$\overline{\text{BUSY}}$	10 µs
- GBX	to	L1STR	10 µs
- L2NO	to	$\overline{\text{BUSY}}$	40 µs
- L1YES	to	L2STR	60 µs
- BUSY duration			650 ms

I.B.3 DEAD-TIME COUNTERS

The TS has to measure the dead-time of the experiment. This is based on a measure of the duration of BUSY. This is implemented with a resolution of 10 µs. The useful information is the duration of BUSY for good events (L2YES), but this imply the availability of the duration of all BUSY states.

An additional measure of dead-time is based on a set of event counters, counting the number of BX and L1YES. The counting of L2YES is done by the STR501. The number of L1NO and L2NO can be obtained by differences. The counting of BX is split in three different counters, according to the state of the TS:

- Ready BX counted in GBX counter.
- BUSY BX counted in BX on BUSY counter.
- Other BX counted in BX on Pause counter.

I.C Interfaces of TS

I.C.1 ROC/FIO INTERFACE.

This interface was defined in DATACQ 85-21. Since that time, five levels were added: EGBX, MT, READY, PAUSE REQUEST and GREF. The complete list of levels is now: BUSY, GBXACK and PAUSE REQUEST as input, BX, EGBX, GBX, L1NO, L1YES, L2NO, L2YES, HOLD, MT, READY and GREF as output.

BUSY and GBXACK are identical at the level of the ROCS. BUSY is the **or** of all the ROCs BUSY. GBXACK is the **and** of all the ROCs BUSY.

EGBX is an early warning of GBX, the gated beam crossing.

L1NO, L1YES, L2NO and L2YES are the Trigger Logic decisions.

HOLD is the level issued by the TS when an error has been detected. It is used to freeze all levels on the cables between the TS, the FIO-boxes and the ROCs. The error conditions able to generate HOLD are programmable in the TS.

MT is a random event indicator. The Trigger Logic generates random events for background study and for calibration. These events are flagged in the TRIGGER MASK, but an early warning is requested by the TPC.

PAUSE REQUEST is a level used to pause the TS, i.e. during ECAL refreshes in cosmic mode. PAUSE REQUEST is ignored in test mode.

GREF is a signal used in cosmic mode to refresh HCAL electronics. When enabled, it is a copy of REFIN. The internal pause of the TS is the **or** of PAUSE REQUEST and of GREF.

READY is the ready state of the TS. It is provided as a PAUSE REQUEST acknowledge. Great care for the propagation times should be taken, if one want to use this signal to foresee the imminence of an EGBX.

I.C.2 TIMING UNIT INTERFACE.

The TS expects four timing inputs: EBX, BXIN, L1STR, L2STR.

EBX and BXIN are event timing. In collider mode they are 45 KHz pulses just before a beam-crossing, in principle EBX is 2 μs before BXIN, BXIN is 2 μs before actual beam-crossing. In cosmic mode they are generated just after the passage of the muon.

L1STR and L2STR are the strobes for sampling the results of the Trigger Logic. L1STR is expected 6 μs after BXIN, L2STR 50 μs after L1STR.

Another control input is REFIN, the refresh clock used in cosmic mode. It is designed to prevent events during refreshes. It is treated as PAUSE REQUEST. In fact, it is a general purpose inhibit input. The

GREF output to the ROCs, is a copy of this signal. REFIN must be enabled by a special mode bit and is ignored in test mode.

I.C.3 TRIGGER LOGIC INTERFACE.

The Trigger Logic informations are: LVL1, LVL2, TMT and TRIGGER MASK.

LVL1 and LVL2 are the Trigger Logic decisions for level 1 and 2. They are sampled at L1STR and L2STR.

TMT, the random event indicator, is sampled at EGBX to produce MT.

The 32 bits of TRIGGER MASK are sampled at L2YES for transmission to the STR501.

I.C.4 STR501 INTERFACE.

The TS is a slave of the STR501. It can activate the interrupt line on the STR501 bus when it needs attention. It communicates informations to the STR501 and receives controls through 14 registers.

I.C.4.a Interrupts

The TS may interrupt the STR501 when a good event has been recognized (i.e. when L2YES is generated). The STR501 has then to perform the FASTBUS broadcast defined in DATACQ 85-21. The TS may also interrupt the STR501 when an error is detected. The last class of interrupts is counter overflows: To simplify the TS, the counters are only 16 bits wide. This is insufficient to record all the BX of a run. The extra bits needed are implemented in software in the STR501. The counters are designed to allow accurate counting in this split implementation.

I.C.4.b Interrupts control

There are 13 individual interrupts sources. Each one has its own status bit, set when the condition occurs and reset by the STR501. Each source have also an enable bit. The enable register has the same layout as the status register.

An overall status, the Major status, is the OR of the enabled status. There is also an overall enable. If the Major status is on and enabled, then an interrupt is sent to the STR501.

I.C.4.c Registers

The TS/STR501 interface contains 14 registers located on long words addresses starting at XX0000Y0, where XX can be 00 to FF, and Y can be 0,4,8 or C. These 10 bits are selected with internal switches. These registers are accessible in User Data space and/or in Supervisor Data space, according to the setting of a 3 positions strap (User only, Supervisor only or both). These registers are described in the next chapter.

I.D Miscellaneous

I.D.1 MECHANICS

I.D.1.a Size

The TS is implemented in FASTBUS mechanics. It is one slot width.

I.D.1.b Front panel

The front panel contains 36 leds and 4 connectors.

I.D.1.b.1 Front panel Leds

The leds are divided in 24 indicators and a dead-time scale (12 leds). The indicators are: +5V, EVENT, HOLD, IT (major status bit), BXIN, EBX, L1STR, L2STR, LVL1, LVL2, L1NO, L1YES, L2NO, L2YES, GBX, EGBX, BUSY, GBXACK, AUTO (automatic mode enabled), PAUSE REQUEST, Protocol violation, STOP, RUN and ACQ (from EGBX to end of BUSY).

The four timing signals (BXIN, EBX, L1STR, L2STR) are conditioned by a flicker circuit to give a feeling of the frequency. The other indicators use unconditioned signals. The $\overline{\text{READY}}$ bar graph represents a dead-time of 10% (resp. 20%, 50%) as a string of 5 (resp. 8, 12) leds

I.D.1.b.2 Front panel connectors

- A DIN 96 pins, for connection to the STR501. Its position and pin definition matches the STR501 specifications.
- A 3M 34 pins, for cables to the FIO-BOXes and ROCs. This connector has been defined in DATACQ 85-21, and is reproduced in section III.A.3
- A 3M 20 pins, for control and timing signals from the Trigger Logic, described in section III.C.2
- A BERG 6 pins, for signals from the Timing Unit, described in section III.B.3

I.D.1.c Rear connectors

The rear of the TS contains two FASTBUS connectors:

- The auxiliary one (130 pins) used with an auxiliary card containing two 3M 34 pins connectors. These are used to input the TRIGGER MASK from the Trigger Logic, one 16 bits word on each cable. These connectors are described in section III.C.3
- The main FASTBUS connector is used only for power supplies.

I.D.2 ELECTRICAL

- The connection to STR501 is equipped with F series TTL drivers/receivers. These chips are located as close as possible to the DIN connector, to reduce track lengths.
- All other signals are transmitted on pairs, with differential ECL levels, terminated through 50 Ω to -2 Volts, according to standard IEC 912.
- The fast logic is implemented in ECL 100K, giving a transit time BXIN to BX/GBX of 5 ns.
- The remaining logic is implemented with programmable PALs.

REGISTERS DESCRIPTION

II.1 INTERRUPT STATUS REGISTER

Address: 0
Read At any time.
Write: At any time.
Set: Status bits are set by the TS logic.
Clear: At initialization.
The status bits are:

Major Status bit 31 is on when at least one of the other status is on and enabled. An interrupt request is transmitted to the STR501 when the Major status is on and enabled.

EVENT bit 30 is set when L2YES is generated.

HOLDint bit 28 is set when HOLD (the output line and the bit 31 of **Hold Status Register**).is going up. This bit can be cleared at any time. Clearing of this bit is necessary, but not sufficient, to remove the HOLD condition.

Errors bits 21 to 29 are set when the corresponding error occurs.

Bit	Error
21	Time-out GBX/GBXACK
22	Time-out EGBX/BXIN
23	Time-out L1NO/ $\overline{\text{BUSY}}$
24	Time-out GBX/L1STR
25	Time-out L2NO/ $\overline{\text{BUSY}}$
26	Time-out L1YES/L2STR
27	Time-out on BUSY
28	HOLD
29	Protocol Violation

Overflows bits 16 to 19 are set when the corresponding counter overflows

Bit	Overflow
16	BX on Pause counter
17	BX on BUSY counter
18	Gated BX counter
19	L1YES counter

The Major Status bit is read-only. But one can write the other status bits, writing a 0 has no effect, writing a 1 clears the corresponding status bit.

II.2 INTERRUPT CONTROL REGISTER

Address: 4
Read: At any time.
Write: At any time.
Clear: At initialization.

Each bit in this register is the enable of the corresponding bit in the **Interrupt Status Register**. When some status are set, writing an adequate pattern in this register may turn on or off the interrupt request to the STR501.

II.3 TRIGGER MASK REGISTER

Address: 8
Read: At any time.
Write: Only in test mode, see **Test Mode Register.**
Set: At the on transition of L2YES.

This register is loaded, when L2YES is set, with the content of the TRIGGER MASK from the Trigger Logic, except in Trigger Bypass Mode. Loading of this register has priority over writing, i.e. a read during L2STR may produce unpredictable results. The content of this register is unpredictable after a power-up.

This register is not cleared by initialization.

II.4 HOLD STATUS REGISTER

Address: C
Read: At any time.
Write: Never, read-only register.
Set: Continuously, except when HOLD is on.

This register contains the state of the lines between the TS and the ROCs, and also of the main lines between the TS and the Trigger Logic. It contains the current state only when HOLD is off.

When HOLD is on, the TS is frozen, this register contains the state at the time of the on transition of HOLD. This can only differ from the current state on the input bits (BUSY, GBXACK, PAUSE REQUEST, LVL1, LVL2). To clear HOLD (the output level and consequently bit 31), on has **both** to remove the cause of HOLD and to clear bit 28 of the **Interrupt Status Register**

This register is not cleared by initialization, but all outputs of the TS are cleared by initialization: only input bits can be set.

II.5 GATED BX COUNTER

Address: 10
Read: At any time.
Write: Never, read-only register.
Counting: When the RUN bit is set in the **Main Control Register**, and also in Test Counters mode.
Clear: At initialization, and by setting the CLEAR COUNTERS bit in the **Main Control Register** (except in some register test modes).

This counter is incremented when GBX is transmitted to the ROCs and in register test mode.

When EVENT is true, the value read by the STR501 is the value of the counter at the on transition of EVENT, but the counter remains active. This feature is implemented for the 4 read-only counters.

II.6 L1YES COUNTER

Address: 14
Read: At any time.
Write: Never, read-only register.
Counting: same as **Gated BX Counter**.
Clear: same as **Gated BX Counter**.

This counter is incremented when L1YES is transmitted to the FIO-BOXes.

II.7 BX ON BUSY COUNTER

Address: 18
Read: At any time.
Write: Never, read-only register.
Counting: same as **Gated BX Counter**.
Clear: same as **Gated BX Counter**.

This counter is incremented when BX is generated when BUSY is true.

II.8 BX ON PAUSE COUNTER

Address: 1C
Read: At any time.
Write: Never, read-only register.
Counting: same as **Gated BX Counter**.
Clear: same as **Gated BX Counter**.

This counter is incremented when BX is generated while BUSY is false and either the TS is paused (by PAUSE REQUEST or by REFIN) or EVENT is true.

The first case counts the duration of pauses (i.e. refreshes), while the second one corresponds to a slow response of the STR501 to an EVENT interrupt. In normal operations this counter should stay at zero. In any case, the sum of the three BX counters gave the total number of valid BX produced by the TS, this should be equal to the number of BXIN received by the TS, if the EBX are correctly generated.

II.9 BUSY TIME REGISTER

Address: 20
Read: At any time.
Write: Only in test mode, see **Test Mode Register**.
Set: After a L2YES, when BUSY + EVENT becomes false.

This register is loaded from the **BUSY Time Counter** at the end of a read-out sequence. Thus, this register contains the duration of the previous read-out sequence, with a resolution of 10 μs. Loading of this register has priority over writing, i.e. a read during the end-of-busy, may produce unpredictable results.

II.10 BUSY TIME COUNTER

Address: 24
Read: At any time.
Write: Only in test mode, see **Test Mode Register**.
Clear: At initialization and when GBX becomes true.
Start of count: When GBXACK becomes true.
End of count: When BUSY becomes false.

This counter is incremented by a 100 KHz clock (or 2 MHz in test register mode). It contains, with a resolution of 10 μs, the duration of the BUSY signal, for each GBX. The overflow of this counter, after about 650 ms, produces the BUSY time-out. This counter is incremented even when HOLD is set.

II.11 TEST MODE REGISTER

Address: 28
Read: At any time.
Write: Only when RUN is false.
Clear: At initialization and when RUN is true.

This register is used to place the TS in one of the following internal test modes:

II.11.a Static Mode

In this mode, enabled by setting bits 17-16 to 01, the content of bits 22 to 31 is transferred to the corresponding outputs of the TS,

and so to the FIO-BOXes and ROCs. This allows to check the transmission of the signals to the FIO-BOXes, especially the operation of HOLD This also provides a way to generate the TS interrupt by software. If HOLD is set in this way, it has to be cleared by writing **both** in this register and in the **Interrupt Status Register.**

II.11.b Time-out Tests

When one wants to check the operation of a watch-dog, one enable this test mode by setting bits 17-16 to 10, and one selects, with bits 21-19, one of the six time-outs. When the TEST bit in the **Main Control Register** is set, the selected time-out counter runs until it produces the time-out. Then the TEST bit is reset.

The meaning of bits 21-19 is:

Bits	Time-out selected
101	GBX to GBXACK
011	EGBX to BXIN
110	L1NO to $\overline{\text{BUSY}}$
001	GBX to L1STR
010	L2NO to $\overline{\text{BUSY}}$
100	L1YES to L2STR

The BUSY time-out is tested with the counter test and not with this mode.

II.11.c Registers Test

In this mode, enabled by setting bits 17-16 to 11, one can write in the registers which are protected in normal operations (**Trigger Mask Register**, **BUSY Time Counter** and **BUSY Time Register**).

When the TEST bit in the **Main Control Register** is set, the test counters procedure runs: the read-only counters and the **BUSY Time Counter**.are incremented by a 2 MHz clock, until the overflow of the **BUSY Time Counter**. Then, the TEST bit is reset. Remark that the overflow of the **BUSY Time Counter** produces a BUSY time-out. The overflows of the read-only counters are treated in the same way as in normal operations.

In order to allow the checking of the counter overflow logic, it is possible to get different values in the read-only counters by using the clear counter inhibit feature: the CLEAR COUNTER bit in the **Main Control Register** is ignored, in this mode, for the read-only registers corresponding to the bits 18-21 which are set.

Bit	Register
21	L1YES counter
20	Gated BX counter
19	BX on BUSY counter
18	BX on Pause counter

II.12 SPECIAL MODES REGISTER

Address: 2C
Read: At any time.
Write: At any time.
Clear: At initialization.

This register is used to place the TS in the following special modes:

II.12.a Automatic Mode

This mode is enabled by bit 31. In this mode, BUSY/GBXACK are replaced by one internal signal beginning 2 μs after GBX, and ending either 10 μs after L1NO, 40 μs after L2NO or 60 μs after L2YES.

II.12.b Trigger Bypass Mode

This mode is enabled by bit 27. The model used for simulating LVL1, LVL2 and TMT is in bits 24 to 26. The loading of the **Trigger Mask Register** is suppressed.

II.12.c Timing Bypass Mode

This mode is enabled by bit 22. The bypassed signals are defined by bits 20 and 21:

Bits 22 21 20	Enabled external Timing signals	Timing signals internally generated by TS
1 0 0	no	EBX, BX, L1STR, L2STR
1 0 1	EBX	BX, L1STR, L2STR
1 1 0	EBX, BX	L1STR, L2STR
1 1 1	EBX, BX, L1STR	L2STR
0 x x	EBX, BX, L1STR, L2STR	no

When bits 22,21,20 have a value of 1,0,0 (i.e. no external signals enabled), a timing sequence (EBX, BX, L1STR, L2STR) is generated when the TRIGGER bit in the **Main Control Register** is set. The TRIGGER bit is reset at the end of the requested sequence.

When bits 22,21,20 have a value of 1,0,1 (i.e. only EBX enabled), a BX is generated 2 μs after each EBX, except during GBX.

This mode can be changed at any time, even during read-out. This may be useful to recover from STOP hang-ups.

II.12.d Refresh enable Mode

This mode is enabled by bit 23. When this bit is set, REFIN is used in READY and the GREF output is enabled. When this bit is reset, REFIN is ignored.

II.13 HOLD CONTROL REGISTER

Address: 30
Read: At any time.
Write: At any time.
Clear: At initialization.

This register contains HOLD enable bits for protocol violation and for the seven time-outs. When at least one of these errors is on (in the **Interrupt Status Register**) and enabled, then the HOLD level is asserted and the HOLD bits (bit 31 of **HOLD Status Register** and bit 28 of **Interrupt Status Register**) are set. This freeze the TS in its current state.

To remove the cause of HOLD one can either reset the corresponding HOLD enable bit, or correct the error and clear the status in the **Interrupt Status Register.** To remove HOLD one has to remove the cause and to clear bit 28 of the **Interrupt Status Register**. If one reset first bit 28 of the **Interrupt Status Register**, HOLD will be reset by removing the cause, conversely if one remove the cause first, then resetting of bit 28 of the **Interrupt Status Register** will clear HOLD output and bit 31 of **HOLD Status Register** and bit 28 of **Interrupt Status Register**.

II.14 MAIN CONTROL REGISTER

Address: 34
Read: At any time.
Write: At any time.
Set: Control bits are cleared by the TS logic.
Clear: At initialization.

This register contains one read-only status bit, RUN to indicate the normal operations of the TS. and six control bits:

START	Enable the normal operations of the TS.
STOP	Stop the normal operations of the TS.
INIT	Perform the same reset as power-up.
CLEAR COUNTERS	Clears the four read-only counters, except in some register test modes.
TRIGGER	Perform a sequence of timing signals, in complete timing bypass mode.
TEST	Perform the test sequence defined by the current configuration of the **Test Mode Register.**

One can write these control bits, writing a 0 has no effects. Writing a 1 executes the operation only if the TS is in the proper state. If it is not, then the operation is not executed and there is no warning. These bits are reset automatically by the TS at the end of the requested operation.

The RUN bit is set by setting START and reset by setting STOP. The START and STOP bits remains on while RUN is not in the requested state. The RUN bit must be reset to allow Test Modes.

If one set STOP while the TS was generating read-out signals, then the cycle completes in automatic mode (see II.12.a) and then the RUN and STOP bits are reset in the register. Stopping the TS, while HOLD is on, imply first a removal of the HOLD condition. If the timing is external, the stopping of the TS may fail (with a time-out error) if a requested timing signal is absent or missed (i.e. because of an HOLD condition). In that case, one has either to reset the TS with INIT, or to switch to internal timing.

INTERFACES DESCRIPTION

III.A Interface with ROCs and FIO-BOXes

The complete list of levels is now: BUSY, GBXACK and PAUSE REQUEST as input, BX, EGBX, GBX, L1NO, L1YES, L2NO, L2YES, HOLD, MT, READY and GREF as output.

III.A.1 LEVEL CONDITIONS

BX

BX is a copy of the BXIN received from the Timing Unit, filtered: i.e. BX is transmitted only if BXIN is preceded by an EBX. BX are transmitted regardless of the state of HOLD.

EGBX

EGBX is started by EBX when READY . $\overline{\text{HOLD}}$ is true. EGBX is maintained until GBX.

GBX

GBX is started by BXIN when EGBX . $\overline{\text{HOLD}}$ is true. GBX is maintained until GBXACK + $\overline{\text{HOLD}}$.

L1NO

L1NO is started by L1STR when GBXACK . $\overline{\text{LVL1}}$. $\overline{\text{HOLD}}$ is true. L1NO is maintained until the end of BUSY + $\overline{\text{HOLD}}$.

L1YES

L1YES is started by L1STR when GBXACK .LVL1 . $\overline{\text{HOLD}}$ is true. L1YES is maintained until the end of BUSY + $\overline{\text{HOLD}}$.

L2YES/L2NO

L2YES or L2NO is started by L2STR, according to the value of LVL2, when L1YES . $\overline{\text{HOLD}}$ is true. L2NO and L2YES are maintained until the end of BUSY + $\overline{\text{HOLD}}$.

MT

MT is started by EBX, when EGBX is generated, if TMT is on. MT is maintained until GBXACK + $\overline{\text{HOLD}}$.

READY

READY is RUN . $\overline{\text{BUSY}}$. $\overline{\text{EVENT}}$. $\overline{\text{pause}}$
with pause = PAUSE REQUEST + REFIN . 2C<23>.

GREF

GREF is REFIN . 2C<23> . RUN . $\overline{\text{HOLD}}$.

III.A.2 TIMING CHARACTERISTICS

- The delay between BXIN and BX/GBX is less than 5 ns, this delay is exactly the same for the two signals. BX, GBX and EGBX have a jitter less than 1 ns.

- The delay between EBX and EGBX is about 10 ns, it has a jitter less than 2 ns.

- The delay between L1STR and L1YES/L1NO and between L2STR and L2YES/L2NO is about 50 ns, it has a jitter less than 5 ns.

- The signals coming from the ROCs (BUSY, GBXACK and PAUSE REQUEST) are filtered to remove transient states of less than 100 ns. This filtering introduces a delay of 200 ns in the recognition of transitions.

III.A.3 CONNECTOR DESCRIPTION

Signal	+ pin	-	
BX	1	2	out
GBX	3	4	out
L1NO	5	6	out
L1YES	7	8	out
L2NO	9	10	out
L2YES	11	12	out
EGBX	13	14	out
MT	15	16	out
SD spec.	17	18	
SD.spec.	19	20	
Reserved	21	22	
READY	23	24	out
GREF	25	26	out
PAUSE REQUEST	27	28	in
GBXACK	29	30	in
BUSY	31	32	in
HOLD	33	34	out

III.B Interface with Timing Unit

III.B.1 TIMING REQUIREMENTS

There are four timing signals: EBX, BXIN, L1STR and L2STR, in that sequence.

The timing signals must be pulses of about 100 ns. The timing information is contained in the rising edge of the pulses.

III.B.1.a Standard Timing

The normal delays are:

EBX to BXIN	2 µs	time-out at	4 µs
BXIN to L1STR	5 µs		10 µs
L1STR to L2STR	50 µs		60 µs

These normal delays are used when the TS is in Timing Bypass Mode.

III.B.1.b Cosmic mode timing

In cosmic mode, the delay of BXIN has to be as short as possible. The delay EBX-BXIN cannot be reduced below 150 ns because EGBX needs a minimum width. If BXIN is produced by delaying EBX, it is possible to have an accidental coincidence of EBX and BXIN. The definition of EGBX and GBX is such that this coincidence may produce an hang-up of the TS. The Timing Unit should prevent these coincidences.

III.B.2 VALIDATION OF TIMING SIGNALS

Timing signals are expected by the TS as follow:

BX is expected after EBX.
L1STR is expected after GBXACK.
L2STR is expected after L1YES.

Timing signals may be present when these conditions are not meet. The TS has chosen to ignore unexpected timing signals. On the other hand, a missing timing signal will trigger a watchdog and produce a time-out error.

III.B.3 CONNECTOR DESCRIPTION

The BERG connector on the front panel has three pairs:

top EBX
middle BXIN
bottom REFIN

III.C Interface with Trigger Logic

III.C.1 TIMING REQUIREMENTS

LVL1

This line must be stable at least 50 ns before L1STR, and stay at least until the end of L1STR.

LVL2

This line must be stable at least 50 ns before L2STR, and stay at least until the end of L2STR.

TRIGGER MASK

These lines must be stable at least 50 ns before L2STR, and stay at least until the end of L2STR.

TMT

This line must be stable at least 100 ns before EGBX, and stay at least until GBX.

III.C.2 FRONT-PANEL CONNECTOR DESCRIPTION

The 20 pins, 3M connector houses 8 pairs as follow:

+ pin	-		
1	2	L1STR	in
3	4	LVL1	in
5	6	L2STR	in
7	8	LVL2	in
9	10	empty	
11	12	empty	
13	14	TMT	in
15	16	EGBX	out
17	18	GBX	out
19	20	BX	out

III.C.3 REAR CONNECTORS DESCRIPTION

III.C.3.a FASTBUS connector

Trigger Mask line	+ pin	-
TM 0	A00	B00
TM 1	A01	B01
TM 2	A02	B02
TM 3	A03	B03
TM 4	A04	B04
....	.....	.....
....	.....	.....
....	.....	.....
TM 27	A27	B27
TM 28	A28	B28
TM 29	A29	B29
TM 30	A30	B30
TM 31	A31	B31

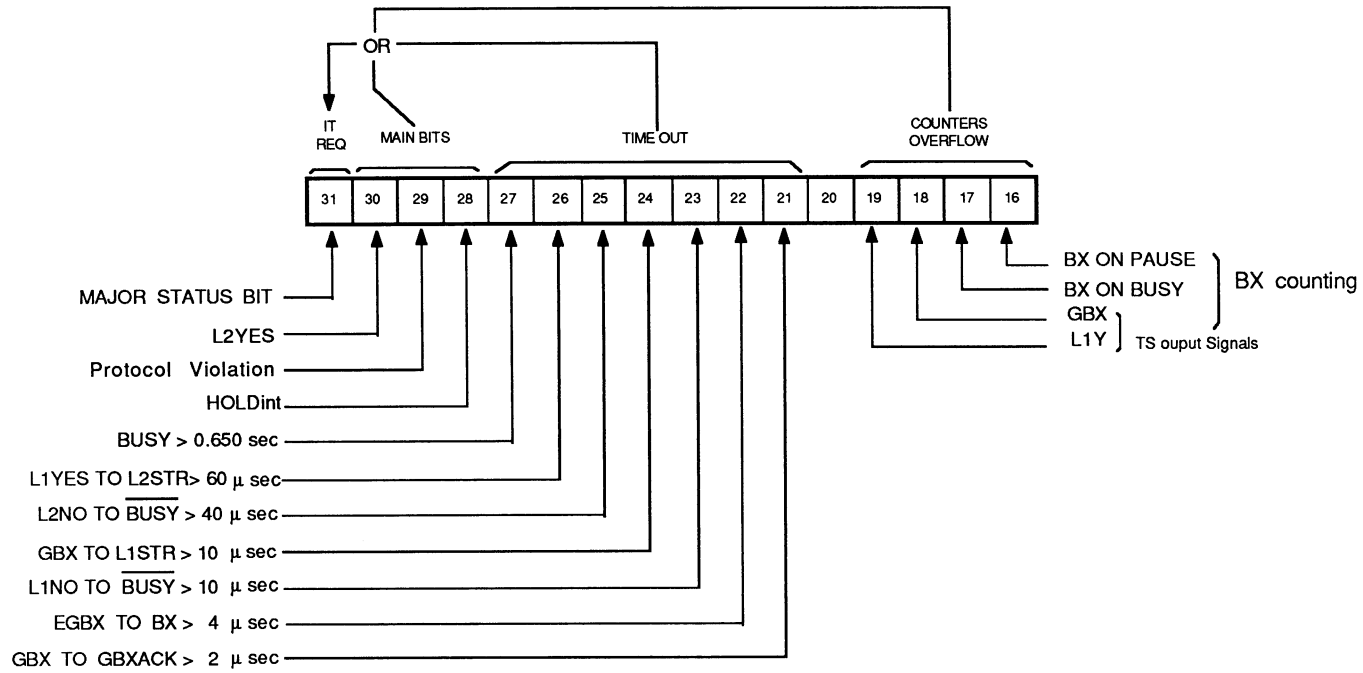
III.C.3.b 3M connector 1, 34 pins

Trigger Mask line	+ pin -
TM 0	1 2
TM 1	3 4
TM 2	5 6
TM 3	7 8
....	....
....	....
....	....
TM13	27 28
TM14	29 30
TM15	31 32
free	33 34

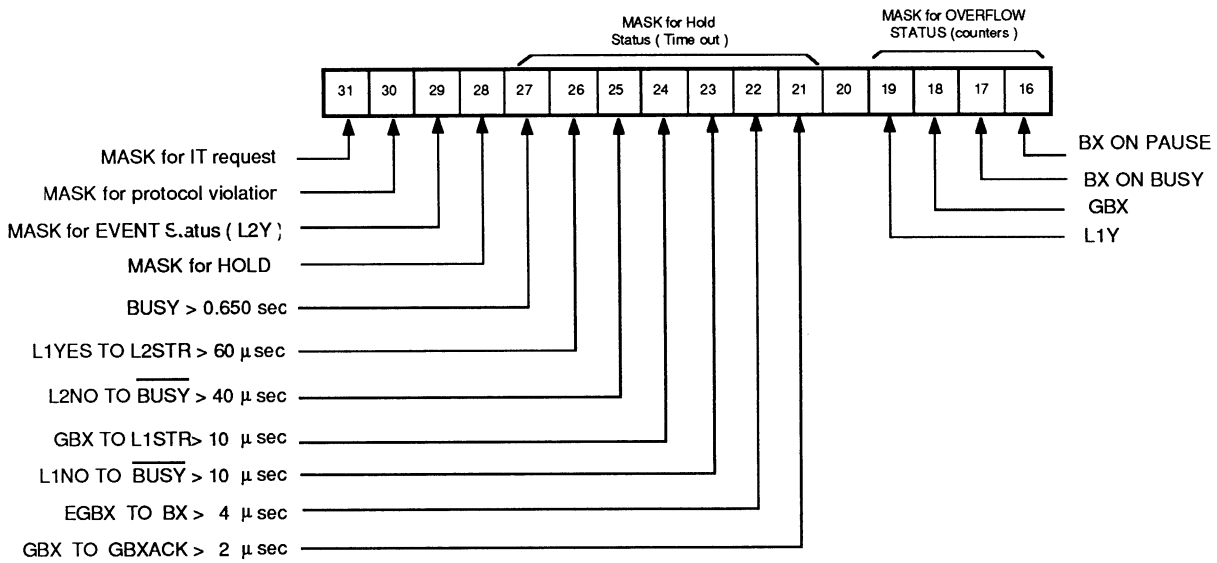
III.C.3.c 3M connector 2, 34 pins

Trigger Mask line	+ pin -
TM16	1 2
TM17	3 4
TM18	5 6
TM19	7 8
....	....
....	....
....	....
TM29	27 28
TM30	29 30
TM31	31 32
free	33 34

INTERRUPT STATUS REGISTER (Addr XX000000)



INTERRUPT CONTROL REGISTER (Addr XX000004)

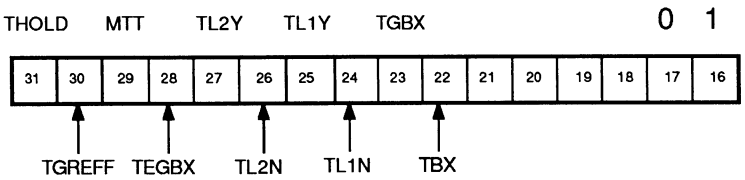


MASK BIT SET : Enable corresponding IT Request

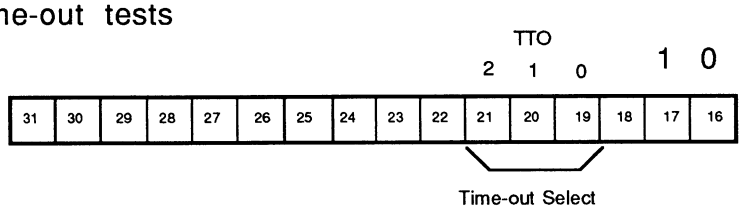
BIT 31 RESET : Disable Status bit 31 and IT Request

TEST MODE REGISTER Address XX000028

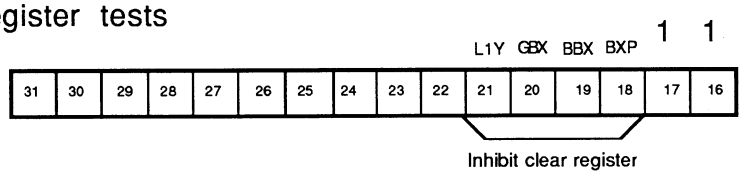
Static tests



Time-out tests

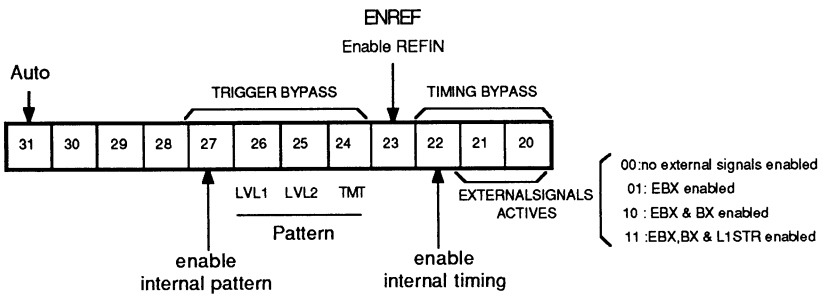


Register tests

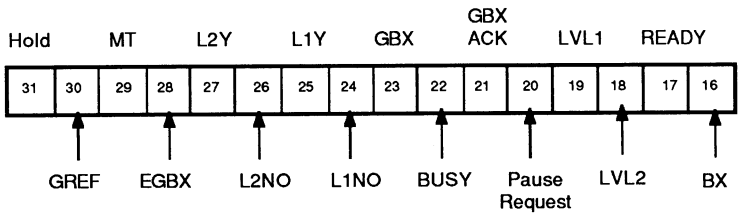


Note : All bits Reset when RUN bit Set in TS CONTROL REGISTER

SPECIAL MODES REGISTER Address XX00002C

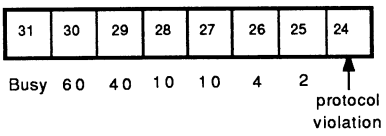


HOLD STATUS REGISTER Address XX00000C (Read only)

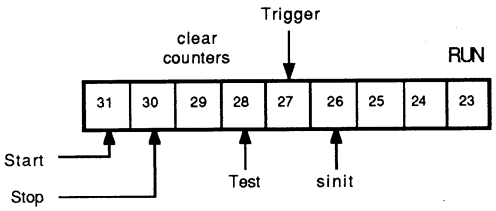


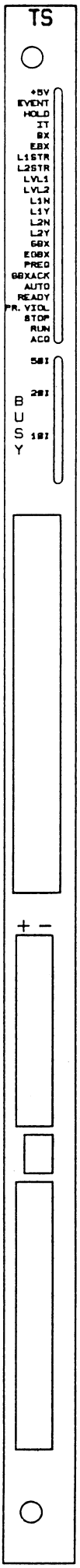
TRANSPARENT LATCHES if HOLD FALSE
RETAIN DATA when HOLD TRUE

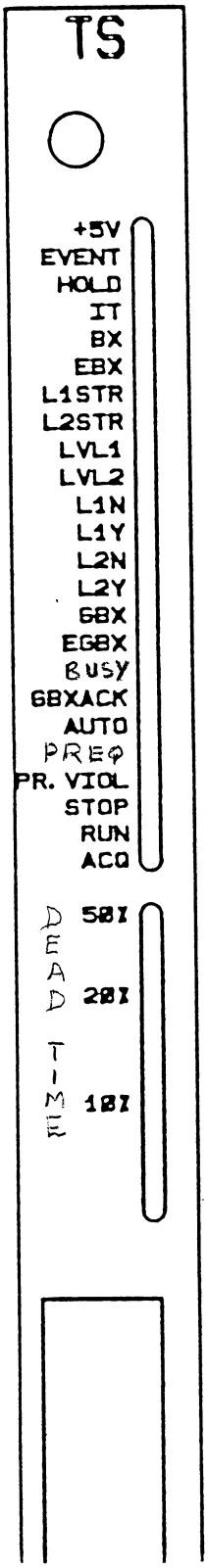
HOLD CONTROL REGISTER Address XX000030



MAIN CONTROL REGISTER Address XX000034

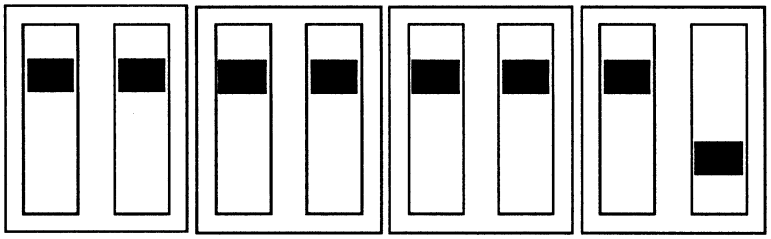



TS
+5V
EVENT
HOLD
IT
BX
EBX
L1STR
L2STR
LVL1
LVL2
L1N
L1Y
L2N
L2Y
GBX
EGBX
PREQ
GBXACK
AUTO
READY
PR. VIOL
STOP
RUN
ACQ
BUSY
50I
20I
10I
+ −


TS
+5V
EVENT
HOLD
IT
BX
EBX
L1STR
L2STR
LVL1
LVL2
L1N
L1Y
L2N
L2Y
GBX
EGBX
BUSY
GBXACK
AUTO
PREQ
PR. VIOL
STOP
RUN
ACQ
DEAD TIME
50I
20I
10I

PROTOTYPES ONLY

DIP SWITCHES MEANING



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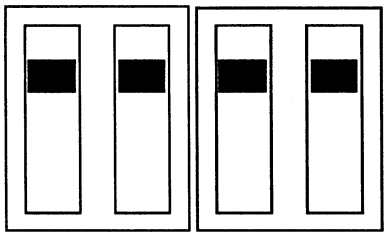
AD 28 29 30 31 24 25 26 27



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AD 6 7