ALEPH 86-10
20.1.86 Distr. TPC

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THE TPC CALIBRATION SYSTEM

The hardware for the TPC calibration system will be described.

1.0 Introduction

The analog electronics for the TPC will be constructed from components with highly accurate values. In the ideal case, the response of all the electronic channels to a given quantity of charge would be identical. However, in reality, a certain amount of fluctuation in component values will always exist. Each electronic channel will have its own characteristic response to an input source. The crucial signal to noise ratio will also differ from channel to channel since the majority of noise electrons will be generated within the electronic channel itself.

The variations in performance of different channels, if left unaccounted for, will lead directly to a worsening of spatial resolution in the TPC. Recall that the r-ϕ coordinate will be measured by taking ratios of pulse heights from adjacent pads. If the responses of the electronics of these pads are not known exactly, an uncertainty will be created in the pulse height measurements and therefore the r-ϕ coordinate. For example, recall the two pad algorithm :

$$\phi = (\phi_1 + \phi_2)/2 + \sigma^2 \cdot \ln(P_1/P_2) \; / \; [R^2 \cdot (\phi_1 - \phi_2)].$$

The uncertainty in r-ϕ will then be

$$\Delta(r\phi) = \sigma^2/[\phi_1 - \phi_2] \cdot \sqrt{(\Delta P_1/P_1)^2 + (\Delta P_2/P_2)^2}.$$

If the relative uncertainty in the pulse height measurement is 5%, the resulting coordinate uncertainty in the TPC, with typical values of $R \cdot (\phi_1 - \phi_2) = .67$ cm and $\sigma = .32$mm will be 108μm. The pre-amplifier and shaping amplifier together will have 16 passive components (resistors and capacitors). If the value of each component has an error of 2%, the subsequent coordinate error will be 90 μm [1]. These errors are not acceptable and must therefore be corrected for.

A calibration system to measure the response of individual channels to a given input will be necessary to ensure good spatial resolution in

the TPC. Since the pre-amplifiers will be charge sensitive devices, the method chosen to calibrate the electronics will be to inject a common amount of charge into the pre-amplifiers. By measuring the corresponding responses, the relative gains of the electronic channels can be determined. Calibration constants will be calculated from the calibration data and will be used to normalize the responses of all the channels. Pulse heights originating from tracks in the chamber will be corrected using the calibration constants. This type of calibration procedure described above will be called the "gain calibration."

A system to calibrate the electronics for the ALEPH TPC has been designed, built and tested. The primary function for the system will be to perform the gain calibration for cathode pad and sense wire channels. The electronics will be calibrated by voltage test pulses that are converted to charges through a given capacitance. The amplitude, phase and distribution of test pulses will be controlled through computers connected to the TPC FASTBUS system.

The phase of a pulse refers to the arrival time of the pulse at the electronics with respect to the digitizer clocks. If necessary, the errors associated with asynchronous sampling could be corrected by a "phase calibration." The test pulse would be injected into the pre-amplifiers at set phase differences with respect to the digitizer clocks.

The calibration system will also be used as a debug tool. The ability to control the distribution of test pulses enables the system to easily find defective channels. A test pulse will also have the

capability to pulse at various points along a given electronics chain. The source of breakdown can then also be easily discovered.

2.0 Calibration System Overview [2]

The hardware for the calibration system consists of two modules for each TPC sector. One module lies in a FASTBUS bin and is called the Sector Test Pulser Controller (STPC), while the second is mounted directly on the sector and is called the Sector Controller (SC).

The STPC provides all interactions and controls necessary to activate the electronics involved in a calibration operation. The on-line computer system initiates any given calibration procedure. All relevant information such as type of calibration, phase and calibration pulse amplitude is sent to the STPC via FASTBUS. The STPC in turn activates the internal hardware function demanded by the computer. Three areas are controlled by the STPC :

1) The sector pre-amplifier power is turned on or off by a designated register in the STPC. This enables the pre-amplifier DC power to be turned off when the sector cooling system is not operational. This feature is useful for quick de-bug operations.

2) A test pulse of variable amplitude can be sent directly to the shaping amplifiers in the TPD's. This pulse is used to isolate a defect in a faulty electronic channel. A total of 25 linear buffers distribute the common test pulse to each TPD module. The DAC's, buffer drivers and all circuitry to form these test pulses are mounted directly on the STPC. The pulses will be that of a step function with a maximum amplitude of 5 volt. The output impedance from the pulser will be 10 ohms.

3) The pulsing to calibrate the pad wire pre-amplifiers is controlled through the STPC. However, the actual pulses are formed and distributed by circuitry on the SC. A 24 bit word is bit serially shifted from the STPC to the SC. These data control a DAC on the SC that determines the amplitude of the test pulses. They also control which drivers will issue test pulses in a given calibration run. In addition, a one bit register on the STPC can turn the DC power in the SC on or off to eliminate power dissipation when the calibration system is not in use.

Block diagrams of the STPC and SC are given in Figures 1 a and b.

3.0 Methods of Test Pulsing

The main purpose of the gain calibration is to measure the relative gains between adjacent pad channels. A critical requirement for this

measurement is that each pre-amplifier is injected with the same amount of charge. The method chosen to accomplish this involves pulsing the field wires which are strung across the pad rows. The common capacitive couplings between the field wires and the pads will ensure that , to an approximation, each pad pre-amplifier sees an identical test charge. A single driver located on the SC will simultaneously pulse all the field wires on a sector. Therefore, all pads in a sector can be calibrated at the same time. A register on the STPC controls a group of FET switches that are connected in series with the AC ground of the field wires. The switches will be opened during calibration pulsing and closed during chamber data taking.

Each pad and wire pre-amplifier will possess a test input equipped with a test pulse coupling capacitor. Another method of calibration is to inject test pulses directly into these capacitors. Four drivers for pads and four drivers for wires are available on the SC to perform this "direct pre-amplifier pulsing." See Figure 2 for the test pulse distribution. Each pad and wire driver will pulse every fourth pre-amplifier input. This enables the calibration system to measure the cross-talk between neighboring channels. This method of direct pre-amplifier pulsing can only be used effectively after the relative values of the coupling capacitors is determined. The results from the field wire pulsing and the direct pulsing can be compared to give these values.

The field wire driver is capable of switching polarity to calibrate either the wire or pad channels. The wire channels will use the field wire driver only as a backup. Difficulties arise in this method for

wires because the sense wires in the sectors will have different lengths. The amount of test charge seen by a wire is then dependent on its length. The primary form of calibration for the wires will be to pulse the pre-amplifiers directly. The values of the test capacitors for the wire channels will be established by comparing the test pulse data with the pulse height spectrum from cosmic ray data.

4.0 Pulse Shapes for the Calibration System

Several pulse shapes have been considered for implementation in the calibration system [3]. A major consideration in choosing a pulse shape was that all associated hardware would be placed on the SC. Minimal electronics would be required to conserve space and power dissipation. The simplest possible test pulse shape would be a step function. This pulse shape, however, would have a different response in the electronics than an actual chamber signal. Software corrections would have to be applied to get the proper normalizations. A signal which mimics a chamber pulse would simplify the overall calibration procedure, but would be more complicated in terms of the circuitry. A preliminary study was undertaken to study the response of the electronics to the two types of input pulses. It was also determined whether a chamber signal could be simulated by a simple function which could be represented by a modest electronic network.

The chamber signal was modeled according to a formula derived for a cylindrical proportional chamber [4]. The integrated charge at time t due to a single electron is given by

$$S = q/[2 \cdot C \cdot \ln(b/a)] \cdot \ln[1 + (2 \cdot V \cdot \mu \cdot t)/(p \cdot a^2 \cdot \ln(b/a))]$$

where (values used are in parentheses)

a = wire radius (1×10^{-5} m)

b = radius of outer wall, est. by using cell size (4×10^{-3} m)

C = electrostatic capacitance of counter (6×10^{-12} f/m)

q = electron charge

V = applied voltage (1500 Volts)

μ = positive ion mobility (1.87×10^{-11} atm-m^2/volt-sec)

p = gas pressure (1 atm)

In Figure 3a, the shape of the chamber input signal to the electronics can be seen to be a logarithm. The input is characterized by a fast rise due to the motion of ions in a high field near the sense wire and a long, slow tail due to ions which drift far from the wire in a low field. The response of the electronics is shown in the same figure.

The step function has the major advantage of being technically simple and is also well suited to uncover defects in an electronics

channel. Unfortunately, the shaper response to such a pulse differs substantially from that of a chamber pulse. See Figure 3b. The main differences are the shift in time of the peak of the shaped pulse and the presence of the undershoot. The shift of the peak will cause the calibration pulse to have a different phase response than a chamber pulse. This problem could be overcome by shifting the phase of the calibration pulse every 10 ns along the output signal until the entire signal is mapped. The disadvantages of this method would be the requirements of more memory, CPU and associated software.

A simulated chamber signal would have circumvented the problems mentioned above. The question was whether this input could be easily produced using simple circuitry. As described before, the chamber pulse was characterized by a fast rise (~50 ns) and a slow, long tail. The function that was used to represent this logarithm was the weighted sum of two exponentials. The first exponential had a small time constant to account for the fast rise while the second exponential had a long time constant to account for the slow logarithmic tail. The functional form is as follows :

$$F(t) = K_1 \cdot (1 - e^{-t/RC_1}) + K_2 \cdot (1 - e^{-t/RC_2})$$

where K_1,K_2,RC_1 and RC_2 are parameters to be fitted.

This parametric equation was fitted to the logarithmic chamber pulse. The result is shown in Figure 3c. This simulated pulse shape

was found to make a reasonable approximation to the input pulse from a proportional wire.

The fitted function can be represented by two simple integrators. The production of a simulated chamber pulse using minimal electronics is shown to be feasible. The prototype calibration system uses a simulated chamber pulse from a $\theta = 90^{\circ}$ (with respect to the beam axis), straight track. This pulse does not take into account effects from Landau fluctuations, diffusion or noise.

A more elaborate Monte Carlo simulation study was undertaken to investigate how these effects alter the pulse shape. The study reviewed whether the present calibration system with a $\theta = 90^{\circ}$ pulse is sufficient to overcome the errors introduced by these effects and adequately calibrate the electronics. The results will be presented in the subsequent note.

5.0 The Sector Test Pulse Controller

The STPC is the interface between FASTBUS and the test pulser. It provides for the reading and writing of seven control registers and additional functions.

5.1 Register 1 (REG1)

Register 1 is a 24-bit register that can be read or written through FASTBUS. In addition, the contents of this register can be transmitted to the SC in bit serial format. The data word written in this register controls the amplitude and the on/off state of 9 test pulse drivers on the SC. The contents of the register can be changed in the following ways

1) Read or write directly from FASTBUS. This is possible only if the secondary address bits <6:4> = 0.

2) Bit serially transfer the contents of the shift register on the SC called the sector control register (SCR) to register 1. The tri-state gates of register 1 are arranged such that the same data are also transmitted back to the SCR. FASTBUS is released immediately after the command to transfer data is issued. In this way, other FASTBUS commands or bus operations can occur during the data transfer (~35 μs). However, if another command is sent to the STPC during data transfer, the command is ignored and a slave status response SS = 1 or "busy" is sent from the STPC to FASTBUS. This type of transfer occurs when the secondary address bits <6:4> = 1.

3) Bit serially transfer the contents of the SCR to REG1 with a delayed read. During the transfer time (~35 μs) the FASTBUS WAIT state is entered. The WAIT (WT) signal has the action of blocking all subsequent timing signals. It freezes the present

state of the bus. At the end of the WAIT, the contents of the SCR ,now in REG1 is put on the FASTBUS AD lines. The secondary address bits are set to <6:4> = 2.

4) Write to REG1 from FASTBUS with an automatic transfer of the data to the SCR. During the transfer, the contents or REG1 and the SCR are exchanged. If a command is written to the STPC during data transfer, the command is ignored and SS = 1 is returned. The secondary address bits <6:4> = 3.

5) Circulate REG1 and the SCR. FASTBUS is released immediately after this command is received by the STPC. This command exchanges the contents of REG1 and the STPC with no direct reads or writes to or from FASTBUS. Once again, any command written to the STPC during data transfer is ignored and the STPC returns SS = 1. This circulation of data is used mainly for maintenance purposes. The secondary address bits <6:4> = 6.

In some of the modes, if the STPC is busy, SS = 1 is returned to FASTBUS. This busy state can also be monitored by reading bit 0 of CSR register 10 (hex). If this bit is true, the transfer of data is in progress.

5.2 Register 2 (REG2)

REG2 is a 3-bit register which is read or written directly from FASTBUS. This register selects a time interval to delay the calibration test pulse with respect to the digitizer clocks. The delays available are multiples (0-7) of 1/8 the length of a digitzer bin (80 ns). Requests for test pulses are issued by the trigger control system synchronous to the digitizer clocks. The test pulses are then issued in a defined time relationship with the digitizers. This permits the calibration to study and , if necessary, calibrate the effects of phase when sampling a pulse.

5.3 Register 3 (REG3)

REG3 is a 1-bit register which controls the FET switches which are connected to the field wires. When REG3 contains a logical 1, the FET switches are opened to provide an AC short to ground for the field wires. This is the normal state for the switches. The FET's are turned off only during calibration procedures. When the switches are off, this allows the test pulses to propagate down the field wires. The status of this register is monitored by reading CSR register 10 (hex).

5.4 Register 4 (REG4)

REG4 is a 1-bit register which controls the on/off state of the DC power for the circuitry on the SC. When the register has a logic 1, the power is "on". This register is used to eliminate the need for a cooling system for the SC. The status of this register can be monitored by reading bit 2 of CSR register 10 (hex).

5.5 Register 5 (REG5)

REG5 is a 1-bit register which controls the on/off state of the DC power for the pre-amplifiers. A logic 1 means that the power is "on." A separate control of pre-amplifier power is useful during installation or maintenance periods when the cooling systems may not be operational. The status of REG5 is reflected by reading bit 3 of CSR register 10 (hex).

5.6 Register 6 (REG6)

REG6 is a 12-bit register written and read directly from FASTBUS. This register is used as the input to a 12-bit DAC that controls the amplitude of test pulses that are input to the shaping amplifiers in the digitizer modules.

5.7 Register 7 (REG7)

REG7 is a 1-bit register which controls the on/off state of the DC power for the drivers which pulse the shaping amplifiers in the TPD's.

5.8 Test Pulse Functions

The STPC has 6 built in functions for test pulsing and maintenance. The action of these functions are closely tied with the capabilities of data register 1. The function desired is chosen by the selection of the proper secondary address read by the STPC. The secondary address bits <6:4> are decoded to provide the following functions :

Decoded Value	Function
0	Normal read/write to data registers 0 through 7
1	Transfer the contents of the SCR to REG1. The SCR is left unchanged.
2	Exchange the contents of the SCR and REG1. A FASTBUS WAIT is invoked until completion of the operation.

3	Write to REG1 through FASTBUS. After the data cycle, exchange the contents of REG1 and the SCR.
4	Circulate the contents of REG1 and the SCR
5	Issue a test pulse via an internal trigger.
6	Write to REG1 through FASTBUS. The FASTBUS WAIT state is invoked during the circulation of data between REG1 and the SCR. The contents of these registers is exchanged. The WAIT state is removed upon completion of the exchange.

6.0 The Sector Controller

The SC is a total slave to the STPC. All actions performed by the SC are a result of signals which come into the cards from the STPC. The 24-bit SCR contains the amplitude and control information needed by the SC. The amplitude of the pulse is controlled by the 12 most significant bits. The test pulse distribution information is contained in the 9 least significant bits. These 9 bits control the on or off state of the field wire driver, the 4 pad drivers and the 4 wire drivers.

A test pulse is started from two choppers. One is for the field wire drivers and the other is for the direct pre-amplifier pulsing

drivers. A digital test pulse (DTP) comes from the STPC to act as a trigger for the pulse circuitry. The DTP triggers the choppers to output a pulse whose amplitude is proportional to the DC level of the DAC. The pulse from the choppers then enters a system of integrators which shapes the pulse that simulates a chamber pulse. The outputs from the field wire driver is fed directly into the field wires. The driver outputs for the direct pre-amplifier pulsing is buffered by drivers cards that distribute the test pulse. There is one driver card per pad row for pads and wires. The driver cards are necessary to minimize the number of pre-amplifiers pulsed by a single driver.

The SC circuitry was checked for linearity, stability and crosstalk between the drivers [5]. The procedures and results are presented below.

the linearity test was conducted by the use of a Silena ADC - multi-channel analyzer (MCA) system. The MCA was first calibrated with a known, precise Ortec pulser and a shaping amplifier which could be reproduce the 250 (0-100%) risetime of the TPC calibration pulser. The signal from the Ortec pulser was found to exhibit perfect linearity over 1000 channels of the MCA. The TPC pulser was then tested for linearity with the MCA. The results are given in Table 1. The pulser was found to be linear to about 1 channel or 1 part per 1000. However, the linearity was probably better since problems with noise and cabling were encountered.

The heat stability of the SC was tested by crude, but effective methods. The SC cards were first placed under a hot lamp to test the overall stability. The linearity and stability of the pulser were

severely affected. The cause of the instability was determined by applying a hot soldering iron to various components on the cards. The problem was due to a heat sensitive diode. This component has since been replaced by a heat compensating device. The DAC and chopper circuitry were stable to within one channel. The individual components on the card were then tested by using copper rods at room temperature and at 0° C. At a difference of 20° C, the DAC, choppers, driver transistors and a set of linear gates were found to shift by at most a channel.

The crosstalk tests were also conducted using the MCA. The crosstalk between the pad and wire drivers was tested directly off the SC and also off the buffer distribution cards both with a long and a short cable. The procedure used was to first find the pedestal by having zero amplitude on the pulser and all drivers switched off. The MCA was connected to only one driver. The monitored driver was then turned on to a low DAC setting with all other drivers turned off. The other three drivers were turned on in succession to low DAC settings to see their relative effects on the monitored driver. The next test consisted of turning off the monitored driver and turn on the other three drivers to full scale. The final test was to turn on the monitored driver to full scale then other three in succession to full scale. The results are shown in Table 2.

It must be mentioned that the expected channel shift for the wire drivers should have been greater than for the pad drivers. Originally, a 10 ohm resistor was placed in front of linear gates to the wire and pad drivers. This resistor was shorted out in the case of the pad gate.

When a driver was turned on, the 10 ohm resistor was put in series with a 10,000 ohm resistance arising from the driver circuitry. Each additional driver turned on would put another 10,000 ohms in parallel with the original 10,000 ohms. So for a single driver, a 1 part per 1000 attenuation was expected. For two drivers, a 1 part per 500 and so forth. This attenuation effect should be considered when reviewing the results of the crosstalk measurements. This effect was eventually reduced to less than 1:1000 by reducing the value of this resistor from 10 ohms to 2.7 ohms.

7.0 Calibration Test Software

A computer program to communicate with the STPC was written for de-bugging, testing and operating the TPC calibration system. A full de-bug facility was written with "scope loops" or the ability to execute the same hardware function a given number of times. The program was designed to test all functions and operations of all registers. It was used to de-bug the hardware to the one chip level.

The software also has the ability to pulse the field wires and directly pulse the pre-amplifiers and TPD's using both an external or an internal trigger.

The final software to operate the calibration system is still under development and is dependent upon the completion of the TPD and the TPP.

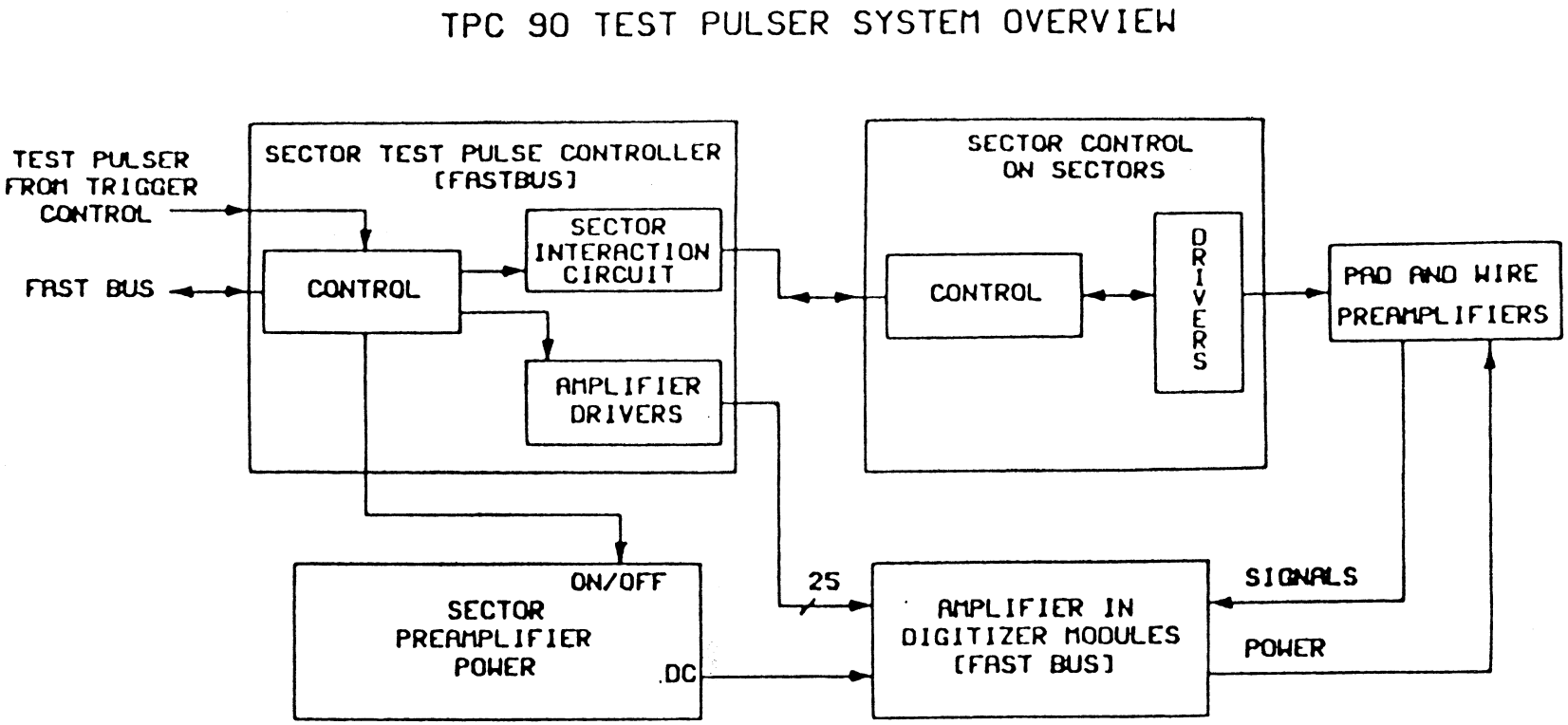
Table 1 Linearity Results

(Average over 5 runs, approx. 15,000 events per DAC setting)

DAC Setting	MCA Channel
Full Scale	963
	853
	742
(Intevals	631
of 512)	520
	409
	299
	189

Table 2 Crosstalk Results : The shift in Number of MCA Channels

Monitored Channel	Pad (Main Board)	Wire (Main Board)	Pad 1 (Buffer card long cable)	Pad 2 (Buffer card Long cable)	Pad 1 (Buffer Card Short cable)	Pad 2 (Buffer card Short cable)	Wire (Buffer Car Short cabl
Turn on Monitored Driver to 0 ampl.	1	1	1	1	1	1	1
Monitored driver at 0 ampl. Turn on other 3 drivers to 0 ampl.	1 (1:4000)	1	1	1	1	1	0
Monitored driver off. Turn on other 3 drivers to full ampl.	1 (1:4000)	1 (1:4000)	2 (1:2000)	3 (1:1333)	3 (1:1333)	2 (1:2000)	1 (1:4000)
Monitored driver on full ampl. Turn on other 3 drivers to full ampl.	1 (1:1000)	2 (1:500)	3 (1:333)	3 (1:333)	2 (1:500)	1 (1:1000)	3 (1:133)



Figures 1a and b

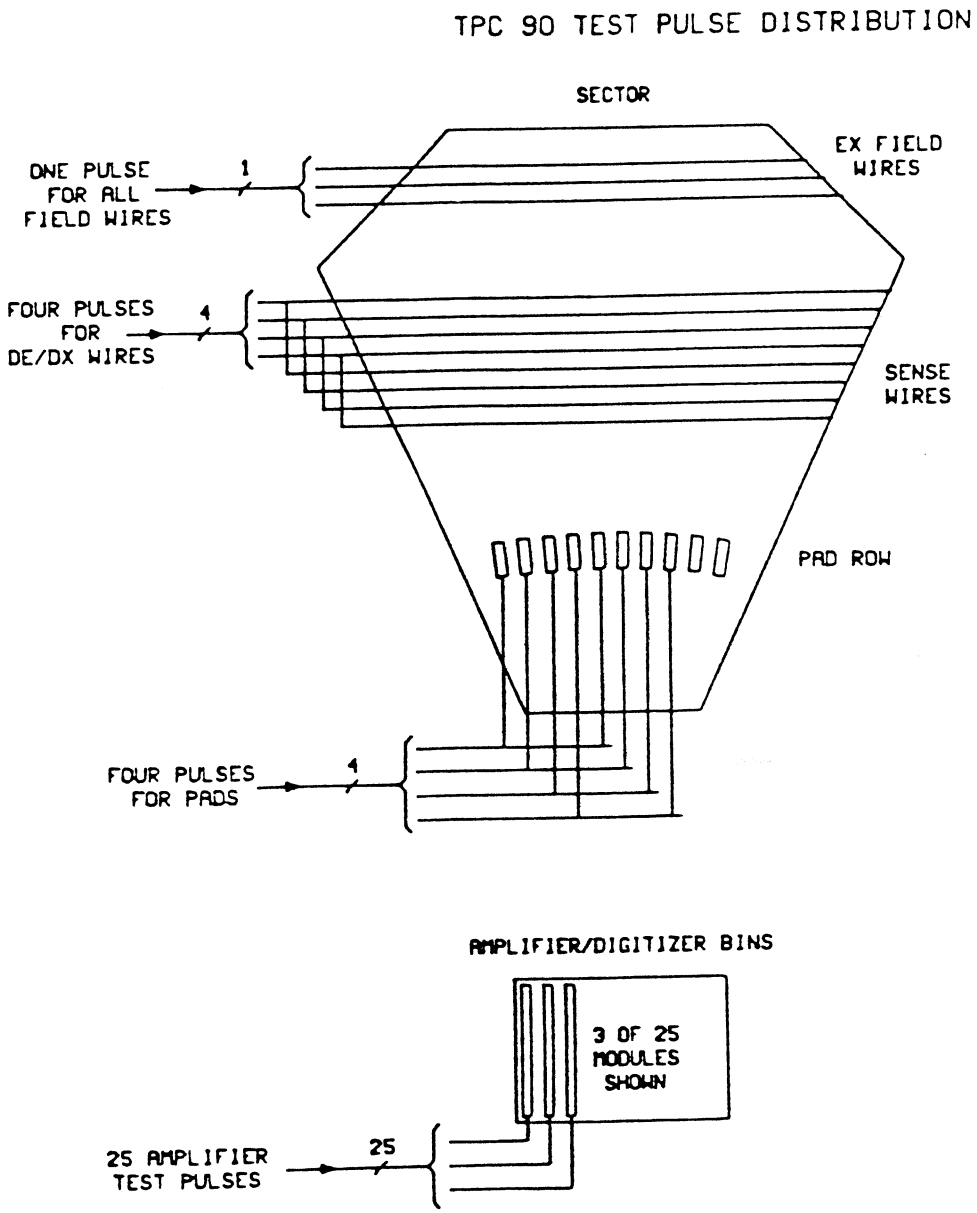

TPC 90 TEST PULSE DISTRIBUTION
SECTOR
EX FIELD WIRES
ONE PULSE FOR ALL FIELD WIRES
1
FOUR PULSES FOR DE/DX WIRES
4
SENSE WIRES
PAD ROW
FOUR PULSES FOR PADS
4
AMPLIFIER/DIGITIZER BINS
3 OF 25 MODULES SHOWN
25 AMPLIFIER TEST PULSES
25

Figure 2

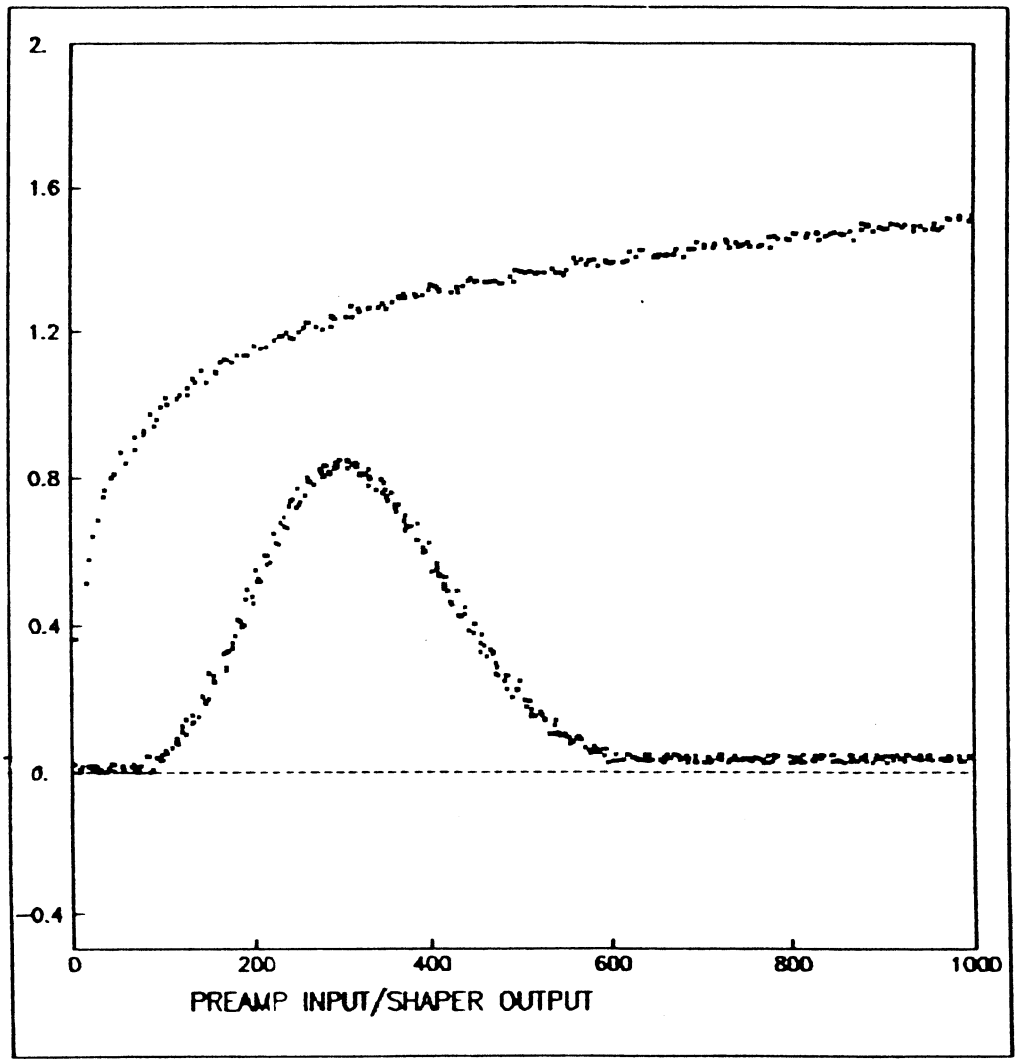
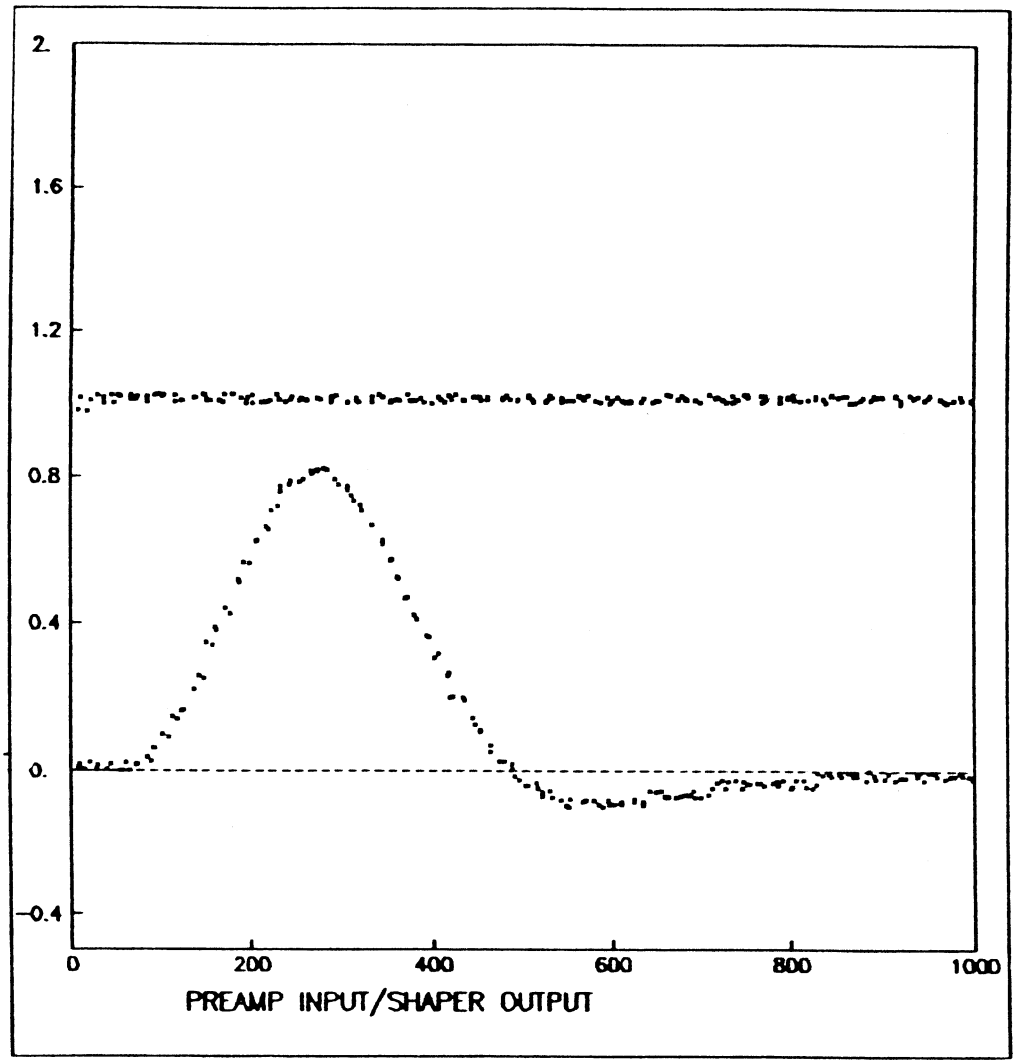

2.
1.6
1.2
0.8
0.4
0.
-0.4
0
200
400
600
800
1000
PREAMP INPUT/SHAPER OUTPUT

Figure 3a


2.
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-0.4
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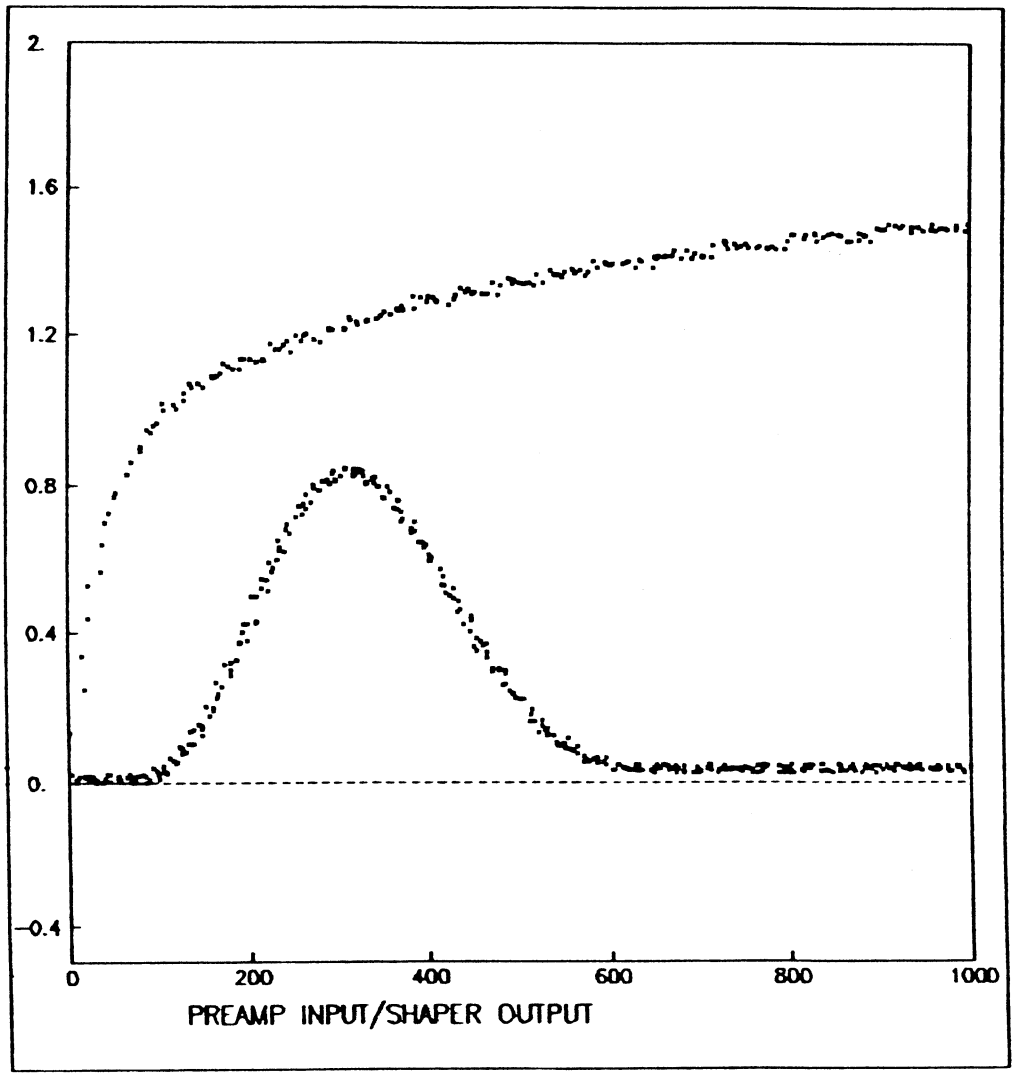
PREAMP INPUT/SHAPER OUTPUT

Figure 3b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0.8
0.4
0.
-0.4
0
200
400
600
800
1000
PREAMP INPUT/SHAPER OUTPUT

Figure 3c

References

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[5] R.C. Jared and M. Takashima, "Status of the TPC Calibration System", ALEPH-TPC Note #84-57 (1984).