ALEPH 86-89
S. Amendolia
18.7.86

Distr.: DATACQ-TRIGGER

ALEPH TRIGGER SUPERVISOR

F 682D

Functional Specifications

S.R.Amendolia, C.Avanzini, S.Galeotti,
M.Givoletti, F.Morsani, D.Passuello

INFN-Pisa
Dip. di Fisica - Universita' di Pisa

Version 1.0

June 29th, 1986

1. INTRODUCTION

ALEPH DATACQ Note 85-21[1] describes the Hardware Functional Specifications of the DAQ System. A good knowledge of this note (in particular chapters 2,3,4,7) is needed for the understanding of this document.

The ALEPH DAQ system can be subdivided in partitions; the system itself as a whole is one of the possible partitions, called the Main Partition.
For each partition, there are a set of ROCs (Read-Out Controllers) which, in response to a sequence of trigger signals, perform the read-out of the front-end electronics.

The specific source of the trigger signals is not relevant to the discussion (it could be the Main Trigger System, or any dedicated local trigger mechanism): what matters is the way in which the trigger signals are issued, which has to be standard. The source will be referred to as the Trigger System.

The Trigger Supervisor (TS) is the interface between the Trigger System and the ROCs. The TS operation is independent of the partition in which it operates; also, each partition needs one and only one TS. [2] It follows that there are many identical Trigger Supervisors in the system, one per partition.

The task of the TS is only to control the communication between the Trigger System and the ROCs: control means that it can act on the signals being transmitted, thus affecting the performance of the Data Acquisition System, i.e. it can inhibit the acquisition of the data, or can halt the system upon error detection.

The TS must be usable in all the phases of the DAQ operation, namely setting-up, system test, data acquisition: this implies that the device must be operated in continuous or single-step mode.

The TS does not include any "rate scaling" mechanism, nor it can perform actions based on statistical evaluations related to the quality of the data (monitor-like activity): it reacts to event-based triggers, and communicates with the ROCs, irrespective of the physical content of the data themselves.

2. COMMUNICATION PROTOCOL

2.1 Protocol between TS and ROCs

The synchronization of the exchange of messages (i.e. the Communication Protocol) between the TS and the Trigger System on one side, and the TS and the ROCs on the other side, is described by the Petri Net in Fig. 1 (refer to [1] for a discussion on the Petri Net approach).

Fig. 1 does not show any exception handling. The ROC states here described refer only to the ROC activity which is related to the trigger signals handling, and are not linked to the internal states of the CPU of these controllers.

In words, Fig. 1 can be read this way:

a. The TS receives Bunch Crossing (BX) signals from the Trigger System. The EGBX (Early Gated Bunch Crossing) and the GBX (Gated Bunch Crossing) signals are issued from the TS to the ROCs only if the system is ready to accept events. This implies that the READY state must be reached by the TS a fixed time before the BX is received, so that the EGBX can be issued early enough to trigger the initialization phases of the read-out of the sub-detectors.

b. There is no acknowledge of the EGBX by the ROCs.
In response to GBX, the ROCs issue a GBX ACK signal and a BUSY signal (the same signal on two different lines). The GBX ACK signal received by the TS is the AND of all the GBX ACK signals issued by the ROCs. This AND function is performed by the FIO boxes [3] . The receipt of the GBX ACK is a necessary condition for the TS to continue operation.

c. A Level 1 NO received by the TS and issued to the ROCs causes reset. A Level 1 YES allows data acquisition to continue until the complete result of the trigger is known. There is no direct acknowledge by the ROCs of the Level 1 YES signal.

d. There is no conceptual difference between a Level 2 NO and a Level 2 YES: they both imply some activity on the ROC side after which the ROC will release the BUSY signal.
A Level 2 NO causes the re-enabling of the front-end electronics for the acquisition of the next event: all this may require a non negligible amount of time.
A Level 2 YES implies that the data in the front-end electronics should be kept. No more events can be taken until at least one front-end buffer is free. In front-end modules without multiple input buffers, this will be the case until the ROC has read all the

data out.

e. The ROCs will in general begin the read-out of the front-end modules as soon as they receive the Level 2 YES via cable. But the specific action to be undertaken on the event is decided by each ROC when the Level 2 Broadcast message, issued by the TS, is received. See chapter 7 for details.

f. During all the time that the front-end modules' input buffers are not available for a new event, the ROCs hold the BUSY line on. The BUSY signal seen by the TS is the OR of all the BUSY lines of the ROCs (OR function performed by the FIO boxes [3]). The transition to a END_OF_BUSY state is the necessary condition for the TS to enable further triggers' acceptance.

2.2 Protocol between TS and Trigger System

There is no hand-shaking of messages between the TS and the Trigger System, i.e. the Level 1 and Level 2 pulses are issued by the Trigger System only when the GBX signal coming from the TS has been received. The trigger generation has to be inhibited inside the Trigger System itself. Lack of this will cause an error status reported by the TS.

2.3 Time diagrams

Fig. 2 (a,b,c) show the timing diagrams for the 3 possible "normal" trigger outcomes during data acquisition:

a. Level 1 NO
b. Level 1 YES followed by Level 2 NO
c. Level 1 YES followed by Level 2 YES.

As general remarks on Fig. 1,2, note that:

* Apart from the Bunch Crossing, Level 1 and Level 2 signals (input to the TS) and the EGBX (output), all the communications take place via levels: the levels are kept on as long as they do not cause ambiguities, and whenever possible are reset only at process completion.

* We never induce the negative signal from the absence of the positive one: absence or presence of both are a possible third state in the logic (read: error) which we want to detect, and this implies transferring even a YES/NO information on more than one bit.

3. *SPECIAL OPERATION MODES*

On top of the Normal Operation mode, the TS will implement a Single-Step Operation Mode and a Trigger Bypass Mode.

3.1 Single-Step Operation Mode

The inputs can come from the front-panel connector (external input) or can be simulated writing a specific pattern in an internal Fastbus register. Transitions are induced under the control of the operator, through a front-panel button or remotely, via Fastbus commands.
Event numbers start from zero, and are recorded and incremented in a different register than for Normal Operation Mode.

3.2 Trigger Bypass Operation Mode

In Trigger Bypass Mode, all the signals subject to non-Fastbus time-outs (like GBX ACK, Level 1 NO,...) are no longer necessary to cause a transition; if not present physically at time-out time, the "correct" transition takes place, and no time-out error is flagged; only the relative time-out counter is incremented (see register list). This can be done selectively on any subset of the input signals.
The event number is incremented starting from zero as for Single-Step Operating Mode, and using the same register.
This operating mode is different from simple time-out disabling, which can cause system hang-ups (for debugging purposes).
The aim is to allow a powerful tool to spot hang-ups in the Trigger System or on the ROC side.

4. FASTBUS COMMUNICATION

4.1 Addressing

The TS is a Fastbus master.
It responds to geographical addressing only.
It does not respond to broadcast operations.

4.2 Error handling

Parity is generated (odd) when sending data, and checked when data are received.
See below for the interpretation of the non-zero SS codes.

Errors can be fatal or non-fatal: some of them can be programmed to fall in one or the other cathegory.
The occurrence of any error (fatal or not) results in the setting of specific bits in CSR registers (see text and list further on).

The following information is stored in case of fatal FB transaction (master operation):

1. CSR 11: Fastbus error status
2. CSR 12: primary address of last FB error
3. CSR 13: secondary address of last FB error
4. CSR 14: data asserted during last FB error

All error conditions set CSR 0<00>.

4.3 SS Code interpretation

SS bits are stored in FB Error Status Register CSR 11<00:02>.

4.3.1 Master - Address cycle

* SS=0 normal - continue
* SS=1 Network busy: current operation aborted, wait and retry; increment counter in C000_0009, and set bit CSR 10<05>.
* SS=2 Network failure: fatal; set CSR 0<13> ,CSR 10<00> and halt.
* SS=3 Network abort: wait and retry; increment counter in C000_0009 and set bit CSR 10<05>.
* SS=4-7 fatal; set CSR 0<13>, CSR 10<00> and halt.

4.3.2 Master - data cycle

* SS=0 continue
* SS=1 Device busy: wait and retry; increment counter in C000_0007 and set CSR 10<04>
* SS=2 end-of-block; abnormal; halt (set CSR 0<13>,CSR 10<00>)
* SS=3 User defined; not expected; halt (set CSR 0<13>, CSR 10<00>)
* SS=4-5 Reserved; halt; (set CSR 0<13>, CSR 10<00>)
* SS=6-7 Data error; halt; (set CSR 0<13>, CSR 10<00>)

4.3.3 Slave

As a slave, transactions are ignored if errors are detected; codes are set to aid diagnostics.

1. PARITY ERROR:
   * no response on primary address if parity error detected
   * parity errors on secondary addresses and data cycles cause SS=6, and transactions are ignored; sets CSR 0<14>. Subsequent FB operations not affected.

2. INVALID INTERNAL ADDRESS:
   On both primary and secondary address, it causes SS=6; sets CSR 2<08>.

3. BLOCK TRANSFER: not implemented.

5. IINPUTS AND OUTPUTS

Communication between the TS and the modules in the DAQ system takes place via dedicated cables and Fastbus. Refer to [1] for a preliminary discussion of the physical implementation of the cable connection.

5.1 Inputs

5.1.1 Dedicated cables (external inputs)

1.	BX (Bunch Crossing)	Pulse; issued by LEP machine timing
2.	Level 1 NO	Pulse; issued by Trigger System
3.	Level 1 YES	Pulse; issued by Trigger System
4.	Level 2 NO	Pulse; issued by Trigger System
5.	Level 2 YES	Pulse; issued by Trigger System
6.	GBX ACK	Level; issued by FIO Box [3]: it is the AND of the GBX ACK signals from the ROCs
7.	BUSY	Level; issued by FIO Box: it is the OR of the BUSY signals from the ROCs
8.	TRIGGER TYPE	There are 32 lines carrying a 32-bit information; these are levels, representing the trigger type as determined by the Trigger System logic. These levels are latched into C000_0001 when the Level 2 YES input is received.

Each external input sets a Set/Reset FlipFlop, thus transforming the incoming pulses in levels. These levels enter CSR 16 (see CSR registers detail - section 7.2), where they are latched in phase with the TS internal clock.
When the output signal corresponding to a given input is issued by the TS (e.g. the GBX corresponding to a BX), the relative FlipFlop is reset, and the corresponding bit in CSR 16 cleared at the next clock edge: this allows a clean illegal input detection in each state.
The same is true when CSR 16 is written via Fastbus (only possible in Single Step Mode with External Input disabled): the FlipFlops are disabled, CSR 16 is reset via software.
The FlipFlop levels are internal to the TS: only the status latched by CSR 16 can be known from outside.

5.1.2 Control via Fastbus

The control of the TS takes place via Fastbus commands issued by the Partition Control Computer.

5.1.2.1 RUN/HALT

The TS is running when it is moving along the state diagram of Fig. 3, i.e. the occurrence of one of the conditions is sufficient to cause the corresponding transition. If in Single Step Mode, the transition is performed when a CONTINUE command is received (see below).

For any operation mode, the running state is indicated by the ACTIVE bit being on (CSR 0<15>); RUN/HALT is controlled by CSR 0<02>,<18>.

If HALT is requested, when in Normal or Trigger Bypass Mode, using CSR0<18>, the TS will complete the pending operations until it reaches the state "wait for BX", then it will HALT.
If in Single Step Mode, HALT is effective as soon as the current transition is performed.

Error conditions which cause the TS to HALT imply an immediate halt, irrespective of the state in which the error condition occurred.
When recovery from the error is completed, the RUN bit (CSR 0<02>) has to be set in order to resume operation; irrespective of the operation mode, action will be resumed from the state "wait for BX".
When RUN is requested, all error bits are cleared, but not the error counters (true for any operation mode).

5.1.2.2 PAUSE / CONTINUE

In Normal Operation or Trigger Bypass Mode, the PAUSE can be requested at any time writing in CSR 0<06>; however, the PAUSE state will be entered only when the pending event is completed, i.e. only from the state "Wait for BX". When paused, the ACTIVE bit will be set to zero.

In Single Step Mode, the PAUSE state is entered automatically when the RUN bit is set: a transition takes place only when the PAUSE bit is cleared (CONTINUE requested, setting bit CSR 0<22>); when the corresponding action is completed, the PAUSE state is re-entered automatically.

When inSingle Step Mode (only), the CONTINUE bit is ORed with the Front Panel

button, to allow manual operation of the module. However, the ACTIVE bit is kept ON irrespective of being or not in the PAUSE state.

5.1.2.3 ACTIVE Bit

As specified above, the ACTIVE bit ON indicates that the TS is running. The ACTIVE bit is OFF when the TS is halted.

The ACTIVE bit is OFF when the TS is in Normal Operation or Trigger Bypass Mode, and is paused: this bit can be read to know when the PAUSE state is actually entered, which can take place several milliseconds after the PAUSE has been requested writing in CSR 0<06>.

In Single Step Mode, the ACTIVE bit is ON also when the TS is paused; thus the Operation Mode bits (CSR 0 <07-09>) must be read together with teh ACTIVE bit.

5.1.2.4 External Input

External Input enabling is controlled via CSR 0<10>. External inputs come from the front-panel connector (see section 5.1.1).

In Normal Operation or Trigger Bypass Mode, the External Input is automatically enabled: the front-panel connector has to be the only source of input signals.

In Single Step Mode, the External Input can be disabled. The input configuration is then written via Fastbus in CSR 16, where the external inputs are normally latched. At the subsequent CONTINUE command, the input configuration as stored in CSR 16 is used to determine the transition.

5.1.3 Illegal input control

Illegal inputs are signals coming from external world (Trigger System, Rocs) at wrong times (out of sequence): a relative counter is incremented. A fatal error is flagged if the relative bit in CSR 2<00> is on.

Illegal Inputs are checked by a dedicated piece of hardware, irrespective of the input source (external or Fastbus): the check is performed on CSR 16, which latches the input line status.

After Level 2 YES or NO receival (refer to the state diagram in Fig. 3), CSR 16 configuration is cheched to verify that no spurious signals have reached the TS before than the pending event is completed.
BX signals, arriving every 22.5 μsec, are ignored, and CSR 16 <00> cleared.
This check is performed if the Illegal Input detection is enabled.

Irrespective of the Illegal Input detection setting, and for all the operation modes, the status of the GBX ACK input is always checked to be ON, excepted the states "Wait for END_OF_BUSY", "Wait for BX", "Wait for GBX ACK". GBX ACK going down between the state "Wait for Level 1" and the state "Broadcast Level 2 Message" is the only indication of an associated Raed-Out Controller which is malfunctioning.
Occurrence of this error condition will cause the HOLD line to be set and the TS to halt.

Bits for ILLEGAL INPUT Status are CSR 10<20-24>; bits for ILLEGAL INPUT LIMIT Overflow are CSR 10<25-29>; registers for ILLEGAL INPUT count and count limit are C000_0017 to C000_0020.

5.1.4 Time-out Control

Changing the Enable Status of the timers (Fastbus or non-Fastbus), or the value of the time-out for the software timers, can only take place when the TS is in the PAUSE state (CSR 0<06> set), or even HALTed (CSR 0<02> set to zero) for the Normal Operation Mode.

5.1.4.1 Fastbus time-outs

Fastbus transactions are monitored by four timers:

1. LONG TIMER: times the total length of a FB transaction.
2. WAIT TIMER: times the duration of assertion of WT.
3. ADDRESS TIMER: time between asserting AS and receiving AK.
4. DATA TIMER: time between asserting DS and receiving DK.

These timers are controlled through CSR 9.
Occurrence of any of these time-outs sets CSR 0<00>; the four timers set also CSR 10<16>,<17>,<18>,<19> respectively.

The values for these timers are hardware set , and will be determined according to the specific layout of the Fastbus set-up.

5.1.4.2 Non-Fastbus time-outs

During normal operation, the following events need to be checked versus time-out by the following timers:

1. BX Timer
   - Time-out value : 30 µsec
   - Tolerance : 5 µsec
   - Type : hardware
   - Control : CSR 15<00>,<16>
   - The check is performed only when in state "Wait for BX"

2. GBX ACK Timer
   - Time-out value : 1.0 µsec
   - Tolerance : .5 µsec
   - Type : hardware
   - Control : CSR 15<01>,<17>
   - Activated when GBX is issued

3. Level 1 (YES or NO) Timer
   - Time-out value : 4 µsec typical (stored in CSR C000_000D)
   - Tolerance : .5 µsec
   - Type : hardware
   - Control : CSR 15<02>,<18>
   - Activated when GBX is issued

4. Level 2 (YES or NO) Timer

   Time-out value : 60 μsec typical (stored in CSR C000_000F)
   Tolerance : 5 μsec
   Type : software
   Control : CSR 15<03>,<19>
   Activated when Level 1 is received (in state "Wait Level 2")

5. Arbitration Timer

   This is the time the TS is allowed to wait to win the mastership on the relevant segments (i.e. the time between the receival of the Level 2 YES -which triggers the arbitration request- and the moment when AG(d)):
   Time-out value : 50 msec (stored in C000_0011)
   Tolerance : 5 msec
   Type : software
   Control : CSR 15<04>,<20>
   Activated when AR is issued.

6. Broadcast Timer

   This is the time the TS is allowed to wait until the broadcast message has reached its destinations (i.e. the time between the start of the broadcast operation -establish broadcast address- and the moment when AK # 0): this timer is replaced by the Fastbus WAIT TIMER.

7. END_OF_BUSY Timer

   Time-out value : 5 msec typical (stored in CSR C000_0015)
   Tolerance : .5 msec
   Type : software
   Control : CSR 15<05>,<21>
   Activated at the end of the broadcast operation

5.1.5 Changing Operation Modes

The TS has to be halted in order to change the Operation Mode (setting or resetting bits CSR 0<7-9>).
Any attempt to change operation mode when not halted will result in an SS = 6 response, and the request is ignored.

An operation mode has to be explicitily requested setting one of the relative bits (7-9) in CSR 0: when one is set, the other two are automatically cleared (only if the TS is halted, i.e. CSR 0<02> OFF).
Clearing an operation mode bit already OFF will have no effect.
Clearing the one operation bit which is ON will put the TS in an "idle" state (bits CSR 0<07-09> all zero): any attempt to RUN the TS (setting CSR 0<02>) will result in an SS = 6 response, and no action is taken.

When restarted (i.e. RUN requested, setting bit CSR 0<02>), operation will immediately resume from state "Wait for BX" if in Normal Operation or Trigger Bypass Mode (PAUSE bit CSR 0<06> set to 0).
If in Single Step Mode, a RESTART (RUN) will put the TS in the PAUSE state: steps are induced one by one by pushing the front-panel button or setting the CONTINUE bit (CSR 0<22>); after each action, PAUSE state is reentered.

CLEAR ERR, during any operation mode, affects the error bits, but not the error counters, which have to be explicitily zeroed. They are cleared at POWER ON, at RESET, or when changing operation mode.

WARNING: Error counters are cleared when changing operation modes (by writing in CSR 0<07-09>): they must be read before the change is done if they need to be recorded. This is particularly relevant in Normal Operation Mode, where error counts are part of the global run statistics.

At POWER ON and RESET, the dafault operation mode is NORMAL.
Refer to CSR Bit settings (section 7.3) for the configuration set at PWR ON and RESET.

5.1.5.1 Normal Operation Mode

It is controlled by CSR 0<09>,<25>.

Any change of the parameters which govern the TS functioning is considered a major modification to the running conditions, deserving a special attention by the RUN Control software in the Partition Control Computer: thus the TS needs to be halted also for:

1. changing the Timers Control (CSR 9, 15)
2. enabling the Illegal Input detection (CSR 0<10>)
3. changing the severity level of the Illegal Input (CSR 2<0>)
4. changing the Time-out values (CSR User Space)
5. changing the error counter limits
6. clearing the error counters

5.1.5.2 Trigger Bypass Mode

It is controlled by CSR 0<08>,<24>.

Contrary to the Normal Operation Mode, any of the running parameters can be changed, and error counters can be cleared, also when in the PAUSE state.

The Fastbus Timers (CSR 9) setting is the same as for the Normal Operation Mode. Non-Fastbus Timers control bits (CSR 15) take over the following meaning:

bit OFF Timer disabled, no time-out condition can happen for the corresponding signal (same as for the other operation modes)

bit ON Fake signal generation enabled: the timer is active, but the time-out recovery routine, instead of flagging a fatal time-out error, and halting the TS, increments the corresponding "Fake Signal" counter (CSR User Space - see section 7.1) and causes the transition to the next state. When two signals are controlled by the same timer (e.g Level 2 YES and NO, exclusively) the "positive" transition (Level 2 YES in the example) is always induced.

5.1.5.3 Single Step Mode

It is controlled by CSR 0<07>,<23>.

Parameters' change and clearing of counters can take place also when paused (PAUSE is the most frequent state in Single Step Mode).

Illegal Input detection can be enabled, independent of the source of the inputs (external or Fastbus)

Non-Fastbus Timers control is meaningless in most cases.

5.2 Outputs

5.2.1 Dedicated cables

1. EGBX (Early Gated Bunch Crossing) .
   Destination: all front-end ROCs participating in the partition (via FIO boxes).
   Type: Level; reset at GBX generation

2. GBX (Gated Bunch Crossing) .
   Destination: all front-end ROCs participating in the partition (via FIO boxes).
   Type: Level; reset upon reception of GBX ACK. .

3. Level 1 NO .
   Destination: ROCs as above
   Type: Level; reset upon reception of END_OF_BUSY (i.e. transition 1 --> 0 of BUSY signal). .

4. Level 1 YES
   Destination: ROCs as above
   Type: Level; reset by END_OF_BUSY as for Level 1 NO

5. Level 2 NO
   Destination: ROCs as above
   Type: Level; reset by END_OF_BUSY

6. Level 2 YES
   Destination: ROCs as above
   Type: Level; reset by END_OF_BUSY

6. HOLD
   Destination: FIO Box
   Type: Level

5.2.1.1 EGBX generation

This signal is generated when in the state "Wait BX".
Each BX received by the TS during its operation (i.e. when the ACTIVE bit is ON) starts a hardware timer (EGBX Timer) which interrupts the TS.

If the EGBX Timer interrupts the TS when in the "Wait BX" state, the EGBX level is issued, and the next BX received will cause GBX generation.
If the EGBX Timer interrupts the TS when still in the "Wait END_OF_BUSY" state, no EGBX is issued, and also the next BX will be ignored.
Any interrupt from the EGBX Timer received in any state other than "Wait BX" will be ignored.

In other words, GBX generation is gated by the fact that EGBX has been generated as well.
The EGBX output level is reset by the GBX level generation.

EGBX is issued by the TS to provider an "early warning" to the Read-Out Controllers which may have to initiate read-out procedures before than the actual beam-crossing takes place. The setting of the EGBX Timer has to be done in accordance with the sub-detectors requirements.

5.2.1.2 Level 2 YES generation

For any LEVEL 2 YES a Broadcast Message will be issued to the ROCs, carrying the relevant information needed by the ROC's to carry-on with digitization and formatting; since the broadcast can be delayed by a large amount of time [1], the Level 2 YES is sent also via cable to initiate read-out in the ROCs at the earliest time possible.

5.2.1.3 HOLD line

A level is present on this general line each time a fatal error is detected (and the TS halts). However, critical sub-detector read-out parts should not rely on this line to take actions, but should react locally to abnormal statuses.

The HOLD line is distributed to all the intelligent devices taking part in the partition, as an "information line" and shall be reset by a TS RESTART (RUN). It is expected that these devices [1] interrupt their current action and "latch" their input and output lines for investigation by the Partition Control Computer.

When the HOLD line is set, the status of CSR 16 is frozen, i.e. signals arriving at the TS front-panel are no longer latched: CSR 16 reflects the input status at the time of the error.

5.2.2 Fastbus

5.2.2.1 Level 2 Broadcast

The primary and secondary addresses for the Broadcast message are in registers C000_0003 and C000_0004. The broadcast message is then delivered in data cycles.

C000_0003 is downloaded directly by the Partition Control Computer: it contains the broadcast address to be used by the Ts master port for broadcasting the Level 2 YES message to the Read-Out Controller pertaining to that partition, univoquely identified by a broadcast class number. See section 7.2.13 for C000_0003 and C000_0004 structure.

Message format (in Normal Operation Mode):

word 1	bits 0-31	event number (copied from C000_0000)
word 2	bits 0-31	trigger type (copied from C000_0001)

In Single-Step and Trigger Bypass Operation modes, the Message format is:

word 1	bits 0-31	event number (copied from C000_000B)
word 2	bits 0-31	all ones

5.2.2.2 Request service

This message is issued when a fatal error condition is detected; a Fastbus Interrupt will be issued to the Partition Control Computer. Addresses are in CSR E,F; the operation is controlled via CSR 2<04>.

5.2.3 Dead Time measurement outputs

The TS provides four output signals which may be used for dead-time measurements: the reason for this is that the TS is the only central point in the data acquisition system where the status of the read-out processes, of the trigger outcomes, and of the possible errors or abnormal running conditions is known.

These signals are only given when in Normal Operation Mode; they are ECL differential , and can be used as a gate for an external scaler.

Active time : present when the Active bit is ON (and the PAUSE is OFF). Measures the time during which the TS is accepting inputs from the Trigger System.

Level 1 busy time: present from GBX generation until Level 1 NO is issued. Measures the time during which the TS is busy waiting for a Level 1 trigger reject; in practice, this should not contribute to the dead-time, since Level 1 response is due to arrive well before the next bunch crossing.

Level 2 busy time: present from GBX generation until Level 2 NO is issued. Measures the time during which the TS is busy waiting for a Level 2 reject.

Busy time: Present from GBX generation until an EGBX is successfully generated.
Measures the time during which the TS is busy dealing with triggers (rejected or not).

Note: it is implied that an external scaler be counting the BX signals during the times the above gates are ON; in this way, a direct measurement of the dead-time is given by the ratio of Busy Time counts on Active Time counts. Ratios of Level 1 or 2 busy times on Active Time can be used to analize the contribution of rejecting triggers to the overall dead-time.

Since in Normal Operation Mode any Fastbus command can be given only when the TS is Halted or Paused, contributions to the dead-time from the interaction of the operator with the TS are automatically excluded by these measurements.
Also, error conditions raising the HOLD line cause a TS HALT, which is not reflected in the above quantities.

6. *FINITE STATE MACHINE DESCRIPTION*

The functioning of the TS can be described in terms of a Finite State Machine. Fig. 3 shows the corresponding state diagram for Normal Operation Mode.

In the figure, the circles represent states of the machine: they shall be uniquely numbered, and this number will be stored in CSR 17. Numbering is not sequential, but reflects a coding which depends on the intternal hardware structure of the TS.
Transitions from a state to another can be induced only by a change of the input conditions (here input means a combination of physical inputs to the TS, time-out interrupts, other general internal exceptions).
Arrows in Fig. 3 are labelled with the condition which determines them, and they correspond to the action to be performed to move from one state to another: given an initial state and a condition, it is univoquely determined the final state and the action needed to reach it. An action is made of one or more elementary operations (enabling time-outs, resetting bits, etc.).

7. FASTBUS REGISTERS

Only CSR space is used in the TS; a list of the registers used and of their contents follow.
Refer to Fastbus specifications (Chapter 8) for further details on the use of selective set/clear registers.

7.1 Register list

REG	TYPE	CONTENT
0	S/C	ID,STATUS,CONTROL
2	S/C	STATUS AND CONTROL
7	R/W	BROADCAST CLASS
8	R/W	ARBITRATION LEVEL
9	S/C	FB TIMERS CONTROL
E	R/W	SOURCE A INTERRUPT PRIMARY ADDRESS
F	R/W	SOURCE A INTERRUPT SECONDARY ADDRESS
10	R/W	ERROR STATUS
11	R/W	FB ERROR STATUS
12	R/W	LAST PRIMARY ADDRESS AT ERROR
13	R/W	LAST SECONDARY ADDRESS AT ERROR
14	R/W	LAST DATA ASSERTED AT ERROR
15	S/C	TIME-OUT CONTROL
16	R/W	INPUT/OUTPUT LINES CURRENT STATUS
17	R/W	INTERNAL STATE
C000_0000	R/W	EVENT NUMBER
C000_0001	R/W	TRIGGER TYPE
C000_0003	R/W	BROADCAST PRIMARY ADDRESS
C000_0004	R/W	BROADCAST SECONDARY ADDRESS
C000_0007	R/W	DEVICE RETRY TOTAL COUNTER
C000_0008	R/W	DEVICE RETRY COUNTER LIMIT
C000_0009	R/W	NETWORK RETRY TOTAL COUNTER
C000_000A	R/W	NETWORK RETRY COUNTER LIMIT
C000_000B	R/W	EVENT NUMBER IN S-S AND BYPASS MODES
C000_000C	R/W	FAKE GBX ACK TIME-OUT TOTAL COUNTER
C000_000D	R/W	LEVEL 1 TIME-OUT VALUE
C000_000E	R/W	FAKE LEVEL 1 TIME-OUT TOTAL COUNTER
C000_000F	R/W	LEVEL 2 TIME-OUT VALUE
C000_0010	R/W	FAKE LEVEL 2 TIME-OUT TOTAL COUNTER
C000_0011	R/W	ARBITRATION TIME-OUT VALUE
C000_0012	R/W	ARBITRATION TIME-OUT TOTAL COUNTER
C000_0013	R/W	BROADCAST TIME-OUT VALUE

C000_0015	R/W	END_OF_BUSY TIME-OUT VALUE
C000_0016	R/W	FAKE END_OF_BUSY TIME-OUT TOTAL COUNTER
C000_0017	R/W	ILLEGAL BX INPUT TOTAL COUNTER
C000_0018	R/W	ILLEGAL BX INPUT COUNTER LIMIT
C000_0019	R/W	ILLEGAL LEVEL 1 NO INPUT TOTAL COUNTER
C000_001A	R/W	ILLEGAL LEVEL 1 NO INPUT COUNTER LIMIT
C000_001B	R/W	ILLEGAL LEVEL 1 YES INPUT TOTAL COUNTER
C000_001C	R/W	ILLEGAL LEVEL 1 YES INPUT COUNTER LIMIT
C000_001D	R/W	ILLEGAL LEVEL 2 NO INPUT TOTAL COUNTER
C000_001E	R/W	ILLEGAL LEVEL 2 NO INPUT COUNTER LIMIT
C000_001F	R/W	ILLEGAL LEVEL 2 YES INPUT TOTAL COUNTER
C000_0020	R/W	ILLEGAL LEVEL 2 YES INPUT COUNTER LIMIT

Note:

1. TOTAL COUNTERS are incremented each time the appropriate error condition happens: the increment is made via software.

2. COUNTER LIMITS are set at initialization, before the TS is RUN, or modified when in PAUSE state (for Single Step or Trigger Bypass Modes only - ref. section 5.1.5). Ecah time an error condition takes place, an internal register is incremented (independent of the TOTAL COUNTER above): this register's content is compared with the corresponding COUNTER LIMIT register to determine if the limit has been exceeded, in which case an overflow error will be flagged (see CSR 10 - section 7.2.6).

7.2 Register content

7.2.1 CSR 0 : ID,STATUS AND CONTROL

BIT	READ	WRITE
0	Error flag	Unused
1	Not implemented	
2	Running	Run
3-5	Not implemented	
6	PAUSED	Request PAUSE
7	Single Step Mode enabled	Enable Single Step Mode
8	Trigger Bypass Mode enabled	Enable Trigger Bypass Mode
9	Normal Oper. Mode enabled	Enable Normal Oper. Mode
10	Illegal Input detection enabled	Enable Illegal Input detection
11	External Input enabled	Enable External Input
12	Unused	Unused
13	Fatal error	Unused
14	Parity error	Unused
15	Active (0 = halted)	Unused
16	Device	Clear error flag
17	|	Unused
18	|	HALT
19	Type	Unused
20	Manufact ID (LSB)	Unused
21	|	Unused
22	|	CONTINUE
23	|	Clear Single Step Mode
24	|	Clear Trigger Bypass Mode
25	|	Clear Normal Oper. Mode
26	|	Disable Ilegal Input detection
27	|	Disable External Input
28-30	|	Unused
31	Manufact ID (MSB)	Unused

7.2.2 CSR 2 : STATUS AND CONTROL

BIT	READ	WRITE
0	Illegal Input severity = fatal	Set Illeg. Input severity fatal
1-3	Unused	
4	Source A Interrupt enabled	Enable Source C Interrupt
5-7	Unused	
8	Non-existent address	Set non-existent address
9-31	Unused	

7.2.3 CSR 8 : ARBITRATION LEVEL

bit	0-5	Arbitration Level
bit	6	Unused
bit	7	Not implemented
bit	8-31	Unused

7.2.4 CSR 9 : FASTBUS TIMERS CONTROL

BIT	READ	WRITE
0-3	Unused	
4	Long Timer enabled	Enable Long Timer
5	Wait Timer enabled	Enable Wait Timer
6	Address Timer enabled	Enable Address Timer
7	Data Timer enabled	Enable Data Timer
8-19	Unused	
20		Disable Long Timer
21		Disable Wait Timer
22		Disable Address Timer
23		Disable Data Timer
24-31	Unused	

7.2.5 CSR E,F : Interrupt Control

CSR E bit 0-31 Interrupt Primary Address

CSR F bit 0-31 Interrupt Secondary Address

The only use of Fastbus Interrupts is to signal fatal errors to the Host Computer, to which the addresses in CSR E,F refer.

7.2.6 CSR 10 : ERROR STATUS

BIT	CONTENT
0	Fastbus error
1	Time-out
2	Illegal Input
3	Unused
4	Device retry
5	Network retry
6	Device retry overflow
7	Network retry overflow
8	Unused
9	GBX ACK Time-out
10	Level 1 Time-out
11	Level 2 Time-out
12	Arbitration Time-out
13	Broadcast Time-out
14	END_OF_BUSY Time-out
15	Unused
16	Long timer Time-out
17	Wait timer Time-out
18	Address timer Time-out
19	Data timer Time-out
20	Illegal BX input
21	Illegal Level 1 NO input
22	Illegal Level 1 YES input
23	Illegal Level 2 NO input
24	Illegal Level2 YES input
25	Illegal BX input overflow
26	Illegal Level 1 NO input overflow
27	Illegal Level 1 YES input overflow
28	Illegal Level 2 NO input overflow
29	Illegal Level 2 YES input overflow
30	Unused
31	Unused

7.2.7 CSR 11 : FASTBUS ERROR STATUS (MASTER)

BIT	CONTENT
0	SS0
1	SS1
2	SS2
3	MS0
4	MS1
5	MS2
6	P bit (= 1 means error in primary cycle)
7	S bit (= 1 means error in secondary cycle)
8	D bit (= 1 means error in data cycle)
9-31	Unused

7.2.8 Fastbus Status at error

CSR 12	bit 0-31	Primary address
CSR 13	bit 0-31	Secondary address
CSR 14	bit 0-31	Data

At each operation performed by the Master Fastbus Port, addresses and data are stored in CSR 12-14: when an error condition occurs,they contain the most recent configuration at the time of the error; P,S,D bits in CSR 11 tell in which cycle of the Fastbus operation the error occurred.

7.2.9 CSR 15: Time-out Control

BIT	READ	WRITE
0	BX Timer enabled	Enable BX Timer
1	GBX ACK Timer enable	Enable GBX ACK Timer
2	Level 1 Timer enabled	Enable Level 1 Timer
3	Level 2 Timer enabled	Enable Level 2 Timer
4	Arbitration Timer enabled	Enable Arbitration Timer
5	END_OF_BUSY Timer enabled	Enabled END_OF_BUSY Timer
6-15	Unused	
16		Disable BX Timer
17		Disable GBX ACK Timer
18		Disable Level 1 Timer
19		Disable Level 2 Timer
20		Disable Arbitration Timer
21		Disable END_OF_BUSY Timer
22-31	Unused	

The action taken by the TS at time-out depends on the Operation Mode setting.

7.2.10 CSR 16 : Input/Output Lines Status

BIT	CONTENT	TYPE
0-5	Unused	
6	HOLD	OUT
7	BUSY	IN
8	EGBX	OUT
9	BX	IN
10	Level 1 NO	IN
11	Level 1 YES	IN
12	Level 2 NO	IN
13	Level 2 YES	IN
14	GBX ACK	IN
15-31	Unused	

Input signals are latched in phase with the TS internal clock.

7.2.11 CSR 17 : Internal State

BIT	CONTENT
0-5	Internal State number
6-31	unused

Internal states numbering is not sequential. On the contrary, it reflects addresses of internal memories where the microcoded operation sequences are stored.

7.2.12 Broadcast Message Registers

CSR C000_0000 bit 0-31 Event number

Used in Normal Operation Mode only. This is the only place where the event number for a specific run is generated. It is incremented (by software) in the state "Broadcast Level 2 Message". It is automatically cleared at POWER ON, RESET, RUN. Cannot be cleared when in PAUSE state.

CSR C000_000B bit 0-31 Event number

Used only in Trigger Bypass and Single Step Operation Modes. Automatically cleared at POWER on, RESET, RUN. Can be cleared even in PAUSE state.

CSR C000_0001 bit 0-31 Trigger type

Levels coming from the Trigger System are latched by the Level 2 YES input.
This register is cleared when an END_OF_BUSY signal is received.

CSR C000_0000 (or CSR C000_000B depending on the Operation mode) and CSR C000_0001 are copied into the first and the second word of the Level 2 Broadcast Message.

7.2.13 Broadcast Address Registers

CSR C000_0003 Primary Address

BIT	MEANING	VALUE
0	L Bit	1
1	G Bit	1
2		1
3		0
4-7	Function Bits	N
8-30		0
31	GP Bit	0

N is the Broadcast Class number identifying the Partition controlled by the TS.

CSR C000_0004 Secondary Address

BIT	VALUE
0-27	0
28	1
29-31	0

So the content is C000_000, mandatorily, as required by [1], Appendix A.
This register is mantained as such (read : downloadable i.e. modifiable) for redundant flexibility.

7.2.14 Retry counters

CSR	C000_0007	bit 0-31	Device Retry Total Counter (software incremented when CSR 10<04> is set)
CSR	C000_0008	bit 0-31	Device Retry Counter Limit
CSR	C000_0009	bit 0-31	Network Retry Total Counter (software incremented when CSR 10<05> is set)
CSR	C000_000A	bit 0-31	Network Retry Counter Limit

These are RAM registers (32 bit deep).
Power on setting is zero. Cleared when any of CSR 0<07-09> is set to 1.
Cleared by RUN (CSR 0<02> set to 1). Cleared by RESET.

7.2.15 Trigger Bypass fake signal counters

CSR	C000_000C	bit 0-31	GBX fake signal counter
CSR	C000_000E	bit 0-31	Level 1 (YES) fake signal counter
CSR	C000_0010	bit 0-31	Level 2 (YES) fake signal counter
CSR	C000_0016	bit 0-31	END_OF_BUSY fake signal counter

These are RAM registers (32 bit deep), software incremented when the corresponding time-out takes place, and the fake signal is generated.
Set at zero at Power on. Cleared by RUN (CSR 0<02> set to 1) and by RESET.

7.2.16 Time-out value registers

CSR	C000_000D	bit 0-31	Level 1 time-out value
CSR	C000_000F	bit 0-31	Level 2 time-out value
CSR	C000_0011	bit 0-31	Arbitration time-out value
CSR	C000_0015	bit 0-31	END_OF_BUSY time-out value

These are RAM registers (32 bit deep).
Setting at Power on is undefined. Unaffected by RESET, RUN, Operation Mode change.

7.2.17 Illegal Input counters

CSR C000_0017 to CSR C000_0020 (see list section 7.1)

All 32 bit deep RAM registers. Total counters are incremented via software when Illegal Input is detected.
Set to zero at Power on. Cleared by RESET, RUN, Operation Mode change (any of CSR 0<07-09> set to 1).

7.3 CSR Bits settings

CSR	BIT	CONTENT	PWR ON	RB	RST	CE	RUN	SING. STEP	BY PASS	NORM MODE
0	0	Error flag	0	-	0	0	0	-	-	-
0	2	RUN	0	0	0	-	1	0	0	0
0	6	PAUSE	1	1	1	-	d	1	0	0
0	7	Single Step Mode	0	-	0	-	-	1	0	0
0	8	Bypass Mode	0	-	0	-	-	0	1	0
0	9	Normal Op. Mode	1	-	1	-	-	0	0	1
0	10	Illeg. Input Enabled	1	-	1	-	-	1	1	1
0	11	Extern. Input Enabled	1	-	1	-	-	0	1	1
0	15	Active	0	-	0	-	1	0	0	0
2	0	Illeg. Input Fatal	1	-	1	-	-	-	-	1
2	4	Source A Intpt. En.	1	-	1	-	-	1	1	1
2	8	Non-exist. address	0	-	0	0	0	0	0	0
9	4-7	FB Timers	1	-	1	-	-	1	1	1
10	All	Error Status	0	-	0	0	0	-	-	-
11	0-10	FB error status	0	-	0	0	0	-	-	-
12	All	Last primary	0	-	0	0	0	-	-	-
13	All	Last secondary	0	-	0	0	0	-	-	-
14	All	Last data	0	-	0	0	0	-	-	-
15	0-4	Time-out control	1	-	1	-	-	0	1	1
16	6-13	I/O lines status	0	-	0	-	0	-	-	-
17	All	Internal state	I	I	I	-	I	-	-	-

(- means "unaffected"
I means "Initial State", i.e. "Wait BX"
d means "dependent on Operation Mode")

Broadcast primary and secondary addresses, Arbitration levels, Time-out values, error counter limits need to be down-loaded at POWER ON.
All error counters are cleared by POWER ON and RESET.

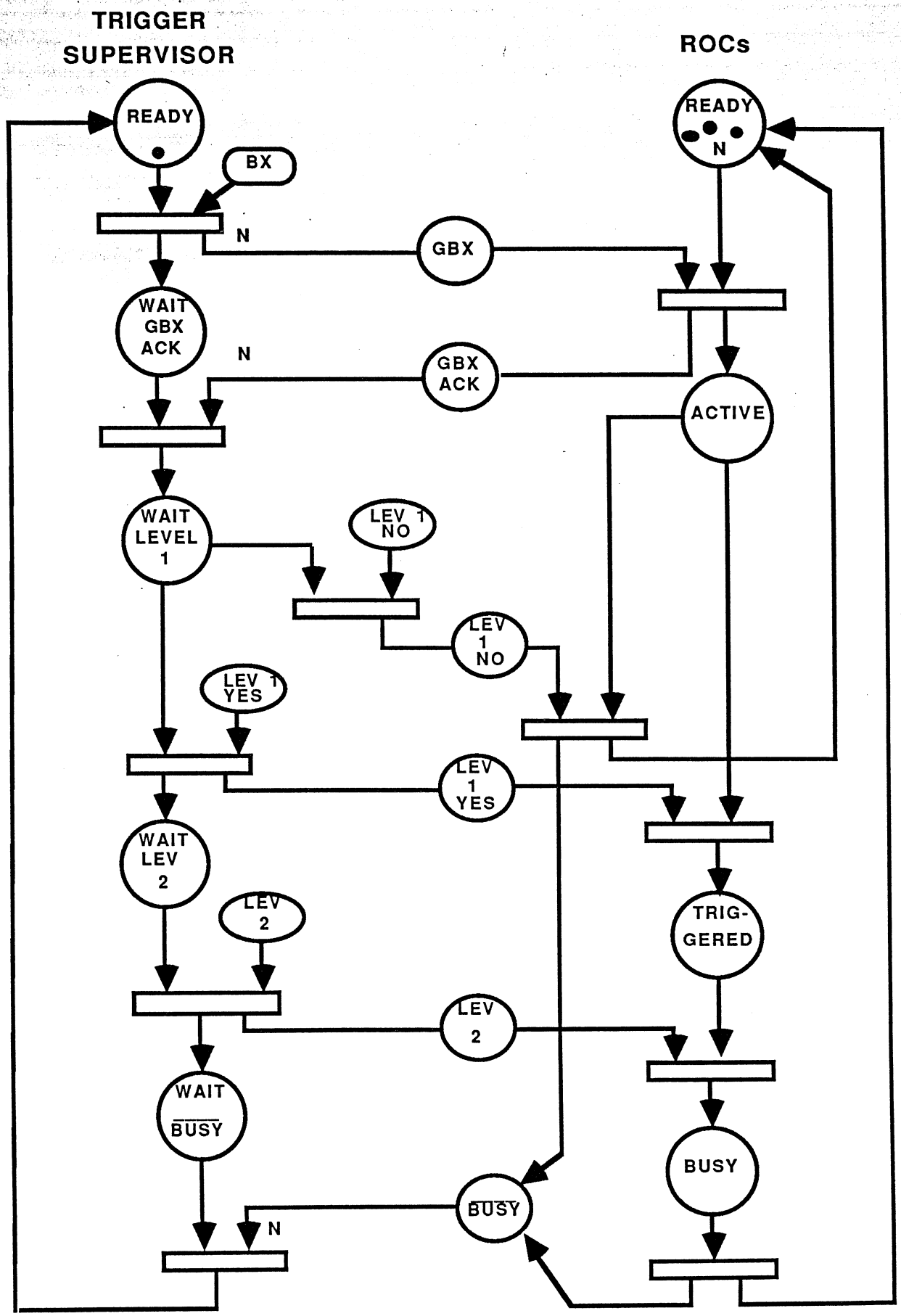

Fig. 1: TS/ROC protocol (Petri Net)

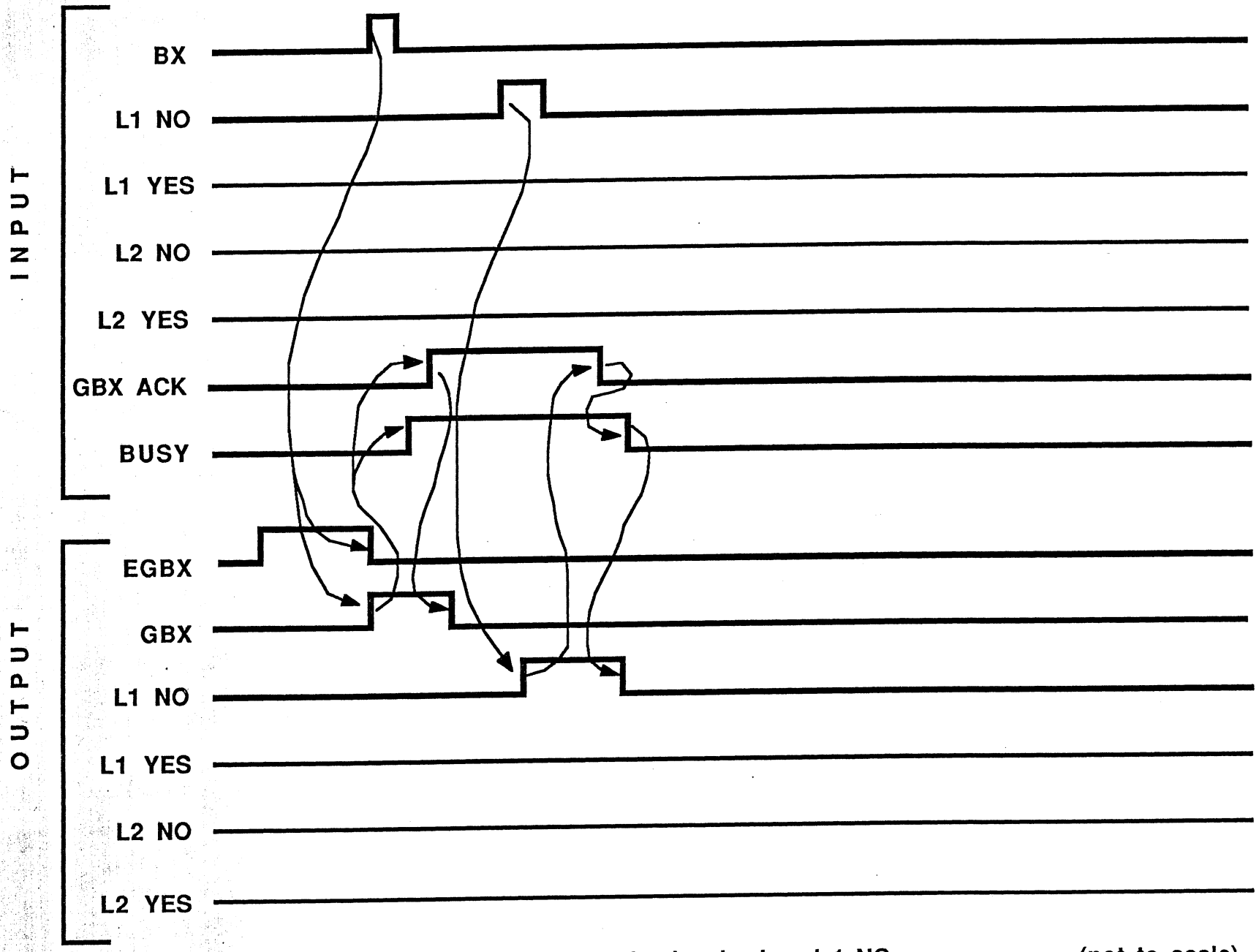

FIG. 2a : rejection by Level 1 NO (not to scale)

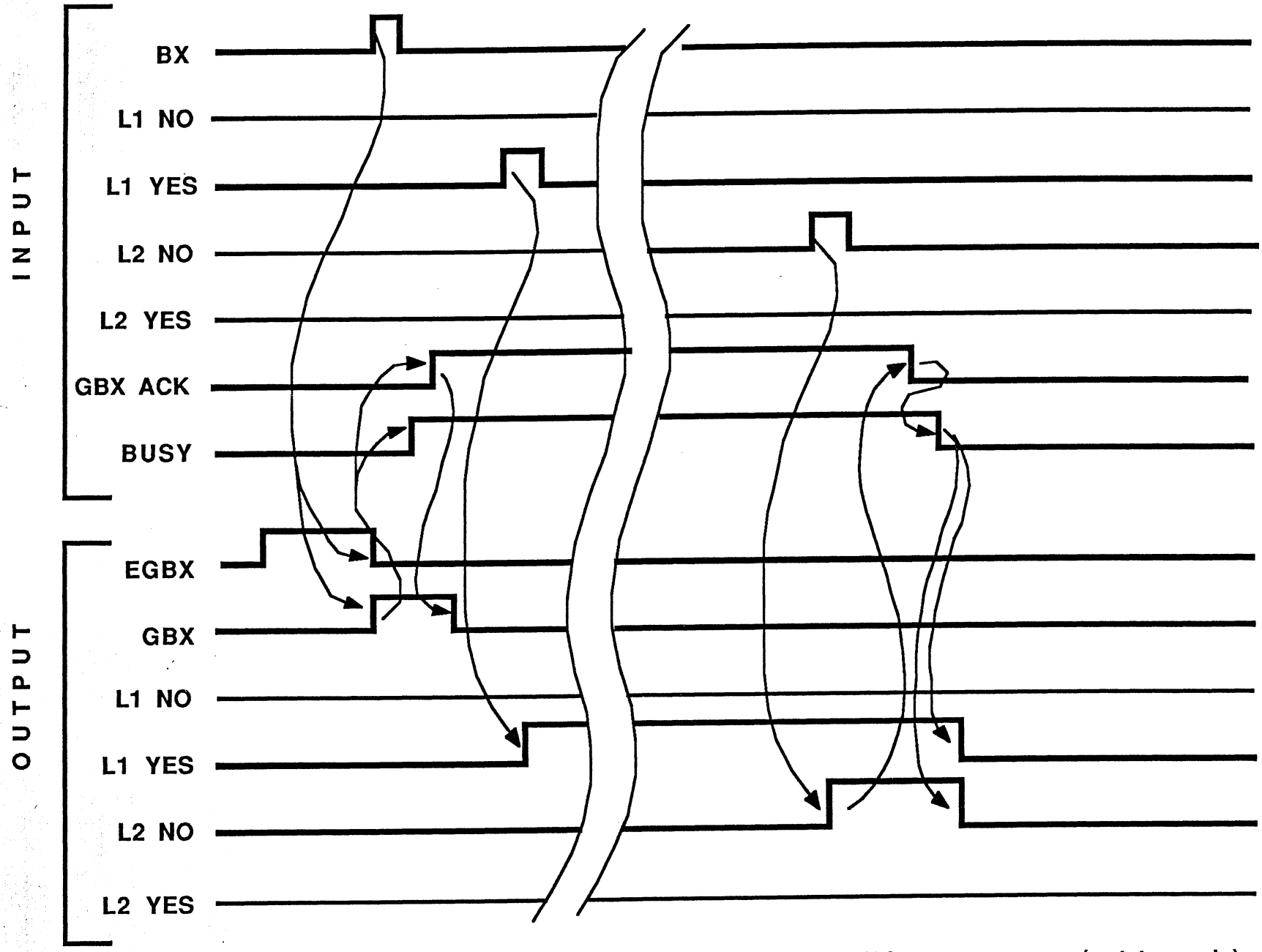

FIG. 2 b : rejection by Level 2 NO (not to scale)

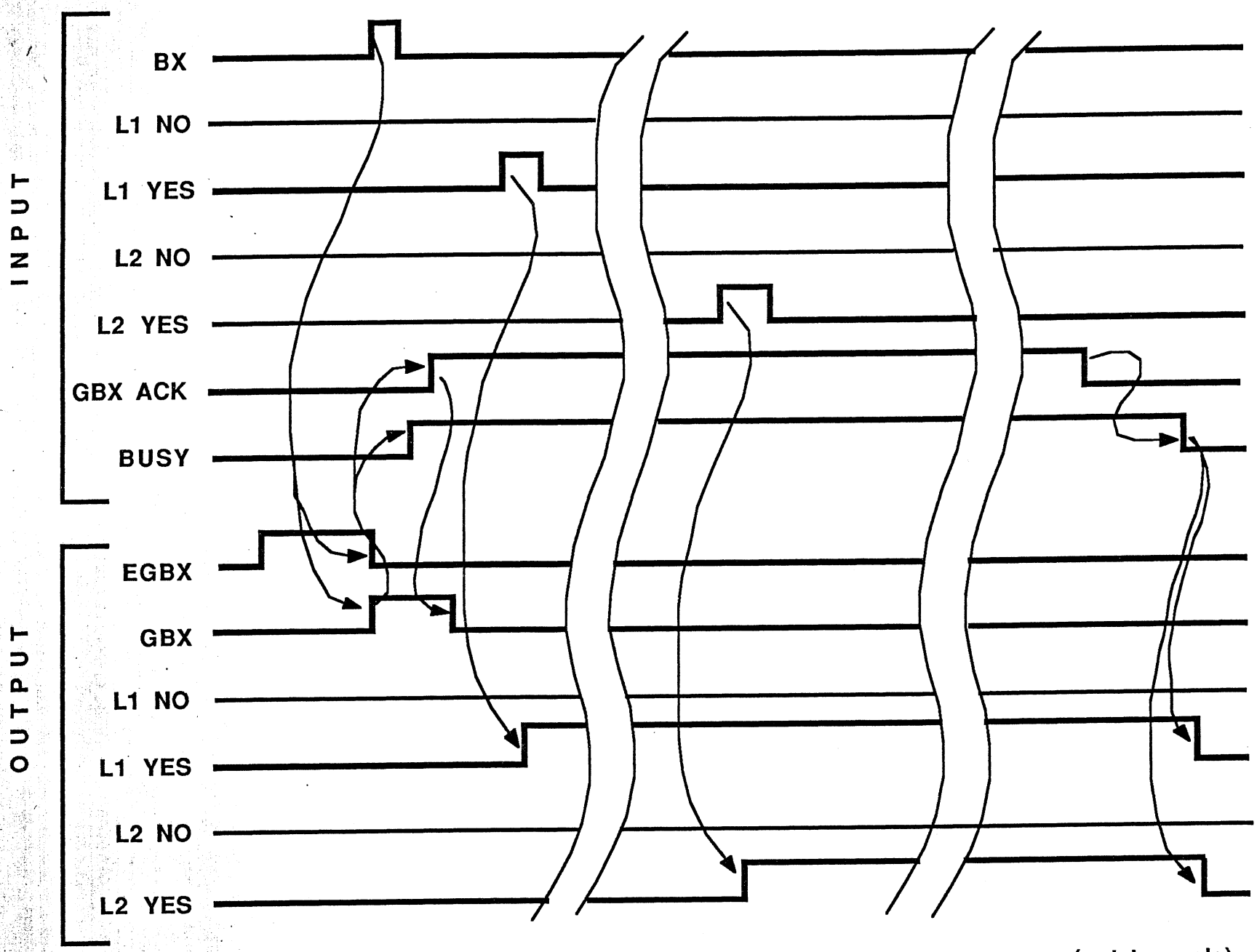

FIG. 2 c : good event

(not to scale)

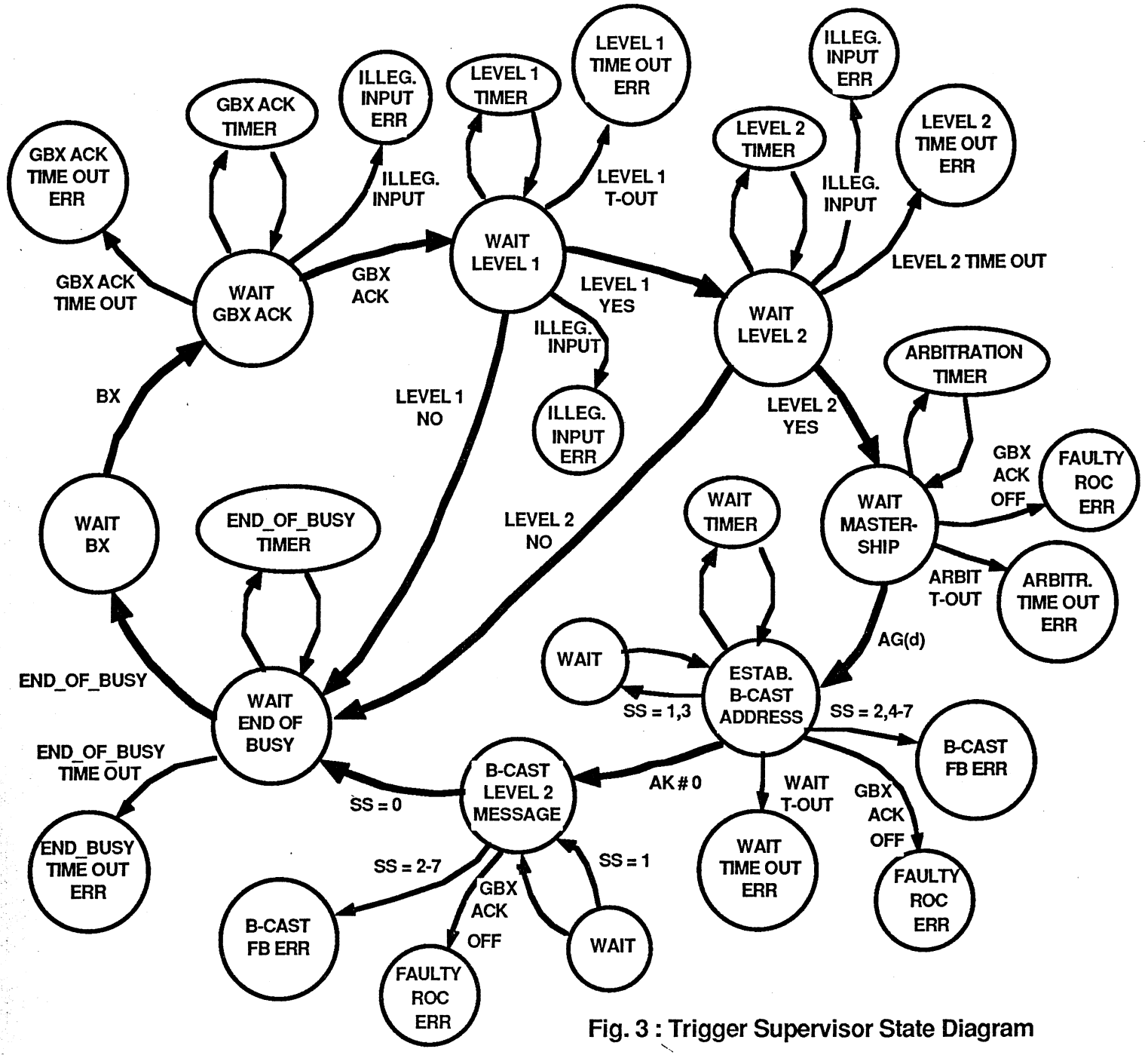

Fig. 3 : Trigger Supervisor State Diagram