CPPM, IN2P3-CNRS et Université d'Aix-Marseille II

Detailed Specification of the ODE- Muon Trigger interface

LHCb Technical Note

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Abstract

This note specifies the electronics interface implemented on the ODE boards to transmit data to the muon trigger processing boards. This interface is based on high speed optical links. The selected components has been qualified against radiation.

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Introduction

This document specifies the electronics interface implemented on the ODE boards transmitting data to the muon trigger processing boards. It is based on high speed optical links running at 1.6 Gb/s with components qualified against radiation.

The optical link interface between an ODE board and a muon trigger processing board consists of two parts:

- **An electronics interface on the ODE boards** containing a low jitter clock distribution circuit, 12 high speed serializers and a parallel transmitter device transforming the 12 electrical signals into optical signals;
- **A physical media between the ODE boards and the muon processing boards. It contains** a ribbon optical fiber with MTP/MPO connector on both sides (~ 10 m), a patch panel, a large cable containing several ribbons each with MTP/MPO connectors on both sides (~ 80 m)and a switch pannel.

In Section A we specify the electronics interface and in Section B the physical media.

A. Electronics interface

The electronics interface on the ODE boards consists of:

- 1 QPLL chip made by CERN for filtering the TTCrx clock jitter;
- a low jitter clock distribution circuit;
- 12 GOL chips from CERN for serialization;
- 1 HFBR-772BE parallel optical transmitter chip from Agilent regrouping 12 channels in a single MTP/MPO connector.

Each ODE board is able to transmit to the trigger board up to 12×32 bits = 384 bits every 25 ns on 12 serial links at 1.6 Gbit/s.

A reference design for the emission chain exists and can be found in [1].

1. TTCrx Jitter filtering system

Initially the LHC clock distributed to the sub-systems was not supposed to be used for optical data transmission. Hence, it does not fulfill the severe jitter constraints required by high speed serializers.

The radiation hard serializer designed by the CERN requires a maximum jitter of 100 ps peak to peak to operate correctly whereas the LHC clock can reach 400 or 500 ps peak to peak.

To reduce the jitter, a radiation hard chip, the QPLL, has been designed by the CERN [2].

This chip receives the clock signal emitted by the TTCrx module. Itfilters out the jitter up to an acceptable value with the help of a reference quartz associated to a phase locked loop. Measurements of the QPLL performance have been made in Marseille during the qualification phase of the final emission design. They are described in [3].

2. Clock distribution

The filtered clock is then sent to the GOL serializers through a clock distribution system. The clock distribution tree is based on the NB100LVEP221 clock repeater from ON semiconductor. This chip is in a technology showing no sensitivity to SEU/SEL[1].

It duplicates a PECL clock to 20 PECL destinations with a very low jitter. Twelve destination only are used since there are only 12 GOLs on the board.

Each clock feeds directly a differential GOL clock input.

1 See J. Whitmore et al. **Radiation validation for the CMS HCAL Front-End electronics**

3. GOL interface

The GOL chip is used in the Fast Ethernet mode in which each byte is converted into a 10-bit word for transmission using a 8B/10B-encoding.

The data path is 32 bits wide.

Two signals control the transmission: *tx_en*, and *tx_er*. The data are transmitted according to Table 1.

When *tx_en* is asserted and *tx_er* is de-asserted then the data bits from pins D [*31..0]* are encoded and transmitted normally.

tx_er	tx_en	Encoded 10 bit output	Use in LHCb
0	0	IDLE (<K28.5>, <D5.6>, <K28.5>, <D16.2>)	Re-synchronization
0	1	Normal data (from din<31:0>)	Data transmission
1	0	Carrier extend (<K23.7>)	Not used
1	1	Transmit error propagation (<K30.7>)	Not used

Table 1: GOL chip in 8B10b mode

When both *tx_en* and *tx_er* are de-asserted a control sequence is emitted. This is used to periodically detect the byte boundary alignment of the bit stream. This detection is also used to periodically reset the state machines on the reception side.

The GOL chip *input* interface requires the following signals:

- *D31* to *D00* input data, and *tx_en* and *tx_er* control signals that are provided jointly by the SYNC chip and external glue logic.
- A *Reset_b* signal that is driven by the L0_Reset signal coming from the on-board TTCrx chip.
- Configuration signals for the GOL registers (I2C bus or JTAG interface) that are provided by the slow control system as described in [4].

The GOL serializes the incoming data on a high speed 1.6 Gbits/s serial stream.

The source of data and its formating depends on the mode of operation of the ODE. Two modes are allowed: *operational* mode and *test* mode.

3.1. Operational mode

In this mode the pad and strip values are sampled in the muon chambers and transmitted to the GOL by the *Sync* chip.

3.1.1. Frame format

The frame formart follows the cycle of the machine and contains 3564 data words. **The first word of the frame is programmable**. It can be either the data related to bunch 0 or the content of an internal register of the *Sync* chip. This allows the ODE boards to send any kind of information to the processing board. For example, this feature can be used to identify the emitting board.

The content of the first word is programmed on the ODE boards through the ECS. It is also through the ECS that both the emitter side and the receiver side are informed about the effective meaning of this word.

The width of the data words is 32 bits. It contains information on the bunch crossing identifiers except for the *idle* words defined in Table 1..

Before the end of the frame a **programmable number of *idle* words** is inserted to systematically reinitialize the memory buffers and the state machines on the reception side as recommended in [5]. This prevents a possible lock-up of the link in case of SEU on the emission side.

Both the emitter and the receiver boards are informed by the ECS of the number of idle words to be used. It can vary between 1 and 32.

The frame format is illustrated in Table 2.

Word	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Tx_er	Tx_en
1st word	Bunch 0 data or content of programmable word																																0	1
2nd word	Bunch 1 data																																0	1
3rd word	Bunch 2 data																																0	1
4th word	Bunch 3 data																																0	1
5th word	Bunch 4 data																																0	1
6th word	Bunch 5 data																																0	1
...	...																																...	...
...	...																																...	...
...	...																																...	...
3557th word	Bunch 3556 data																																0	1
3558th word	Bunch 3357 data																																0	1
3559th word	Idle																																0	0
3560th word	Idle																																0	0
3561st word	Idle																																0	0
3562nd word	Idle																																0	0
3563rd word	Idle																																0	0
3564th word	Idle																																0	0
1st word	Bunch 0 data or content of programmable word																																0	1
2nd word	Bunch 1 data																																0	1
3rd word	Bunch 2 data																																0	1
...	...																																...	...

Table 2: Exemple of frame format for a programmed idle count number fixed to 6

3.1.2. Word data format

The data words are transmitted on 32 bits on the GOL side and received on twice 16 bits on the reception side. To help the detection of demultiplexing errors or synchronization errors, flags are merged with the data as illustrated in Table 3.

The transmission order of the GOL chip is defined as going from the lower to the upper bits: *D [7..0]* is transmitted first, then *D [15..8], D [23..16],* and finally *D [31..24]*. Therefore, as the TLK2501 operates on 16 bits, the 16 lower bits of the GOL word are received first by the TLK2501.

A "switch bit" distinguishes MSB from LSB part. It is placed so that it is always received on *D [0]* for the reception side. A "1" is always attached to the MSB and a "0" to the LSB.

Bit number	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st word	LSB information															0	0
	MSB information															0	1
2nd word	LSB information															1	0
	MSB information															0	1
3rd word	LSB information															0	0
	MSB information															1	1
4th word	LSB information															1	0
	MSB information															1	1

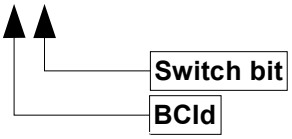

Table 3: Word data format on the reception side

Only the 2 LSB bits of the BCId are transmitted. They are found on the bit *D [1]* of two successive 16 bits words on the reception side. Bits *D [15..2]* for MSB and LSB part contains 14 pads or strips data.

Seen from the ODE, the GOL interface is shown in Table 4.

Bit number	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st word	MSB information														0	1	LSB information														0	0
2nd word	MSB information														0	1	LSB information														1	0
3rd word	MSB information														1	1	LSB information														0	0
4th word	MSB information														1	1	LSB information														1	0

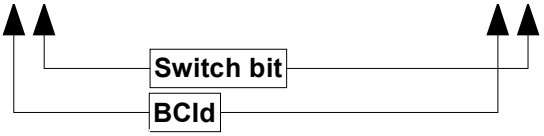

Table 4: Word data format on the emission side

The control bits pattern illustrated in Table 4 is repeated on consecutive words modulo 4 with the addresses.

According to their location in the system, ODE boards can contain between 2 and 4 Sync chips, driving either 7 or 8 bits of data each. However to reduce the number of possible configurations, three generic boards have been designed, resulting in three possible configurations or modes as illustrated in Figure 1.

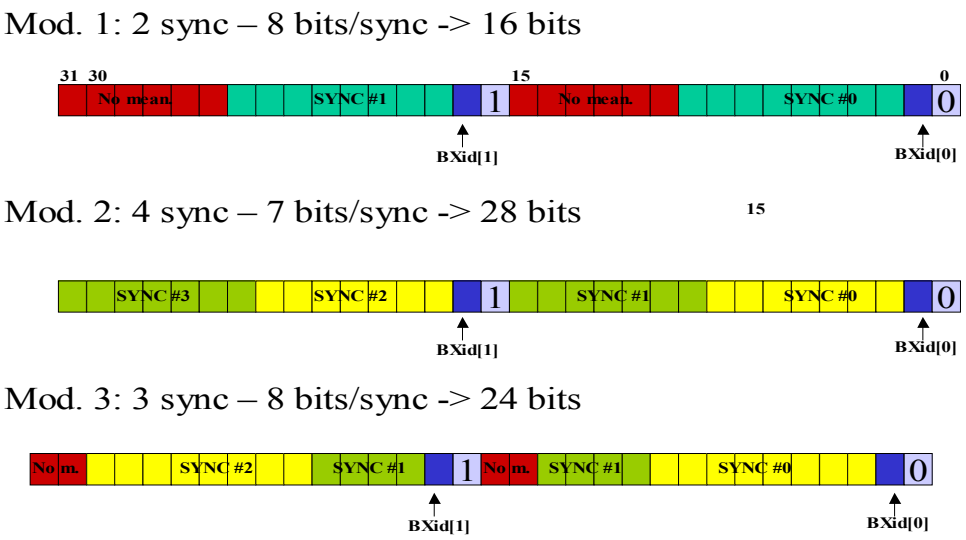

Figure 1: Data word content according to the 3 generic configurations of the ODE board

3.1.3. Time alignment between different links

The *Transmit Enable* control signal of the GOL (*tx_en*) is used to signal the start of a new LHC cycle. **It must be asserted simultaneously with the first data of a machine cycle**. This is essential because the whole time alignment between links on the reception side relies on this condition. The *tx_en* signal must remain asserted as long as there are valid data in the machine cycle. Its de-assertion has to be achieved a few cycles before the end of a machine cycle. The number of cycles during which *tx_en* is deasserted is programmable in the Sync chip between 1 and 32. In this case the number of cycles is referenced backwards starting from cycle 0 and its minimum value is 1.

The frame data format transmitted to the trigger processor is illustrated in Figure 2.

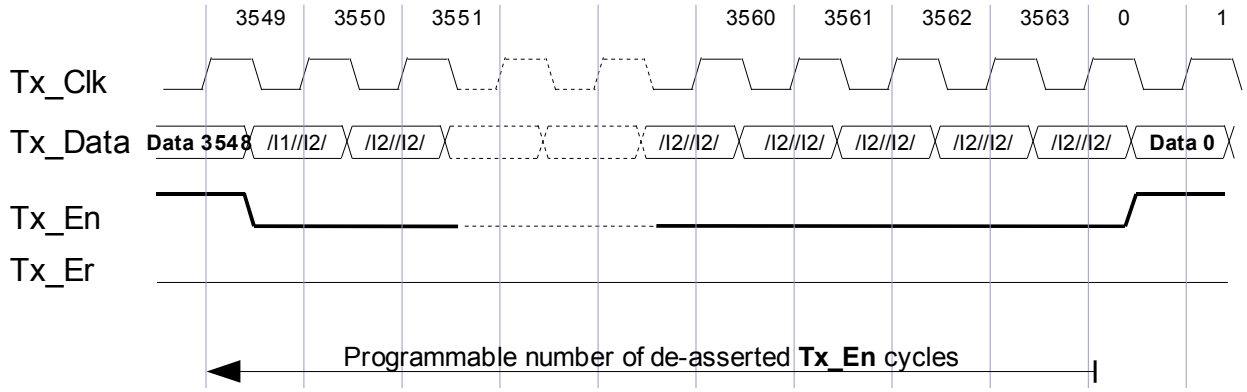

Figure 2: Example of TX_En management on the GOL side

for a running disparity negative at end of cycle 3548

3.1.4. Initialization

After a *L0 front end reset*, the *tx_en* signal must be inactive up to the arrival of the first data of the next LHC cycle as shown in Figure 3.

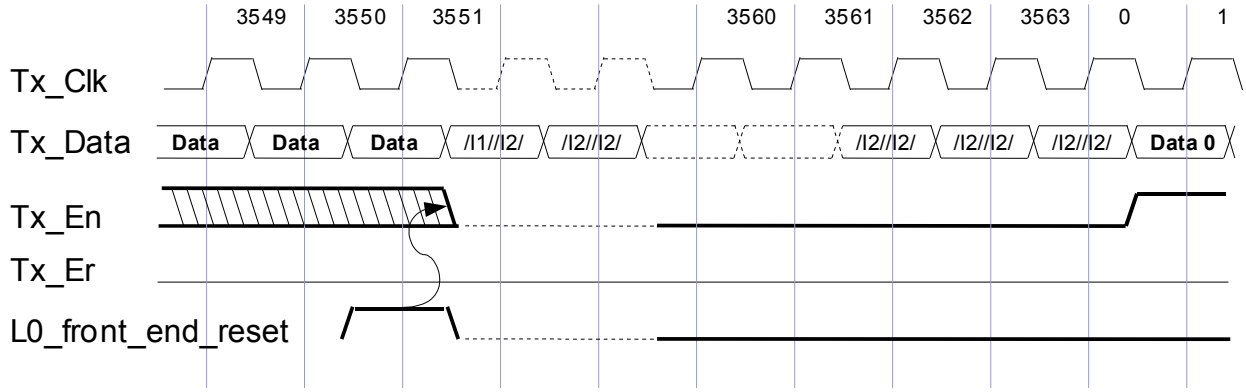

Figure 3: Example of TX_En management on the GOL side after L0 front-end reset

3.2. Test mode

The electrical input of the input signals is the same as in the operational mode. However the content and the sequencing of the data is different. The data come in this case from internal state machine of the GOL under command of the ECS interface.

Three test modes are provided with different levels of complexity:

- A **static test** in which a fixed pattern is sent both on data and controls;
- A **circular tes**t in which a fixed pattern is sent on data but controls signals are automatically toggled;
- A **random pattern test.**

The purpose of these tests is to check that all configurations of input data are transmitted correctly for each individual optical link, to estimate quickly the quality of the link by sending known data words and comma characters (Idle, carrier extend ...) and measuring eye diagrams. They are also used to estimate the Bit Error Rate (BER) of each optical link. Finally they allow to test the data alignment between several links in the context of the LHC cycle.

On the receiver side, the high speed signal is demultiplexed to 32-bit parallel data. These data are then compared to the pattern provided by a generator similar to the one used on the transmitter side.

All the tests are started with the help of the ECS.

3.2.1. Static test

In this test, a fixed pattern is sent on both data and control inputs (tx_en, tx_er) of the GOL. The choice of the pattern is made through the ECS. The purpose of this test is mainly to estimate the quality of the received signal and to measure the deterministic jitter by sending specific repetitive data patterns. The error bit on the reception side can be monitored to provide a raw indication of the error rate.

There is no specific synchronization between the ODE and the processing board. The processing board is informed via the ECS that the ODE is sending such a sequence. An error counter can be started at any moment after the beginning of the test.

3.2.2. Circular test

In this mode, a fixed pattern is sent on the data inputs of the GOL but controls signals are automatically toggled by a 2 bits counter. The sequence is illustrated in Table 5.

Word	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Tx_er	Tx_en
1st word	MSB fixed pattern														0	1	LSB fixed pattern														0	0	0	0
2nd word	MSB fixed pattern														0	1	LSB fixed pattern														1	0	0	1
3rd word	MSB fixed pattern														1	1	LSB fixed pattern														0	0	1	0
4th word	MSB fixed pattern														1	1	LSB fixed pattern														1	0	1	1
5th word	MSB fixed pattern														0	1	LSB fixed pattern														0	0	0	0
6th word	MSB fixed pattern														0	1	LSB fixed pattern														1	0	0	1

Table 5: Control signals sequence modulo 4 on the emission side

Again there is no specific synchronization between the ODE and the processing board. The processing board is informed via the ECS that the ODE is sending such a sequence.

Seen from the muon trigger processing board, due to the 16 bits interface, the sequence differs as illustrated in Table 6.

Bit number	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Tx_er	Tx_en
1st word	Idle word															0	0	0	0
	Idle word															0	1	0	0
2nd word	LSB fixed pattern															1	0	0	1
	MSB fixed pattern															0	1	0	1
3rd word	Idle word															0	0	1	0
	Idle word															1	1	1	0
4th word	LSB fixed pattern															1	0	1	1
	MSB fixed pattern															1	1	1	1
5th word	Idle word															0	0	0	0
	Idle word															0	1	0	0
6th word	LSB fixed pattern															1	0	0	1
	MSB fixed pattern															0	1	0	1

Table 6: Control sequence on the reception side

The idle words received can be either 50BC or C5BC according to the current running disparity. See note [5].

3.2.3. Random test

Linear feedback shift registers (LFSR) are used to implement the pseudo-random pattern generator. They consist of a simple shift register in which some outputs

are X-ORed and sent back to the input as illustrated in Figure 4.

A LFSR of any given size m (number of registers) is capable of producing every possible state during the period $N=2^m-1$, but will do so only if proper feedback taps, or terms, have been chosen. Such a sequence is called a *maximal length sequence* or *m-sequence*.

The feedback sequence $[7, 5, 4, 3]_8$ shown in Figure 4 fulfills the above criteria for an 8 bit random pattern generator. The sequence obtained has a length of 255 words provided that the initial value or *seed* loaded in the registers is not zero. If the seed is zero the sequence produced contains only consecutive zero values. The complete sequence is shown in Tables 10 and 11 of Annex 1.

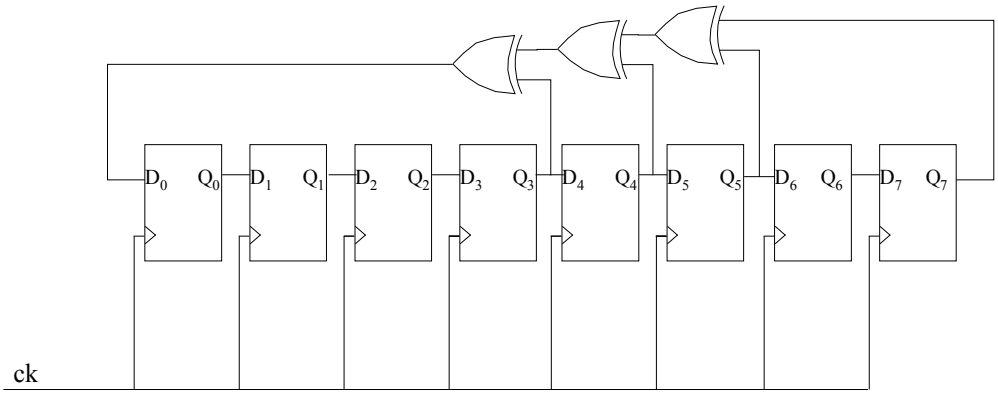

Figure 4: Linear feedback shift register for generating a 255 words sequence

The pseudo-random test generator is based on this principle. It produces the sequence of 4 + 256 words illustrated in Table 7. During the first 4 words the GOL produces idle characters. Then the random sequence begins with the seed programmed in the *Sync* chip. Because the sequence lasts 256 words, the seed is repeated in the last word. See example in Annex 1.

Word	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Tx_er	Tx_en
1st control word	-																																0	0
2nd control word	-																																0	0
3rd control word	-																																0	0
4th control word	-																																0	0
1st data word	0	0	0	0	0	0	12								0	1	0	0	0	0	0	0	12								0	0	0	1
2nd data word	0	0	0	0	0	0	25								0	1	0	0	0	0	0	0	25								1	0	0	1
3rd data word	0	0	0	0	0	0	4B								0	1	0	0	0	0	0	0	4B								0	0	0	1
...	...																																...	...
255th data word	0	0	0	0	0	0	89								0	1	0	0	0	0	0	0	89								0	0	0	1
256th data word	0	0	0	0	0	0	12								0	1	0	0	0	0	0	0	12								1	0	0	1
1st control word	-																																0	0
2nd control word	-																																0	0
...	-																																...	...

Table 7: Random pattern sequence for a mode 1 emission and a seed value = 0h12.

Note that the seed is repeated in the last word because the random sequence is only 255 long

The seed is provided to the emission side as well as the reception side by the ECS.

Seen from the reception side, because of the 16 bits interface, the data and controls received have a different format as illustrated in Table 8.

Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Tx_er	Tx_en
1st control word	Idle word																0	0
	Idle word																0	0
2nd control word	Idle word																0	0
	Idle word																0	0
3rd control word	Idle word																0	0
	Idle word																0	0
4th control word	Idle word																0	0
	Idle word																0	0
1st data word	0	0	0	0	0	0	12								0	0	0	1
	0	0	0	0	0	0	12								0	1	0	1
2nd data word	0	0	0	0	0	0	25								1	0	0	1
	0	0	0	0	0	0	25								0	1	0	1
3rd data word	0	0	0	0	0	0	4B								0	0	0	1
	0	0	0	0	0	0	4B								0	1	0	1
...	...																...	...
255th data word	0	0	0	0	0	0	89								0	0	0	1
	0	0	0	0	0	0	89								0	1	0	1
256th data word	0	0	0	0	0	0	12								0	0	0	1
	0	0	0	0	0	0	12								0	1	0	1
1st control word	Idle word																0	0
	Idle word																0	0
2nd control word	Idle word																0	0
	Idle word																0	0
...	...																...	...

Table 8: Random sequence for a mode 1 reception and a seed value = 0h12

The word format for modes 2 and 3 of the ODE board is shown in Annex 2.

According to the emission mode, the bit organization differs sligthly. In mode 1 two Sync chips feed the GOL data interface. The remaining 12 bits are set to 0 as illustrated in Table 7 and 8. In mode 2, four Sync chips feed the GOL with only the 7 LSB bits of the Random Sequence. In mode 3, three Sync chips provide 8 bits each for a total of 24 bits. The remaining bits are set to 0 like in mode 1.

There is no specific synchronization between the ODE and the processing board. The processing board is informed that the ODE is sending such a sequence by the ECS. The 4 cycles idle sequence is used by the reception side to synchronize a reference random sequence similar to the one produced by the ODE board to which incoming data are compared.

3.3. Serializer output

The serial output of the GOL operates at 1.6 Gbit/s. It drives a 50 Ohm transmission line with Pseudo ECL levels.

It is coupled to the optical emitter in AC coupled mode

4. Optical Transmitter

The HFBR-772BE transmitter from Agilent converts the electrical signal from the GOL chip to an optical one. The circuit drives 12 multimode fibers at a nominal wavelength of 850 nm. It is housed in a MTP/MPO male package as shown in Figure 5.

Figure 5: HFBR-722 transmitter

It is protected against EMI by a noise shield.
It is mounted on a receptaccle and can be easily removed as shown in Figure 6.

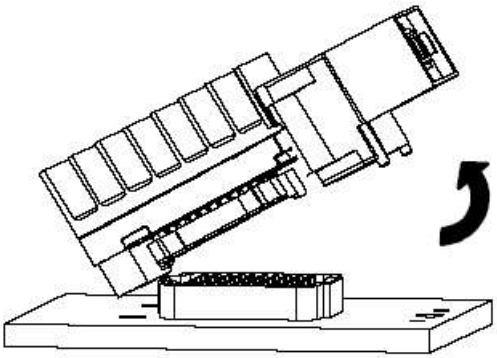

Figure 6: HFBR-722BE receptacle

B. Optical links between ODE boards and processing boards

The optical links are made of multimode 50/125µ cable assemblies with MTP connectors as shown in Figures 7 and 8.

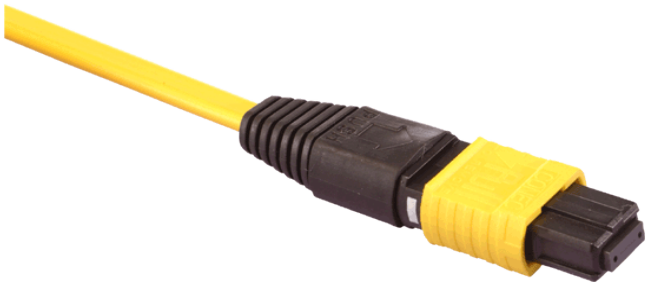

Figure 7: Twelve links ribbon with female MTP connectors

Figure 8: Twelve links ribbon with male MTP connector

To repair the links easily in case of damage, a modular solution has been chosen. It relies on patch and switch panels that are placed both on the emission side and the reception side as illustrated in Figure 9.

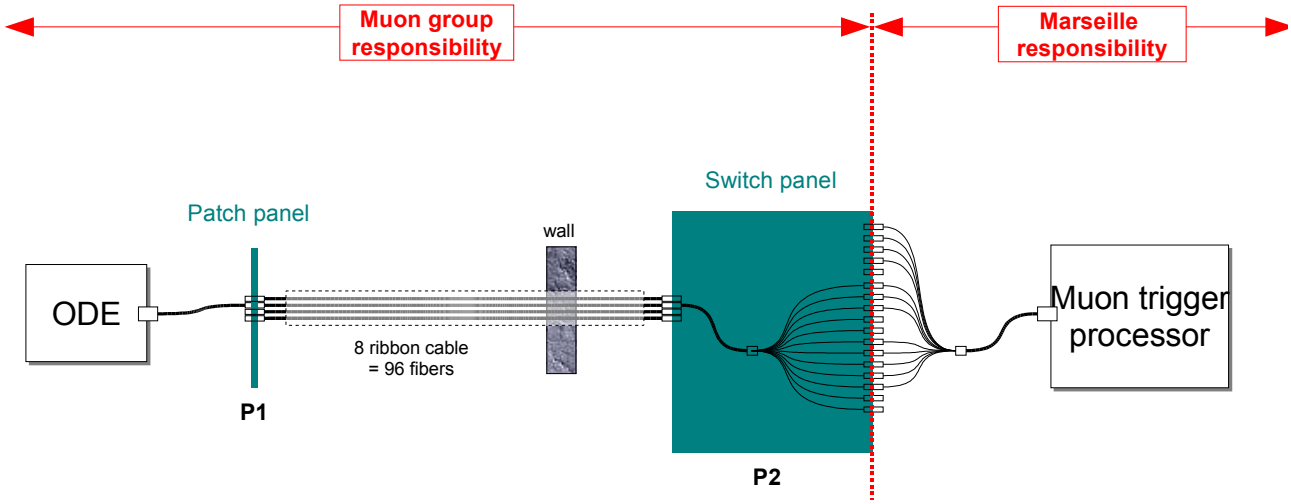

Figure 9: Optical link between the ODE boards and the processing boards

The patch panel P1 is located at approximately 10 meters in average from the ODE. It allows easy replace operations without accessing the cable chain passage. On this panel, mechanical adapters shown in Figure 10 allow the connection of male/female MTP connectors.

Important note : *the adapter is only a mating adapter: the MTP connectors on each side must be of opposite genders.*

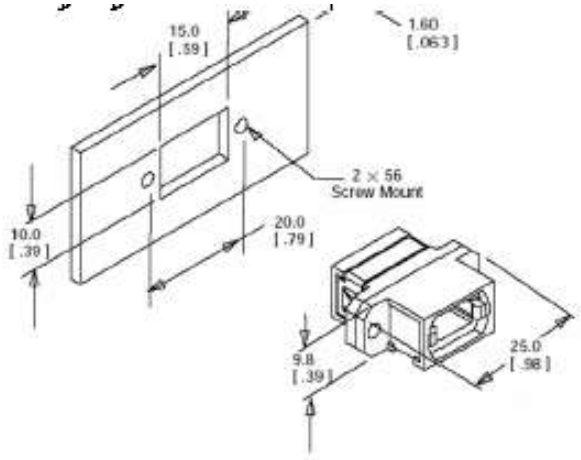

Figure 10: Patch panel mechanical adapters for MTP cables

A large cable including several ribbon cables, like the one described in Figure 11, connects the P1 patch panel through the chicane to the P2 switch panel located behind the wall. The overall length is approximately 80 meters.

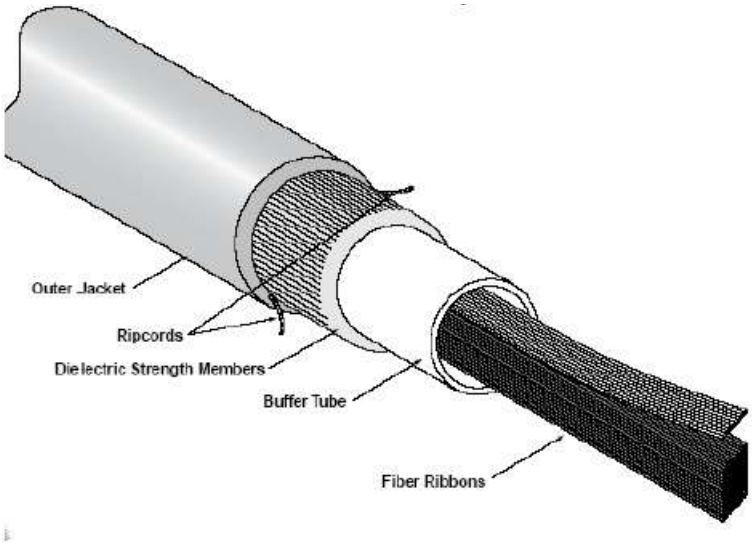

Figure 11: Eight ribbon cable

The role of the P2 switch panel is to split the ribbon cables in order to route the optical links coming from 5 stations to a unique processing board. Splitted ribbon cables like those shown in Figure 12 connect the switch panel to the processing boards.

Figure 12: Splitted optical ribbon

Several solutions are foreseen for making the switch panel. One of them is based on the use of pre-cabled modules as shown in Figure 13.

Figure 13: Pre-cabled MTP/SC or MTP/LC translators

To allow the test of the link without the large 80 meters cable, the following choice of genders has been retained.

Side	Detector side	Cable	Processing side
ODE to P1	MTP female	Ribbon	MTP female
P1 to P2	MTP male	Cable with 8 ribbons	MTP female
P2 switch panel	MTP male	Splitted ribbon	SC or LC female
P2 to Processing board	SC or LC male	Splitted Ribbon	MTP female

Table 9: Cable features

This way it is possible to bypass some parts of the optical path during tests and integration. For example the P1 to P2 part, or P1 to processing board can be shortened if required during the integration phase.

References

[1] http://marwww.in2p3.fr/lhcb/opto/

[2] Aslanides et al., *Synchronization of optical links using the GOL with the TLK2501 or StratixGX buffers,* Note LHCb 2004-012

[3] Paolo Moreira, *QPLL Manual,* CERN-EP/MIC – 2004-01-26

[4] Aslanides et al., *Jitter measurements for the muon trigger optical chain,* LHCb Note in preparation

[5] P. Moreira et al. , *GOL Reference Manual*, CERN-EP/MIC – May 2002 – Version 1.4

Annex 1. Random sequence for a seed value fixed to 0h12

Rank	Binary 7	6	5	4	3	2	1	0	Decimal PRNG 8bit (Dec)	Hexadecimal PRNG 8bit (Hex)
0	0	0	0	1	0	0	1	0	18	12
1	0	0	1	0	0	1	0	1	37	25
2	0	1	0	0	1	0	1	1	75	4B
3	1	0	0	1	0	1	1	1	151	97
4	0	0	1	0	1	1	1	0	46	2E
5	0	1	0	1	1	1	0	0	92	5C
6	1	0	1	1	1	0	0	0	184	B8
7	0	1	1	1	0	0	0	0	112	70
8	1	1	1	0	0	0	0	0	224	E0
9	1	1	0	0	0	0	0	0	192	C0
10	1	0	0	0	0	0	0	1	129	81
11	0	0	0	0	0	0	1	1	3	3
12	0	0	0	0	0	1	1	0	6	6
13	0	0	0	0	1	1	0	0	12	C
14	0	0	0	1	1	0	0	1	25	19
15	0	0	1	1	0	0	1	0	50	32
16	0	1	1	0	0	1	0	0	100	64
17	1	1	0	0	1	0	0	1	201	C9
18	1	0	0	1	0	0	1	0	146	92
19	0	0	1	0	0	1	0	0	36	24
20	0	1	0	0	1	0	0	1	73	49
21	1	0	0	1	0	0	1	1	147	93
22	0	0	1	0	0	1	1	0	38	26
23	0	1	0	0	1	1	0	1	77	4D
24	1	0	0	1	1	0	1	1	155	9B
25	0	0	1	1	0	1	1	1	55	37
26	0	1	1	0	1	1	1	0	110	6E
27	1	1	0	1	1	1	0	0	220	DC
28	1	0	1	1	1	0	0	1	185	B9
29	0	1	1	1	0	0	1	0	114	72
30	1	1	1	0	0	1	0	0	228	E4
31	1	1	0	0	1	0	0	0	200	C8
32	1	0	0	1	0	0	0	0	144	90
33	0	0	1	0	0	0	0	0	32	20
34	0	1	0	0	0	0	0	1	65	41
35	1	0	0	0	0	0	1	0	130	82
36	0	0	0	0	0	1	0	1	5	5
37	0	0	0	0	1	0	1	0	10	A
38	0	0	0	1	0	1	0	1	21	15
39	0	0	1	0	1	0	1	1	43	2B
40	0	1	0	1	0	1	1	0	86	56
41	1	0	1	0	1	1	0	1	173	AD
42	0	1	0	1	1	0	1	1	91	5B
43	1	0	1	1	0	1	1	0	182	B6
44	0	1	1	0	1	1	0	1	109	6D
45	1	1	0	1	1	0	1	0	218	DA
46	1	0	1	1	0	1	0	1	181	B5
47	0	1	1	0	1	0	1	1	107	6B
48	1	1	0	1	0	1	1	0	214	D6
49	1	0	1	0	1	1	0	0	172	AC
50	0	1	0	1	1	0	0	1	89	59
51	1	0	1	1	0	0	1	0	178	B2
52	0	1	1	0	0	1	0	1	101	65
53	1	1	0	0	1	0	1	1	203	CB
54	1	0	0	1	0	1	1	0	150	96
55	0	0	1	0	1	1	0	0	44	2C
56	0	1	0	1	1	0	0	0	88	58
57	1	0	1	1	0	0	0	0	176	B0
58	0	1	1	0	0	0	0	1	97	61
59	1	1	0	0	0	0	1	1	195	C3
60	1	0	0	0	0	1	1	1	135	87
61	0	0	0	0	1	1	1	1	15	F
62	0	0	0	1	1	1	1	1	31	1F
63	0	0	1	1	1	1	1	0	62	3E

Rank	Binary 7	6	5	4	3	2	1	0	Decimal PRNG 8bit (Dec)	Hexadecimal PRNG 8bit (Hex)
64	0	1	1	1	1	1	0	1	125	7D
65	1	1	1	1	1	0	1	1	251	FB
66	1	1	1	1	0	1	1	0	246	F6
67	1	1	1	0	1	1	0	1	237	ED
68	1	1	0	1	1	0	1	1	219	DB
69	1	0	1	1	0	1	1	1	183	B7
70	0	1	1	0	1	1	1	1	111	6F
71	1	1	0	1	1	1	1	0	222	DE
72	1	0	1	1	1	1	0	1	189	BD
73	0	1	1	1	1	0	1	0	122	7A
74	1	1	1	1	0	1	0	1	245	F5
75	1	1	1	0	1	0	1	1	235	EB
76	1	1	0	1	0	1	1	1	215	D7
77	1	0	1	0	1	1	1	0	174	AE
78	0	1	0	1	1	1	0	1	93	5D
79	1	0	1	1	1	0	1	0	186	BA
80	0	1	1	1	0	1	0	0	116	74
81	1	1	1	0	1	0	0	0	232	E8
82	1	1	0	1	0	0	0	1	209	D1
83	1	0	1	0	0	0	1	0	162	A2
84	0	1	0	0	0	1	0	0	68	44
85	1	0	0	0	1	0	0	0	136	88
86	0	0	0	1	0	0	0	0	16	10
87	0	0	1	0	0	0	0	1	33	21
88	0	1	0	0	0	0	1	1	67	43
89	1	0	0	0	0	1	1	0	134	86
90	0	0	0	0	1	1	0	1	13	D
91	0	0	0	1	1	0	1	1	27	1B
92	0	0	1	1	0	1	1	0	54	36
93	0	1	1	0	1	1	0	0	108	6C
94	1	1	0	1	1	0	0	0	216	D8
95	1	0	1	1	0	0	0	1	177	B1
96	0	1	1	0	0	0	1	1	99	63
97	1	1	0	0	0	1	1	1	199	C7
98	1	0	0	0	1	1	1	1	143	8F
99	0	0	0	1	1	1	1	0	30	1E
100	0	0	1	1	1	1	0	0	60	3C
101	0	1	1	1	1	0	0	1	121	79
102	1	1	1	1	0	0	1	1	243	F3
103	1	1	1	0	0	1	1	1	231	E7
104	1	1	0	0	1	1	1	0	206	CE
105	1	0	0	1	1	1	0	0	156	9C
106	0	0	1	1	1	0	0	1	57	39
107	0	1	1	1	0	0	1	1	115	73
108	1	1	1	0	0	1	1	0	230	E6
109	1	1	0	0	1	1	0	0	204	CC
110	1	0	0	1	1	0	0	0	152	98
111	0	0	1	1	0	0	0	1	49	31
112	0	1	1	0	0	0	1	0	98	62
113	1	1	0	0	0	1	0	1	197	C5
114	1	0	0	0	1	0	1	1	139	8B
115	0	0	0	1	0	1	1	0	22	16
116	0	0	1	0	1	1	0	1	45	2D
117	0	1	0	1	1	0	1	0	90	5A
118	1	0	1	1	0	1	0	0	180	B4
119	0	1	1	0	1	0	0	1	105	69
120	1	1	0	1	0	0	1	0	210	D2
121	1	0	1	0	0	1	0	0	164	A4
122	0	1	0	0	1	0	0	0	72	48
123	1	0	0	1	0	0	0	1	145	91
124	0	0	1	0	0	0	1	0	34	22
125	0	1	0	0	0	1	0	1	69	45
126	1	0	0	0	1	0	1	0	138	8A
127	0	0	0	1	0	1	0	0	20	14

Table 10: Random pattern sequence 1/2

Rank	Binary								Decimal	Hexadecimal
	7	6	5	4	3	2	1	0	PRNG 8bit (Dec)	PRNG 8bit (Hex)
128	0	0	1	0	1	0	0	1	41	29
129	0	1	0	1	0	0	1	0	82	52
130	1	0	1	0	0	1	0	1	165	A5
131	0	1	0	0	1	0	1	0	74	4A
132	1	0	0	1	0	1	0	1	149	95
133	0	0	1	0	1	0	1	0	42	2A
134	0	1	0	1	0	1	0	0	84	54
135	1	0	1	0	1	0	0	1	169	A9
136	0	1	0	1	0	0	1	1	83	53
137	1	0	1	0	0	1	1	1	167	A7
138	0	1	0	0	1	1	1	0	78	4E
139	1	0	0	1	1	1	0	1	157	9D
140	0	0	1	1	1	0	1	1	59	3B
141	0	1	1	1	0	1	1	1	119	77
142	1	1	1	0	1	1	1	0	238	EE
143	1	1	0	1	1	1	0	1	221	DD
144	1	0	1	1	1	0	1	1	187	BB
145	0	1	1	1	0	1	1	0	118	76
146	1	1	1	0	1	1	0	0	236	EC
147	1	1	0	1	1	0	0	1	217	D9
148	1	0	1	1	0	0	1	1	179	B3
149	0	1	1	0	0	1	1	1	103	67
150	1	1	0	0	1	1	1	1	207	CF
151	1	0	0	1	1	1	1	0	158	9E
152	0	0	1	1	1	1	0	1	61	3D
153	0	1	1	1	1	0	1	1	123	7B
154	1	1	1	1	0	1	1	1	247	F7
155	1	1	1	0	1	1	1	1	239	EF
156	1	1	0	1	1	1	1	1	223	DF
157	1	0	1	1	1	1	1	1	191	BF
158	0	1	1	1	1	1	1	0	126	7E
159	1	1	1	1	1	1	0	1	253	FD
160	1	1	1	1	1	0	1	0	250	FA
161	1	1	1	1	0	1	0	0	244	F4
162	1	1	1	0	1	0	0	1	233	E9
163	1	1	0	1	0	0	1	1	211	D3
164	1	0	1	0	0	1	1	0	166	A6
165	0	1	0	0	1	1	0	0	76	4C
166	1	0	0	1	1	0	0	1	153	99
167	0	0	1	1	0	0	1	1	51	33
168	0	1	1	0	0	1	1	0	102	66
169	1	1	0	0	1	1	0	1	205	CD
170	1	0	0	1	1	0	1	0	154	9A
171	0	0	1	1	0	1	0	1	53	35
172	0	1	1	0	1	0	1	0	106	6A
173	1	1	0	1	0	1	0	0	212	D4
174	1	0	1	0	1	0	0	0	168	A8
175	0	1	0	1	0	0	0	1	81	51
176	1	0	1	0	0	0	1	1	163	A3
177	0	1	0	0	0	1	1	0	70	46
178	1	0	0	0	1	1	0	0	140	8C
179	0	0	0	1	1	0	0	0	24	18
180	0	0	1	1	0	0	0	0	48	30
181	0	1	1	0	0	0	0	0	96	60
182	1	1	0	0	0	0	0	1	193	C1
183	1	0	0	0	0	0	1	1	131	83
184	0	0	0	0	0	1	1	1	7	7
185	0	0	0	0	1	1	1	0	14	E
186	0	0	0	1	1	1	0	1	29	1D
187	0	0	1	1	1	0	1	0	58	3A
188	0	1	1	1	0	1	0	1	117	75
189	1	1	1	0	1	0	1	0	234	EA
190	1	1	0	1	0	1	0	1	213	D5
191	1	0	1	0	1	0	1	0	170	AA

Rank	Binary								Decimal	Hexadecimal
	7	6	5	4	3	2	1	0	PRNG 8bit (Dec)	PRNG 8bit (Hex)
192	0	1	0	1	0	1	0	1	85	55
193	1	0	1	0	1	0	1	1	171	AB
194	0	1	0	1	0	1	1	1	87	57
195	1	0	1	0	1	1	1	1	175	AF
196	0	1	0	1	1	1	1	1	95	5F
197	1	0	1	1	1	1	1	0	190	BE
198	0	1	1	1	1	1	0	0	124	7C
199	1	1	1	1	1	0	0	1	249	F9
200	1	1	1	1	0	0	1	0	242	F2
201	1	1	1	0	0	1	0	1	229	E5
202	1	1	0	0	1	0	1	0	202	CA
203	1	0	0	1	0	1	0	0	148	94
204	0	0	1	0	1	0	0	0	40	28
205	0	1	0	1	0	0	0	0	80	50
206	1	0	1	0	0	0	0	1	161	A1
207	0	1	0	0	0	0	1	0	66	42
208	1	0	0	0	0	1	0	0	132	84
209	0	0	0	0	1	0	0	1	9	9
210	0	0	0	1	0	0	1	1	19	13
211	0	0	1	0	0	1	1	1	39	27
212	0	1	0	0	1	1	1	1	79	4F
213	1	0	0	1	1	1	1	1	159	9F
214	0	0	1	1	1	1	1	1	63	3F
215	0	1	1	1	1	1	1	1	127	7F
216	1	1	1	1	1	1	1	1	255	FF
217	1	1	1	1	1	1	1	0	254	FE
218	1	1	1	1	1	1	0	0	252	FC
219	1	1	1	1	1	0	0	0	248	F8
220	1	1	1	1	0	0	0	0	240	F0
221	1	1	1	0	0	0	0	1	225	E1
222	1	1	0	0	0	0	1	0	194	C2
223	1	0	0	0	0	1	0	1	133	85
224	0	0	0	0	1	0	1	1	11	B
225	0	0	0	1	0	1	1	1	23	17
226	0	0	1	0	1	1	1	1	47	2F
227	0	1	0	1	1	1	1	0	94	5E
228	1	0	1	1	1	1	0	0	188	BC
229	0	1	1	1	1	0	0	0	120	78
230	1	1	1	1	0	0	0	1	241	F1
231	1	1	1	0	0	0	1	1	227	E3
232	1	1	0	0	0	1	1	0	198	C6
233	1	0	0	0	1	1	0	1	141	8D
234	0	0	0	1	1	0	1	0	26	1A
235	0	0	1	1	0	1	0	0	52	34
236	0	1	1	0	1	0	0	0	104	68
237	1	1	0	1	0	0	0	0	208	D0
238	1	0	1	0	0	0	0	0	160	A0
239	0	1	0	0	0	0	0	0	64	40
240	1	0	0	0	0	0	0	0	128	80
241	0	0	0	0	0	0	0	1	1	1
242	0	0	0	0	0	0	1	0	2	2
243	0	0	0	0	0	1	0	0	4	4
244	0	0	0	0	1	0	0	0	8	8
245	0	0	0	1	0	0	0	1	17	11
246	0	0	1	0	0	0	1	1	35	23
247	0	1	0	0	0	1	1	1	71	47
248	1	0	0	0	1	1	1	0	142	8E
249	0	0	0	1	1	1	0	0	28	1C
250	0	0	1	1	1	0	0	0	56	38
251	0	1	1	1	0	0	0	1	113	71
252	1	1	1	0	0	0	1	0	226	E2
253	1	1	0	0	0	1	0	0	196	C4
254	1	0	0	0	1	0	0	1	137	89
255	0	0	0	1	0	0	1	0	18	12

Table 11: Random pattern sequence 2/2

Annex 2. Word format for random test in modes 2 and 3

Word	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Tx_er	Tx_en
1st control word	-																																0	0
2nd control word	-																																0	0
3rd control word	-																																0	0
4th control word	-																																0	0
1st data word	12							12							0	1	12						12								0	0	0	1
2nd data word	25							25							0	1	25						25								1	0	0	1
3rd data word	4B							4B							0	1	4B						4B								0	0	0	1
...	...																																...	...
255th data word	09							09							0	1	09						09								0	0	0	1
256th data word	12							12							0	1	12						12								1	0	0	1
1st control word	-																																0	0
2nd control word	-																																0	0
...	-																																...	...

Table 12: Random pattern sequence for a mode 2 emission and a seed value = 0h12.

Note that the seed is repeated in the last word because the random sequence is only 255 long

Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Tx_er	Tx_en
1st control word	Idle word																0	0
	Idle word																0	0
2nd control word	Idle word																0	0
	Idle word																0	0
3rd control word	Idle word																0	0
	Idle word																0	0
4th control word	Idle word																0	0
	Idle word																0	0
1st data word	12							12							0	0	0	1
	12							12							0	1	0	1
2nd data word	25							25							1	0	0	1
	25							25							0	1	0	1
3rd data word	4B							4B							0	0	0	1
	4B							4B							0	1	0	1
...	...																...	...
255th data word	09							09							0	0	0	1
	09							09							0	1	0	1
256th data word	12							12							0	0	0	1
	12							12							0	1	0	1
1st control word	Idle word																0	0
	Idle word																0	0
2nd control word	Idle word																0	0
	Idle word																0	0
...	...																...	...

Table 13: Random sequence for a mode 2 reception and a seed value = 0h12

Word	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Tx_er	Tx_en
1st control word	-																																0	0
2nd control word	-																																0	0
3rd control word	-																																0	0
4th control word	-																																0	0
1st data word	0	0	12						1						0	1	0	0	2				12								0	0	0	1
2nd data word	0	0	25						2						0	1	0	0	5				25								1	0	0	1
3rd data word	0	0	4B						4						0	1	0	0	B				4B								0	0	0	1
...	...																																...	...
255th data word	0	0	89						8						0	1	0	0	9				89								0	0	0	1
256th data word	0	0	12						1						0	1	0	0	2				12								1	0	0	1
1st control word	-																																0	0
2nd control word	-																																0	0
...	-																																...	...

Table 14: Random pattern sequence for a mode 3 emission and a seed value = 0h12.

Note that the seed is repeated in the last word because the random sequence is only 255 long

Bit number	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Tx_er	Tx_en
1st control word	Idle word																0	0
	Idle word																0	0
2nd control word	Idle word																0	0
	Idle word																0	0
3rd control word	Idle word																0	0
	Idle word																0	0
4th control word	Idle word																0	0
	Idle word																0	0
1st data word	0	0	2				12								0	0	0	1
	0	0	1				12								0	1	0	1
2nd data word	0	0	5				25								1	0	0	1
	0	0	2				25								0	1	0	1
3rd data word	0	0	B				4B								0	0	0	1
	0	0	4				4B								0	1	0	1
...	...																...	...
255th data word	0	0	9				89								0	0	0	1
	0	0	8				89								0	1	0	1
256th data word	0	0	2				12								0	0	0	1
	0	0	1				12								0	1	0	1
1st control word	Idle word																0	0
	Idle word																0	0
2nd control word	Idle word																0	0
	Idle word																0	0
...	...																...	...

Table 15: Random sequence for a mode 3 reception and a seed value = 0h12