Study of Bump Bonding Technology [#]

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Abstract

Pixel detectors proposed for the new generation of hadron collider experiments will use bump-bonding technology based on either indium or Pb/Sn solder to connect the front-end readout chips to the silicon pixel sensors. We have previously reported large-scale tests of the yield using both indium and Pb/Sn solder bump [1]. The conclusion is that both seem to be viable for pixel detectors. We have also carried out studies of various effects (e.g. storage over long period, effect of heating and cooling, and radiation) on both types of bump bonds using daisy-chained parts on a small scale [2], [3]. Overall, these tests showed little changes in the integrity of the bump connections. Nevertheless, questions still remain on the long-term reliability of the bumps due to thermal cycle effects, attachment to a substrate with a different coefficient of thermal expansion (CTE), and radiation.

I. Introduction

We have carried out studies on effects of temperature changes on both types of bump bonds by observing the performance of single-chip pixel detector assemblies. We have also studied the bumps by visual inspection of bumps bonding silicon to glass substrates before and after thermal cycles and irradiation. We will report the results from these studies and the effect of cryogenic temperatures on the bumps using daisy chained bump-bonds connecting silicon dummies.

II. Silicon-Glass Modules

We have two modules, named AIT_1 and AIT_2, with eight glass chips, which are indium bump bonded to ATLAS tile sensors by AIT (Advanced Interconnect Technologies of Hong Kong). Each chip contains 2934 bumps. Four more modules, where eight glass chips are solder bump bonded to the same type sensors by MCNC of North Carolina, are named MCNC_1, 2, 3 and 4. Each chip in these modules contains 3060 bumps. We video-scanned these modules before and after every test stages they have gone through and recorded the data on 8 mm tapes and DVD+RW's. The coordinate information from the DAQ was superimposed onto the video image so that we could compare the images before and after any procedure. While having the ability of visually inspecting the changes taking place on these modules, it has to be noted that the bonding was between glass and silicon, and not silicon and silicon, as will be the case in real experiment. The CTE (Coefficient of Thermal Expansion) mismatch between silicon and glass, and the possible difficulty in adhesion of under bump metalization (UBM) and bumps to glass were to be considered in the interpretations of the results.

The MCNC modules have gone through the following test procedures:

1. All: 6 cycles of 16 hours at –25C° and 4 hours at room temperature,
2. 1 & 2: Irradiated to 13 MRad (using Co-60),
   3 & 4: 20 cycles of 10 hours at –25C° and 2 hours at room temperature,
3. All: 30 cycles of 6 hours at –25C° and 1 hour at room temperature,
4. 1 & 3 glued on TPG (Thermal Pyrolytic Graphite). All: 105 cycles of 1 hour at –10C° and 1 minute at room temperature (Rapid Thermo Cycling)

The AIT modules have gone through the following test procedures:

1. Both: 5 cycles of 10 hours at –10C° and 4 hours at room temperature,
2. AIT_2 glued on TPG. Both: 105 cycles of 1 hour at –10C° and 1 minute at room temperature (Rapid Thermo Cycling)

A. AIT Modules

Figure 1 shows actual and schematic views of indium bumps. The dark circle in the centre is the UBM (Under Bump Metalization). The indium bump, which is a cylindrical shell, appears as light ring adhered to the glass.

We observed that the indium at some of the bumps degenerated during thermo cycling. Figure 2 shows two such bumps before and after each of two thermal cycling. Degeneration progresses in one bump from one cycling to another. Some bumps had this degeneration before any thermo cycling. Table 1 lists the count of such degenerated bumps before and after each cycling. This effect might cause a change in capacitance of the corresponding electronics channel resulting a noisy readout.

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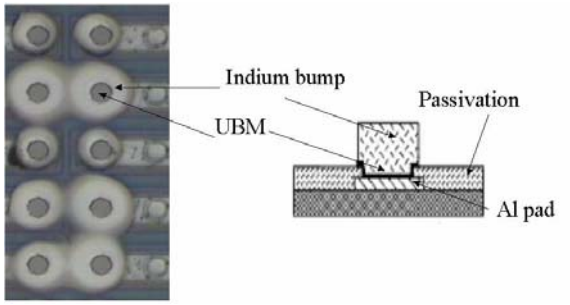

Figure 1: Indium bumps

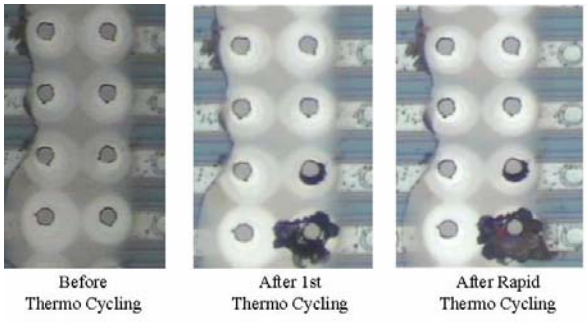

Figure 2: Degeneration at indium bumps

Table 1: Count of degenerated indium bumps

	Existed Before T-Cycling	Created During 1st T-Cycling	Created During Rapid T-Cycling
AIT_1	225 (0.96%)	23	95
AIT_2	255 (1.1%)	28	69

We also observed that the glass chips shifted around during thermo cycling. In Figure 3 we show one corner of the first chip on AIT_1. The inset in each picture indicates the procedure for which the image is taken. Locations of the bumps relative to the structure on the sensors clearly indicate the shift. By studying the other corners of this chip, we concluded that it was originally misaligned during bump bonding. It then moved sideways about 50 μm and rotated counter clockwise during the first thermo cycling. During the second thermo cycling it shifted back to almost its original position with a slight clockwise rotation.

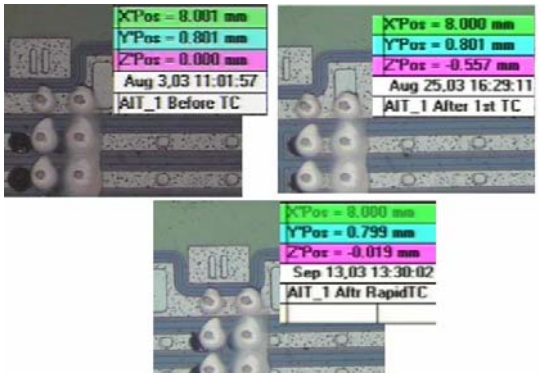

Figure 3: Location of one corner of a chip

The glass chips on the other module, which was glued to TPG before the second thermo cycling did not shift at all, indicating that the CTE mismatch between the TPG and the silicon did not matter in this case.

B. MCNC Modules

Figure 4 shows actual and schematic views of the solder bumps in these modules. The manufacturer used a chemical product called BCB (Benzocyclebutane) for plating and it remained over the UBM. At the bottom of the via of the bumps, the light is reflected up, but not on the walls of the via. This forms the bright circle in the middle and the first dark ring. The light is reflected on the flat part of the UBM again, forming the bright ring. The last dark ring is the solder bump, which is a cylindrical shell.

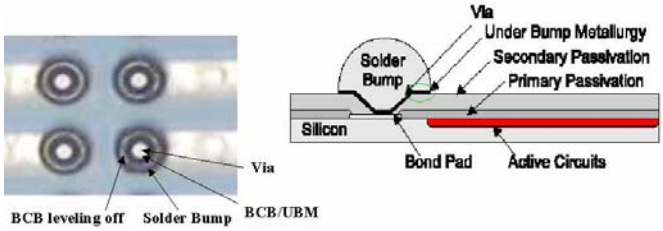

Figure 4: Solder bumps

We observed in some of these bumps that the first dark ring changed colour to blend into the bright circle at the centre. Figure 5 illustrates this colour blending. It occurred originally on ~2% of the bumps, mostly on the edges of the chips. The new occurrences appeared with the second thermo cycling and the irradiation. One of them disappeared during the rapid thermo cycling. Table 2 shows the counts of new occurrences after each process. The module MCNC_1 is excluded because it was damaged during bump bonding procedure.

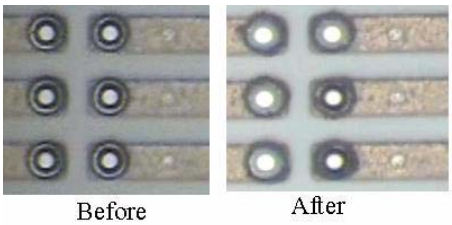

Figure 5: Colour blending of first dark ring

Table 2: Count of new occurrences of first ring blending

MCNC Module	After 1st Cycling	After Radiation	After 2nd Cycling	After 3rd Cycling	After Rapid Cycling
2	0	124	N/A	0	7
3	0	N/A	93	16	99
4	0	N/A	0	3	-1

A possible explanation to this is that, the BCB is lifting off on the walls of the via (with or without cold) and partially reflecting the light causing the colour blending. In one case, the BCB shrinks back to re-create the dark ring. This phenomenon should not cause any problem to the electrical characteristics of the bump.

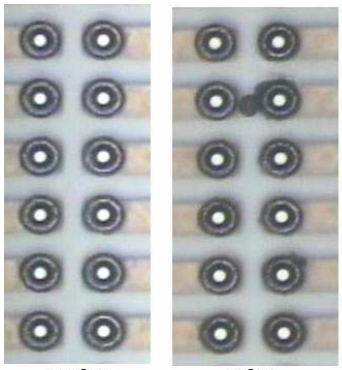

Figure 6: Extrusion developing at solder bumps

We also observed in some of the bumps, development of dark extrusions as shown in Figure 6. These also begin to appear during the second thermo cycling and the irradiation at a rate of ~ 50 per module. They seem to be on the surface (glass side) and mostly on the edge bumps. The vendor suggested they might be due ionic contamination (BCB originated), not completely removed during final cleaning.

We are still investigating with the vendors on the causes of these observed changes. While the bonds seem to remain intact despite these changes, we will do a pull test to study these bumps.

We did not observe any shift on the glass chips due to thermo cycling or due to being glued to the TPG.

III. SINGLE CHIP HYBRID

The BTeV pixel detector will be exposed to significant radiation and to keep it functioning for 5 years or more, it will be operated at a temperature of -5 to -10° C. We studied the temperature dependence of the operation characteristics of the pixel detector. For this study, we used an earlier version of the pixel readout chip developed at Fermilab (FPIX1). Two different FPIX1 chips where tested in a thermal cycle. The first one was assembled on a flex circuit and a SINTEF PSTOP sensor made from low resistivity silicon was bump bonded (indium bumps) to it. A schematic view of the assembly is shown in Figure 7. The second chip was assembled on a PCB and a SINTEF PSTOP sensor made from high resistivity silicon was bump bonded (solder bumps) to it.

To vary the temperature, we used two thermoelectric coolers (Peltier coolers) with the settings and duration controlled automatically by a LabView program.

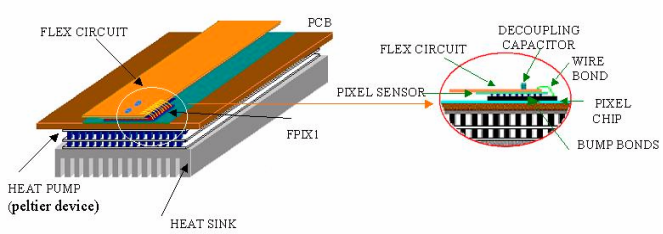

Figure 7: A schematic view of the hybrid assembly

The main goals of this thermo-cycle test were to verify the effect of temperature changes on the bump-bonded connections, on the behaviour of the flex circuit attached to the detector, on the noise and threshold characteristics and dispersion of the readout chips. The details of this study will be presented elsewhere [4]. Here we present in Table 3-6 the effect of a temperature scan on the performance of the chips. The scan for the indium bump detector is shown in Figure 8. Each scan was composed of five runs (cycles) of rising and falling temperatures varying between 7° C, to 69° C for the indium bump detector and 42° C for the solder bump detector.

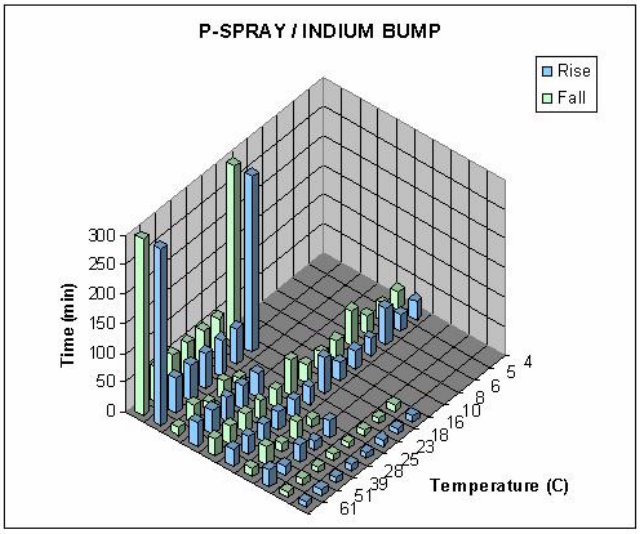

Figure 8: Temperature scan for indium bump detector

Table 3: Channel performance of indium bump detector after the first cycle

% of channels	at 7° C	at 69° C
Working	96.25	61.88
Not Responding	3.20	32.81
Very Noisy	0.55	5.31

Table 4: Channel performance of indium bump detector after all cycles

% of channels	at 7° C	at 69° C
Working	96.02	61.95
Not Responding	3.28	32.27
Very Noisy	0.70	5.78

Table 5: Channel performance of solder bump detector after the first cycle

% of channels	at 7° C	at 42° C
Working	91.25	86.54
Not Responding	8.75	13.17
Very Noisy	0.0	0.29

Table 6: Channel performance of solder bump detector after all cycles

% of channels	at 7° C	at 42° C
Working	91.25	86.54
Not Responding	8.75	13.22
Very Noisy	0.0	0.24

The indium bump detector shows a slightly bigger permanent effect of the thermo cycles compared to the solder bump detector. As we have seen in the cooled glass-silicon modules, the temperature cycling might be damaging the indium bump causing a change in the capacitance of the channel. This in turn results the non-response and/or noisiness we observe on the channels albeit at a very low level (<1%).

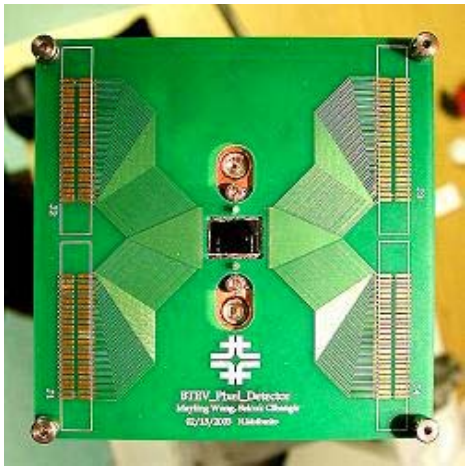

Figure 9: PCB-hybrid assembly for the cryo test

IV. CRYO TEST

The BTeV pixel detector will be operating in a vacuum and be cooled by liquid nitrogen (LN_2). In the event of an accident, the detectors, and therefore the bumps and the wire bonds, might possibly be exposed to cryogenic temperatures. In order to study the effects of such an exposure, we built a cryo vessel that houses a printed circuit board (PCB) on which we installed a dummy hybrid. This hybrid contained 15 channels each with a daisy chain of 32 solder bumps. The channels were wire-bonded to the strips on the PCB and the strips were accessed from outside of the vessel by flat cable connectors. We then measured the electrical resistance of the channels. An open channel (infinite resistance) would indicate a break in either at the bumps or the wire-bond. The hybrid was glued on a TPG, which was glued on a copper plate. The copper plate, and therefore the TPG and the hybrid, were cooled in the vessel by conduction. Figure 9 shows the PCB and the hybrid.

We had two cycles of exposing this PCB-hybrid assembly to LN_2 temperatures and all of 15 channels and their wire-bonds survived with no damage. We have built another PCB-hybrid assembly with 40 channels and will build a few more to extend this study with higher statistics.

V. CONCLUSIONS

The bump bonding technologies with indium and solder are both viable for pixel detectors. The indium bumps look somewhat more susceptible to temperature variations. We visually observed the degeneration of these bumps at cold temperatures. The shift on some of the glass chips we observed can be attributed to the production errors (misalignment) rather than the temperature changes. The solder bumps on the other hand, were not affected by temperature changes or by radiation. The visual changes we observed are superficial in origin and are not expected to cause any operational problems. Furthermore, we observed that, however at low statistics, the solder bumps and the wire bonds as well, are robust enough to withstand the LN_2 temperatures.

The CTE mismatch between the TPG and the silicon of the sensors seems to have no effect on the structural integrity of the bump bonds of either kind.

VI. REFERENCES

[1] S. Cihangir and S. Kwan Nucl. Instr. Meth. A476, 670 (2002).

[2] S. Cihangir et. al., FERMILAB-CONF-01/251-E. Published in the Proceedings of 7th Workshop on Electronics for LHC Experiments.

[3] S. Kwan et. al., FERMILAB-CONF-01/377-E.

[4] M. Turqueti et. al., to be presented at the IEEE Nuclear Science Symposium, Portland, Oregon, USA, Oct. 20-24, 2003.