The CMS Tracker Front-End Driver.

J.A. Coughlan [1], S.A. Baird [1], I. Church [1], E. Corrin [2], C.P. Day [1], C. Foudas [2], E.J. Freeman [1], J. Fulcher [2], W.J.F. Gannon [1], G. Hall [2], R.N.J. Halsall [1], G. Iles [2], M. Noy [2], M. Pearson [1], I. Reid [3], G. Rogers [1], J. Salisbury [1], S. Taghavirad [1], I.R. Tomalin [1], O. Zorba [2]

[1] CCLRC Rutherford Appleton Laboratory, Oxfordshire, UK
[2] Imperial College, London, UK
[3] Brunel University, London, UK

J.Coughlan@rl.ac.uk

Abstract

The Front End Driver (FED) is a 9U 400mm VME64x card designed for reading out the CMS silicon tracker signals transmitted by the APV25 analogue pipeline ASICs. The signals are transmitted to each FED via 96 optical fibers at a total input rate corresponding to 3 Gbytes/s. The FED digitizes the signals and processes the data digitally by applying algorithms for pedestal and common mode noise subtraction. The input data rate is reduced using algorithms that search for clusters of hits. Only the cluster data along with trigger information of the event are transmitted to the CMS DAQ system using the SLINK-64 protocol at a maximum rate of 640 Mbytes/s. All data processing algorithms on the FED are executed in large on-board Field Programmable Gate Arrays (FPGA). Two FED cards have been manufactured during the last quarter of 2002. Results on the performance of the FED are presented and discussed.

I. Introduction

Signals from the silicon strips are amplified and stored in on-detector APV25 ASICs [1], each of which reads 128 strips. On receipt of a Level 1 accept signal the data from multiplexed pairs of APV25s are transmitted along analogue optical links to Front-End Driver (FED) cards in the counting room. A total of 440 FEDs will be needed to readout all 9 million silicon strip channels.

The FEDs digitize the data and perform zero suppression (by cluster finding) before transmitting the data to the central DAQ. At projected CMS trigger rates, the total input data rate on each FED will be approximately 3 Gbytes/s. After zero suppression this is reduced to roughly 50 Mbytes/s/% strip occupancy. The average strip occupancy rates in different regions of the tracker will vary between ~0.5% and 3% in high luminosity LHC running.

This paper provides a status report of the first fully instrumented prototypes of the production FED (called FEDv1). Figure 1 shows the primary and secondary sides of one of the first fully assembled boards. The secondary side contains half of the analogue electronics.

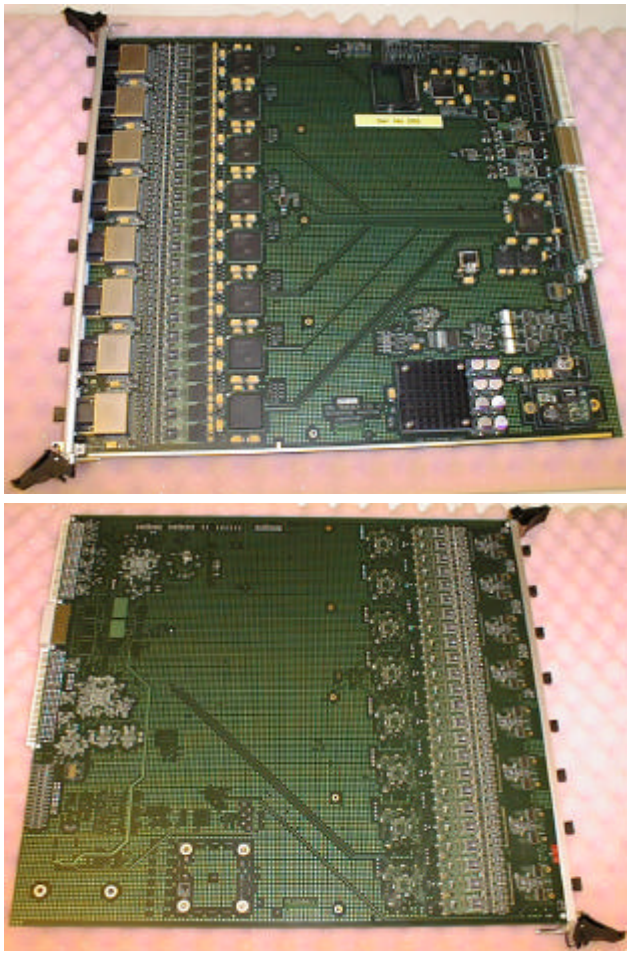

Figure 1: The FEDv1 board primary and secondary sides.

II. Architecture

A full description of the architecture of the FED has been provided in a previous paper [2].

Each FED receives analogue data from eight 12-fibre bundles corresponding to 192 APV25s. The FED front end comprises of 8 identical units each receiving and processing the data from 12 fibres. One Front-End unit consists of:

- One Optical Receiver (OptoRx) module [3], provided by CERN, which receives the optical signals and converts them to electrical using a custom analogue ASIC;
- 6 dual 10 bit ADCs @ 40 MHz (with independent clocks) [4];
- 3 VIRTEX-II XC2V40 (40k gates) FPGAs [5], called delay FPGA, for clock distribution and clock phase adjustment;
- one VIRTEX-II XC2V1500 (1500k gates) FPGA, called the Front-End FPGA, which does the APV25 frame recognition, pedestal subtraction and cluster finding.

The variable length clustered data fragments from all 8 Front-End units are collected on point to point links (4 bits @ 160 MHz) by a single "Back-End" FPGA (XC2V2000). This builds a FED event for each trigger from the data fragments and formats and stores them in an external memory buffer (2 Mbytes deep) to cope with fluctuations in the data rate. The event buffer is implemented with a pair of Quad Data Rate SRAMs (QDRs).

Finally the FED data are transmitted to CMS DAQ via copper links using the S-LINK64 protocol (maximum rate of 640 Mbyte/s). This link is implemented on standard DAQ mezzanine cards carried on VME transition boards. The same FED data buffer can alternatively be read via VME64x (XC2V1000) and this data path will be used during the commissioning phase of the tracker and for calibration and monitoring purposes.

Clock and trigger are generated by on board test logic or received either from VME back-plane signals or via the Timing and Trigger Control system (TTC) [6].

Figure 2 shows a block diagram of the FEDv1 layout.

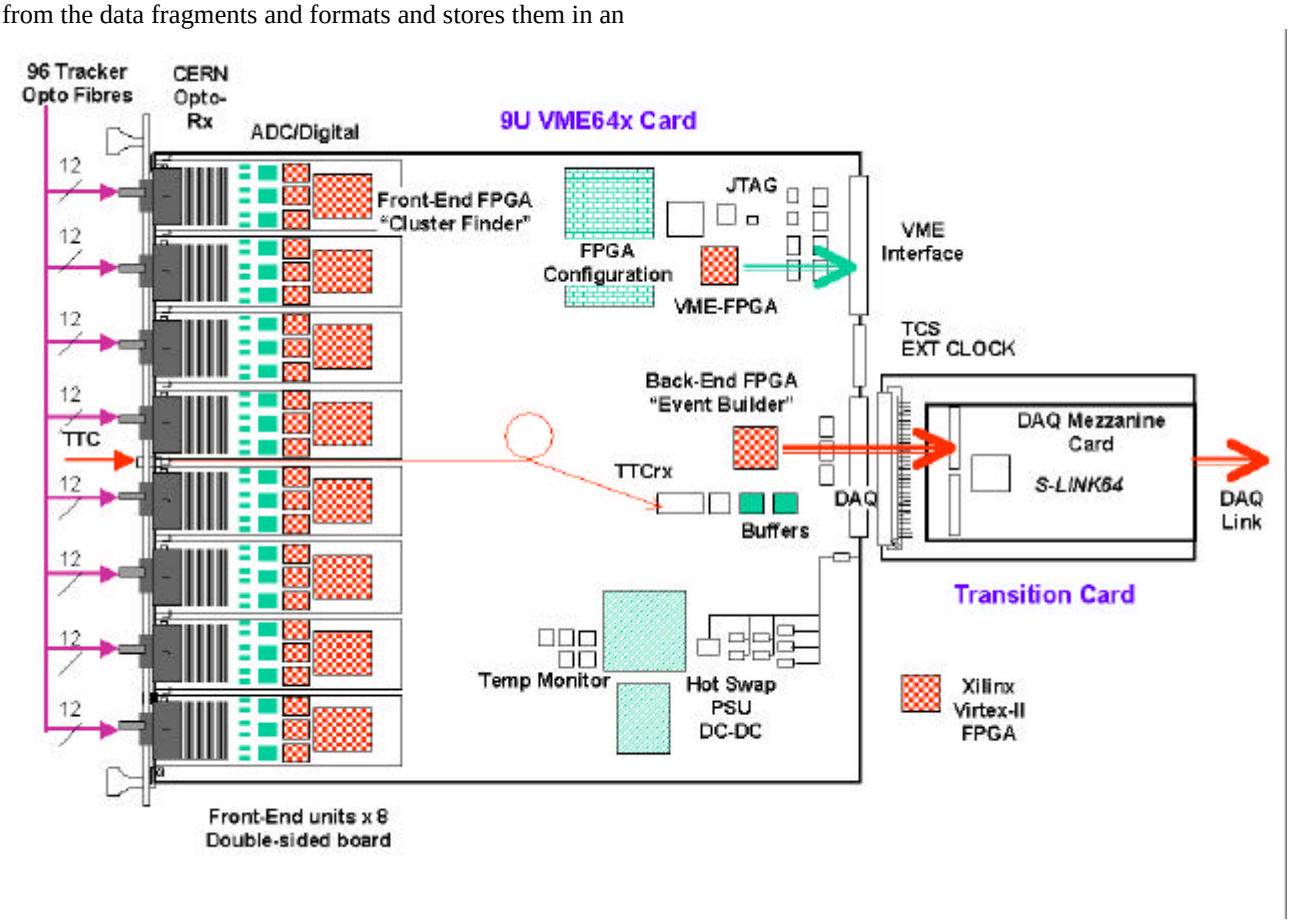

Figure 2: 9U FED board layout with DAQ transition card.

III. Board Design and Status

The FED has been implemented to minimise PCB manufacturing and assembly costs. The card is double-sided to accommodate the high density of components in the analogue section. The total component count is approximately 6,000 with approximately 25,000 tracks. The larger FPGA devices have 676 pins as Ball Grid Arrays (BGA) on a 1mm pitch. The number of signal termination resistors is reduced by the use of the Digitally Controlled Impedance feature of Virtex-II. Digital links are kept separated from analogue signals to avoid interference.

The signal interconnection scheme has been kept as simple as possible to ease layout and routing. There are no inter-connections between neighbouring Front-End modules and all high-speed connections are point to point. The number of FPGA signal interconnects is minimised by the use of Double Data Rate I/O links.

The board has 14 layers, including 6 for power and ground. The board thickness is 2mm. Particular care was taken in de-coupling, especially of the Virtex II FPGAs. The total power consumption of the board has been measured to be approximately 100 W, which is within standard LHC crate limits.

About 10 FEDv1s have been manufactured to date. The build quality has been generally very good. There have been no BGA related faults detected. Minor faults have been associated mainly with the soldering of the components with the smallest footprints (size 0402). Minimising manufacturing errors will be critical when one considers the effort required for fault finding in final production quantities.

IV. Firmware Status

The first FEDv1 boards are destined for use in large scale assembly (LSA) tests of the silicon tracker. These tests require a restricted functionality compared to the final CMS readout needs. Most importantly cluster finding and fast S-LINK readout are not required.

The firmware is implemented in a mixture of VHDL and Verilog. The first boards were manufactured before the design of the final firmware for the Back-End and VME FPGAs had been completed. This firmware was implemented in parallel with board testing.

The following functions have passed preliminary tests:

- Capture of raw data in response to software or external triggers. This mode of operation is required during the synchronisation and calibration of the tracker system [7].
- APV frame finding capture (with cluster finding disabled). This mode of operation is required for standard raw data readout.
- Individual clock skewing adjustment on all 96 ADC channels. This functionality has been implemented using the unique feature of the Xilinx Digital Clock Manager (DCM) cores present in Virtex-II FPGAs. The skews may be dynamically set in fine steps (of approximately 800 ps) across a full clock period of 25 ns (Figure 3) and in coarse steps of whole clock periods. The jitter measured on the clocks is approximately 300 ps.
- The event building logic has been demonstrated at the full QDR data transfer rates of 640 Mbytes/s. Adjustment of the timing of the DCM clocks to meet the timing requirements of the QDR proved critical. Header information is appended to the data payload to provide synchronisation and error detection information on each front-end channel for off-line monitoring.
- VME readout of events (including full raw data size of 50kbytes) in single cycle and block transfer modes. VME64x addressing is achieved using a simple geographic slot decoding scheme.

The following functions necessary for LSA tests have still to be demonstrated:

- Receipt of stable clock and triggers via TTC system.
- Output of throttle signals indicating potential FED buffer overflows to trigger system.
- Temperature sensor monitoring.

V. Testing

Following preliminary power measurements, the first operation carried out on each board is a JTAG chain Boundary Scan [8] test. All connections between digital devices and some connections to analogue components are conveniently verified using these tools. These tests will be essential for early verification of board quality during mass production.

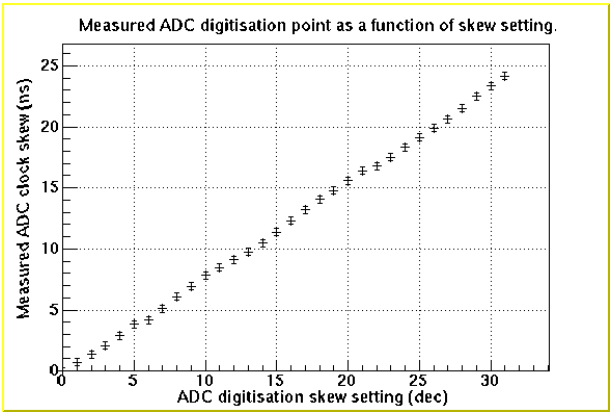

Figure 3: Fine clock skew settings.

There are a total of 34 FPGAs on board ranging from 40k to 2,000k equivalent gate count. The VME-FPGA has a dedicated EPROM for power on configuration. The remaining FPGAs are configured using the Xilinx System ACE CF product [9]. The FPGA configuration files are stored in standard removable Compact Flash cards. This system has proved extremely reliable and efficient. The entire board takes less than 10 seconds to boot up. The System ACE controller is also interfaced to the VME FPGA to permit the future implementation of in-situ reprogramming.

Since the final firmware was not available when board testing commenced, the initial examination of the Front-End analogue chain were carried out using Xilinx Chip Scope Pro Core logic [10]. These tools provide logic

analyser blocks placed inside the FPGA logic, which are readout via the JTAG chain, and proved extremely useful in providing early visualisation of the data before VME readout was available (Figure 4.) They continue to be invaluable in providing in-situ debugging of firmware operation.

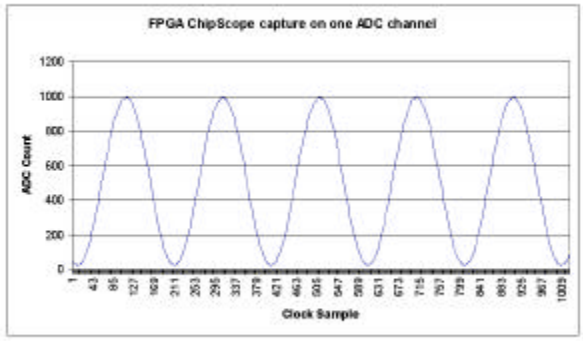

Figure 4: Example of signal generator input data captured using ChipScope logic analyser tool.

The earliest tests were carried out before OptoRx modules were assembled on the boards. Electrical inputs were provided by a purpose built test card (Figure 5), which plugs onto a connector behind the OptoRx module. A programmable analogue cross-point switch [11] passes any of its 3 single-ended inputs to any of the 12 FED analogue channels in a Front-End unit. Eight such cards can be chained together to drive electrical inputs on all 96 channels on the FED simultaneously.

Figure 5: The cross-point switch based electrical test cards.

Preliminary characterisation studies with optical inputs were achieved using a basic set of test firmware together with a prototype Opto-Tester board (6U VME) which was capable of driving data patterns on up to 3 FED input channels simultaneously.

Measurements of pedestals (Figure 6) show a worst-case channel rms noise level of order 1.1 counts (equivalent to 350 electrons).

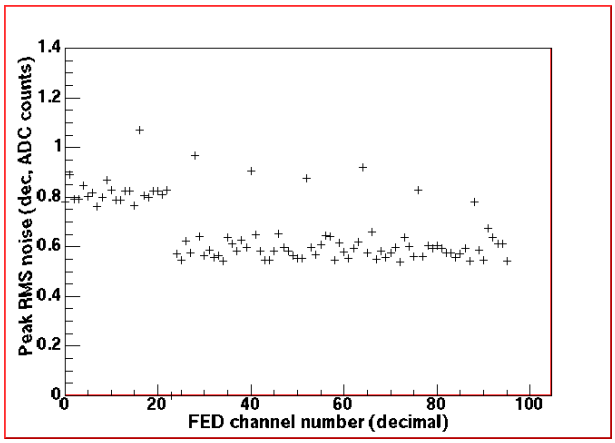

Figure 6: Peak rms noise vs FED channel (N.B. only the first 24 channels are connected to OptoRx module outputs).

By varying a TrimDAC offset available on each ADC channel input the linearity of the ADC response has been verified (Figure 7).

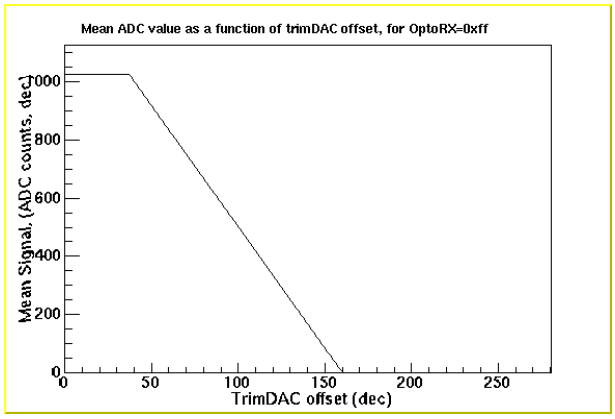

Figure 7: Mean ADC count as a function of TrimDAC offset (for a fixed OptoRx offset setting.)

For evaluation and production testing, a more sophisticated Opto-Tester board (9U VME) has been designed [12]. This card is capable of driving arbitrary data patterns, including APV25-like frames, on up to 24 FED input channels simultaneously.

Figure 8 shows an example event read out from the FED containing APV frames generated by the 9U Opto-Tester on all 12 channels of a Front-End unit. This plot illustrates several programmable features of the FED. A coarse clock skew delay has been set on the first 4 channels. The fine clock skew has been adjusted on several channels. The 2nd channel input has been disabled. The 12th channel has been set to full scale by adjustment of the TrimDAC.

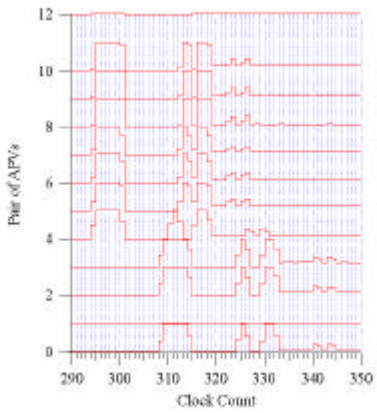

Figure 8: Example readout with FED of data from 9U Opto-Tester on one Front-End unit (Each line represents the ADC count on a given channel versus clock sample.)

VI. Future Plans

The FEDv1 design has so far met functional requirements with only minor modifications. The majority of these are concerned with the sequencing and monitoring of power on the board. The first pair of boards will be delivered next month to CMS for use in LSA tests of the silicon tracker.

The remaining firmware functionality required for the final CMS readout system will be implemented during the next 6 months. In parallel with this effort, detailed and quantitative evaluation of the FED analogue performance, including optical tests driving all 96 FED input channels, will continue in UK.

The manufacture of a small quantity of pre-production boards FEDv2 is foreseen by mid 2004. Full production of the 500 FEDs (including spares) is planned to commence early in 2005 in order to meet the overall CMS tracker schedule of system installation and commissioning, which is scheduled in mid 2005.

VII. Acknowledgements

The authors would like to thank the following: Marcus French (RAL) and Mark Raymond (Imperial College) for their contributions to the design of the FED analogue circuitry. Francois Vasey (CERN) and Jan Troska (CERN) for their assistance with the integration of the opto-receiver modules. Bruce Taylor (CERN) and Paulo Moreira (CERN) for their assistance in integrating the TTCrx. Imperial College electrical workshop for their support work. They would also like to acknowledge the contributions of Attila Racz (CERN), Bill Haynes (RAL) and Joao Varela (CERN) to the design of the DAQ and trigger interfaces and Alessandro Marchioro (CERN) for many helpful discussions. They also wish to acknowledge the support of PPARC.

VIII. References

[1] M. Raymond et. al., “The CMS Tracker APV25 0.25µm CMOS readout chip”, *Sixth Workshop on Electronics for LHC Experiments*, CERN/LHCC/2000-041.

[2] S.A. Baird et. al., “The Front-End Driver card for the CMS Silicon Strip Tracker Readout.”, *Eighth Workshop on Electronics for LHC Experiments*, CERN/LHCC/2002-034.

[3] *cms-tk-opto.web.cern.ch/cms-tk-opto/*

[4] AD9218 manufactured by Analog Devices, Inc., *www.analog.com*

[5] Xilinx, “Virtex-II Platform FPGA Handbook”, *www.xilinx.com*

[6] *ttc.web.cern.ch/TTC/intro.html*

[7] K. Gill et. al., “Synchronisation of the CMS tracker”, these proceedings.

[8] C.M. Maunder and R.E. Tulloss, “*The Test Access Port and Boundary-Scan Architecture”*, IEEE Computer Society Press, Los Alamitos CA, 1990.

[9] Xilinx, “System ACE CF Compact Flash Solution”, *www.xilinx.com*.

[10] Xilinx, “Chip Scope Pro”, *www.xilinx.com*.

[11] AD8116 manufactured by Analog Devices, Inc., *www.analog.com*

[12] G. Iles et. al., “A Testing Device for the CMS Silicon Tracker Front End Driver Cards”, these proceedings.