The Token Bit Manager Chip for the CMS Pixel Readout

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Abstract

A custom chip that controls groupings of pixel readout chips and coordinates their readout has been developed for the CMS experiment. The performance of this chip produced in the DMILL process and the translation of the chip to 0.25 μm process is presented.

I. Introduction

The Token Bit Manager (TBM) is a critical element of the front-end readout for the CMS pixel detector. It is a custom, mixed-mode, radiation-hard IC that controls and orchestrates the readout of a group of pixel ReadOut Chip (ROCs). The TBM is designed to be located on the detector near to the pixel ROCs. In the case of the barrel, they will be mounted on the detector modules and will control the readout of 8 or 16 ROCs depending upon the layer radius. In the case of the forward disks, they will be mounted on the disk blades and will control the readout of 21 or 24 ROCs depending on blade side. [1] A TBM and the group of ROCs that it controls will be connected to a single analog optical link over which the data will be sent to the Front End Driver, a flash ADC module located in the electronics house. The relationship of the TBM to the group of ROCs it controls is shown in Figure 1.

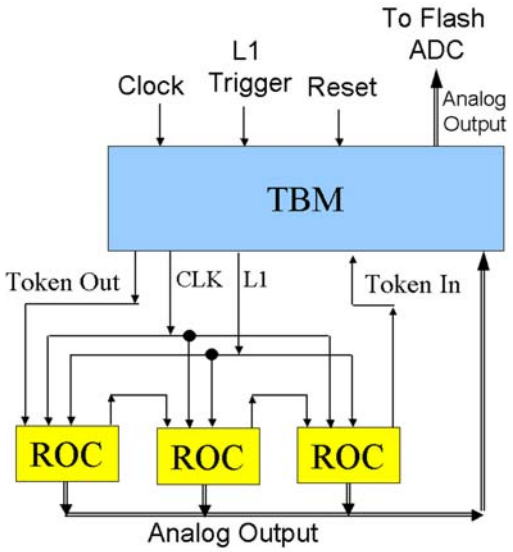


Figure 1: Schematic of a readout chain consisting of a TBM and a group of ROCs.

The principle functions of the TBM include the following.

- It will control the readout of the ROCs by initiating a token pass for each incoming Level 1 trigger.
- On each token pass, it will write a header and a trailer word to the data stream.
- The header will contain an 8-bit event number and the trailer will contain 8-bits of error status. These will be transferred as 2-bit analog encoded digital.
- It will distribute the Level 1 triggers, and clock to the ROCs.
- Each arriving Level 1 trigger will will be placed on a 32-deep stack awaiting its associated token pass. Normally the stack will be empty but is needed to accommodate high burst rates due to either noise, high track density events or trigger bursts.

Since there will be two analog data links per module for the inner two layers of the barrel, the TBMs will be configured as pairs in a Dual TBM Chip. A block diagram of the Dual TBM chip is shown in Figure 2. In addition to two TBMs, this chip also contains a Control Network.

The Hub serves as a port addressing switch for control commands that are sent from the DAQ to the front-end TBMs and ROCs. These control commands will be sent over a digital optical link from a Front End Controller (FEC) in the electronics house to the front-end hubs. The commands will be sent using a serial protocol, similar to the I^2C protocol [2], but modified to run at a speed of 40 MHz. This high speed is mandated by the need to rapidly cycle through a refreshing of the pixel threshold trim bits that can become corrupted due to single event upsets (SEU). There are four external ports on each Hub for communicating with the ROCs and there is one internal port for communicating with the TBMs within the chip. The first byte of each command will contain a 5-bit hub address and a 3-bit port address. When a Hub is addressed, it

selects the addressed port, strips off the byte containing the hub/port address and passes the remainder of the command stream unmodified onto the addressed port. The outputs of the external ports consist of two low voltage differential lines for sending clock and data.

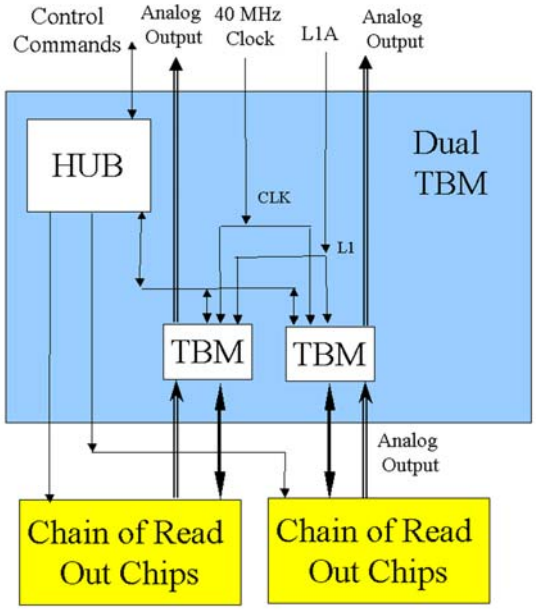


Figure 2: Block diagram of the Dual TBM chip.

II. The Dual TBM Prototype

Although the production Dual TBM chip that will be used in CMS will be built in a 0.25 deep submicron process, the first prototype of the TBM has been produced in the 0.8 micron, SOI, radiation-hard, DMILL process [3].

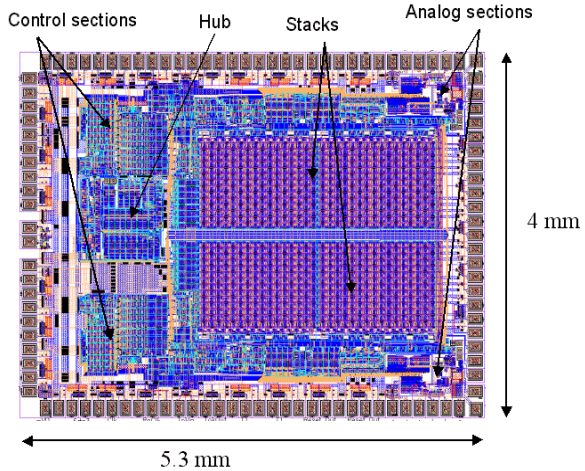
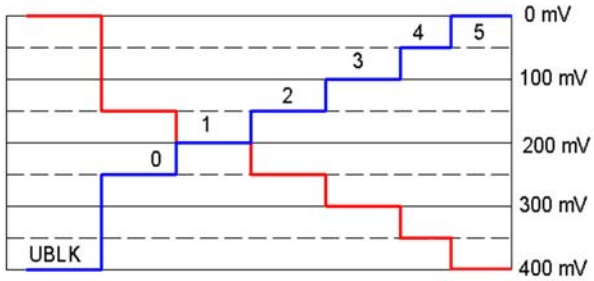


Figure 3: Layout of the Dual TBM chip.

Although the Dual TBM is predominantly a digital chip, an analog section is needed for writing the header and trailer information to the analog output. The analog output uses four levels of information and an additional “ultrablack" level that marks the start of the header and trailer. The output levels produced are shown in Figure 4. They are chosen to match the corresponding levels produced by the ROCs. The ROCs will produce six levels of analog information plus an ultrablack. The TBM uses only the lower four levels.



Signal	Differential Voltage
UBLK	-400 mV
0	-100 mV
1	0 mV
2	+100 mV
3	+200 mV

Figure 4: Output levels of the Dual TBM chip. Voltages referenced to Analog Optical Link input. Levels 4&5 are used by ROC only.

It is essential to have full adjustability of the analog output levels, since there may be large chip-to-chip variations. Also, the TBM output levels should be aligned to the corresponding levels of the readout chips that are connected to the same analog line. The Dual TBM analog output stage in shown in Figure 5. It is driven by a multiplying DAC whose gain can be adjusted by a current source. This is followed by a buffering amp and then by a differential driver. The differential driver has both an adjustable offset and a driver current adjustment. In combination, these three adjustments allow for setting of the offset, gain and the differential zero crossing of the differential output.

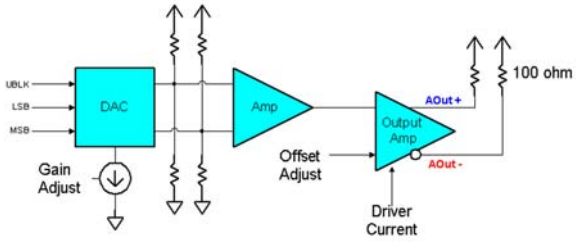


Figure 5: Analog output section of the Dual TBM chip.

An extensive set of control commands have been built into the TBM. These allow various functions and operating modes of the TBM to be controlled by issuing commands to the TBM over the control network described above. The more important of these commands are:

- Analog adjustment
  - adjustment of the analog levels described above
  - enabling and disabling of the analog output
- Trigger Control
  - injection of any trigger type
  - ignoring of incoming triggers
  - enabling and disabling of the trigger output
- Token Passing
  - enabling and disabling of the token passing
- Stack Control
  - read back of the number of events on the stack
  - read back (non-destructively) of stack contents
- General Control
  - switching of the readout speed between 40 MHz and 20 MHz
  - enabling and disabling of the TBM clock
  - reset of the TBM

III. Initial Prototype Results

The DMILL Dual TBM prototype was delivered in May 2002. The functionality of several of the delivered chips have been fully tested. Figure 6 shows the measured response of the DMILL TBM, operating at the full readout clock speed of 40 MHz, upon receipt of a trigger.

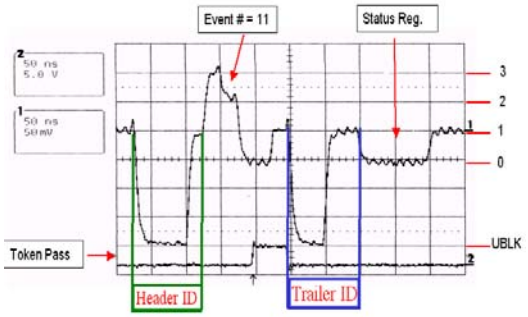


Figure 6: Header and Trailer output for a typical event.

When the trigger is received, the TBM outputs a header ID consisting of three “ultrablack” levels followed by a “1”. The next four clocks contain an 8-bit analog-encoded event number. In the case of the event shown in the figure, the particular event number is 11. Following the header, the TBM issues a token to the first ROC on the readout chain. The ROCs would then place their ID and any hit information onto the data stream and pass the token along. Since in the present test there were no ROCs connected to the TBM, the token is immediately returned to the TBM. Upon receipt of the returned token, the TBM outputs a trailer ID which consists of two “ultrablack" levels followed by two “1”s. The next four clocks contain an 8-bit analog-encoded error status word. In these tests, we have determined that the event number is correctly incremented and reported in the header. In addition, all of the status bits in the trailer are correctly set and cleared. Six Dual TBM chips have been tested. Of these, five are fully functional while one has a dead short somewhere in the power lines of the chip.

The adjustment of the TBM analog outputs works well. The need for this adjustability along with the capability is demonstrated in Figure 7. The top two plots show the outputs of two TBMs before any adjustment is made. The chip-to-chip variation is clearly very pronounced. The lower two plots show the outputs very well matched after adjustment.

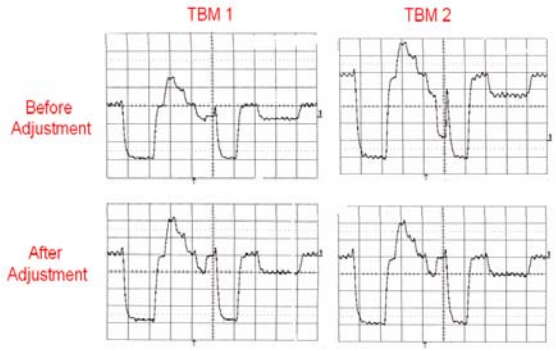


Figure 7: Adjustability of the analog output levels.

In order to see how far beyond design specifications the chip could be run, it was tested with an input trigger rate of 1 MHZ. This far exceeds design requirements since, in normal running, the CMS Level 1 trigger rate is expected to be 30 KHz with possible brief bursts to 100 KHz. Figure 8 shows the output of a TBM chip for a 1 MHz input trigger rate. In this figure, multiple traces for several outputs have been overlaid. The TBM clearly is able to function at this trigger rate. The whole range of 256 event numbers is seen in the header output while the other features: header ID, trailer ID and error status word are indistinguishable from event to event.

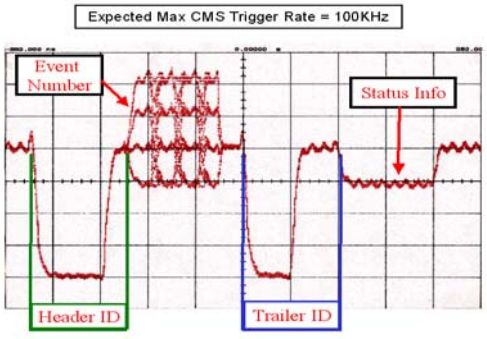


Figure 8: Performance of Dual TBM chip at an input trigger rate of 1 MHz. Outputs of several events are over lain.

The internal fast port that communicates with the TBMs and the four external fast ports that communicate with the

ROCs have also been fully tested and found to be fully functional.

The Dual TBM prototype chip fully functions as designed at the full clocking speed of 40 MHz.

The power consumption of the dual TBM chip is an issue. In the case of the barrel modules, the Dual TBM chip will be located on a hybrid that sits on top of the pixel sensors. The heat generated by the TBM will have to pass through the sensors before reaching the cooling structure. The power consumption of the Dual TBM chip is, therefore, of concern for the barrel application. The present chip consumes 600 mW of power. Of this, 460 mW is consumed by the differential drivers that are used for distributing the clock, Level 1 triggers, resets and token. The remaining 140 mW is consumed by the "core" of the TBM.

IV. Quarter Micron Translation

Several design changes have been introduced in translating the design to 0.25 micron. The original differential drivers used for transmitting digital signals were current drivers. They consumed 20mW per driver. These have been replaced with lower power, low output impedance voltage drivers. The number of devices connected to clock was minimized, and, where possible, the clock is shut down to those sections of the chip when not required.

Also, in an effort to reduce clock usage, majority logic flip/flops were replaced with a SEU resistant flip/flop. These flip/flops are built using latches equipped with minimum size MIM caps, as shown in Figure 9.

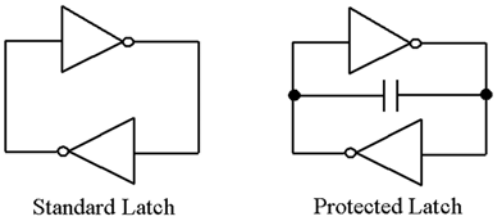


Figure 9: Standard and Protected D-Latch

Based on preliminary beam test data, the effective cross section for a standard flip/flop is 2 x 10^{-13} cm^2, while the cross section for a resistant flip/flop is 2 x 10^{-15} cm^2 [5]. Table 1 shows the expected SEU rate for a Dual TBM, using these flip/flops in all counters and configuration registers.

In the Dmill Prototype, the analog output bus was shared between the TBM and it's group of ROCs in a "wired or" arrangement. This bus now passes through the TBM. This approach offers several advantages. It reduces capacitive loading by distributing as many as 24 ROCs among four input receivers. Secondly, this will allow for a single analog line driver to communicate with the optical components located on the service cylinder, as far as one meter away.

Radius of TBM Placement (Protected F/Fs)	Expected Flux (MHz/cm^2)	Time Per SEU (Hrs/SEU)
4cm Barrel	40	12
7cm Barrel	20	24
11cm Barrel/ Foreward Blade	8	60

Table 1: Expected SEU for critical element of the Dual TBM

The Serial Protocol used to transmit commands from the front end controller to the ROCs required minor modification. The original protocol consisted of 8 data bits, D7 to D0, followed by the complement of the last data bit. This would result in no more than 9 consecutive bits of the same value. The current design of the RX40 chip used in the digital opto-hybrid [6], interprets nine or ten consecutive zeros as a reset command. To avoid this possiblity the data pattern was changed to:

D7 D6 D5 D4 $\overline{D4}$ D3 D2 D1 D0 $\overline{D0}$

This data pattern will result in no more than five consecutive data bits of the same value. In addition, a modification to the RX40 chip has been for the Pixel group. This modified version will require a greater number of consecutive bits to signal a reset.

The Dual TBM chip now has two modes of operation. The inner layers of the Pixel barrel require two TBMs, each one controlling eight readout chips. The Forward Pixel detector requires a single TBM to control as many as 24 readout chips. To that end, one half of the Dual TBM (i.e., one TBM) can be shut down, and all I/O pins associated with that TBM, can be reassigned by control command to the second TBM as shown in Figure 10.

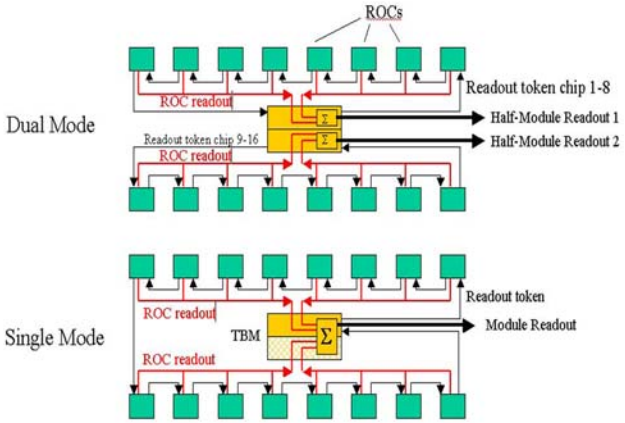


Figure 10: Dual/Single TBM Operating Modes

V. Quarter Micron Submissions

In June 2003, two versions of the Hub were submitted for production, a standard or "Fast" Hub that will be incorporated into the Dual TBM as described earlier, and a "Slow" Hub,

which must output standard I^2C [2] for communicating with the Laser Drivers [7] and a Phase Locked Loop chip [8].

The Slow Hub, as shown in figure 11, is a modified version of the "Fast" Hub. The slow clock output is created by dividing the 40MHz clock down to 156 kHz. Slow data is transmitted as an alternating one/zero pattern, with only the odd number bits latched through to the output. In other words, a pattern of:

10101010… Outputs a one.

And,

01010101… Outputs a zero.

In this way, slow data can be transmitted, while not triggering the reset mechanism of the RX40 chip.

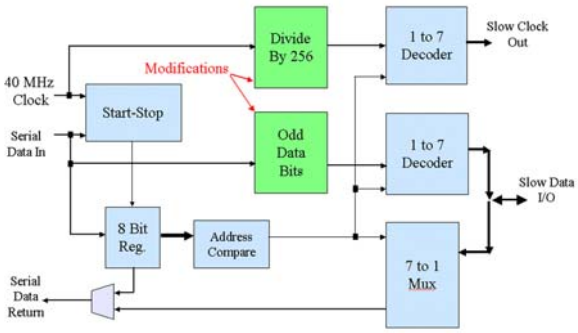


Figure 11: Block diagram of Slow Hub, showing differences from standard Hub Design

One Slow Hub chip will be connected to each Command link, and will reside on the service cylinder as will the Laser Drivers and a Phase Locked Loop chip.

As shown in figure 12, we have nearly completed the translation of the Dual TBM into quarter micron.

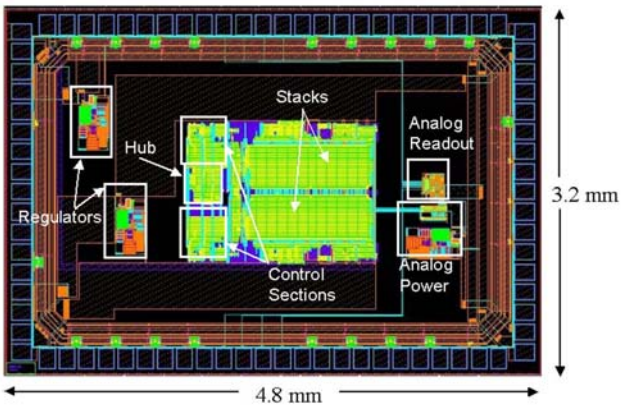


Figure 12: Nearly Completed 0.25 um Dual TBM

Even though this chip is smaller than the previous DMILL prototype, it's size is far more pad limited. There is some chance that additional pads can be removed from the design, and this possibility is being considered for a future TBM prototype, should that prove necessary.

VI. Future Plans

The quarter micron Fast and Slow Hubs will be tested in the coming weeks including testing of the ability of the Fast Hub to communicate with the quarter micron prototype of the Readout chip.

The initial prototype of the quarter micron Dual TBM will be submitted for production in October 2003. A second prototype of the Dual TBM is anticipated, with production complete by the end of 2004.

VII. References

[1] "The CMS Tracker Technical Design Report", CMS/LHCC 98-6.

[2] "I ^{2} C Bus Specification", Application Note, Philips - Signetics, January (1992).

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[6] K. Gill et al., "80Mbit/s Digital Optical Links for Control, Timing and Trigger of the CMS Tracker", Proceedings of LECC 2002, Colmar, Sept. 2002

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