

# Irradiation tests of the ALTERA SRAM based FPGA and fault tolerant design concepts

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## Abstract

In the ALICE Time Projection Chamber [1] TPC at CERN the front end electronics will be located about 3 meters from the interaction point and will therefore be exposed to radiation generated by the particle collisions. Consequently this can lead to single event upsets in sequential logic or in the configuration RAM of the FPGA. Irradiation tests have therefore been developed and carried out using the cyclotron in the physics department at the University of Oslo in Norway. The objective of the test experiment was to measure the radiation tolerance of a SRAM-based field programmable gate array (FPGA). This paper presents an overview of the irradiation tests, the latest test results and will address further investigation into hardening techniques.

## I. INTRODUCTION

The ALICE TPC is a large gas cylinder ( $88 \text{ m}^3$ ) divided in two drift regions by a central electrode located at its axial centre. A field cage creates a uniform electric field along each half of the chamber. Charged particles traversing the TPC volume ionise the gas along their path, liberating electrons that drift towards the detector end plates. The end plates consist of readout chambers divided into 18 regions on each side of the TPC, each region divided into 6 sections.

The readout electronics for the ALICE TPC detector consists of 4356 front-end cards (FECs) that contain the complete chain to readout the signals coming from 570132 pads. The front-end cards are grouped in 216 readout partitions, each controlled by a Readout Control Unit [2] fig. 1(RCU) that interfaces the FECs to the DAQ, the Trigger, and the Detector Control System. Each RCU contains the Altera APEX EP20K400E FPGA we have tested.

Due to the Field Programmable Gate Arrays (FPGA) increased complexity they are in many cases becoming more at-

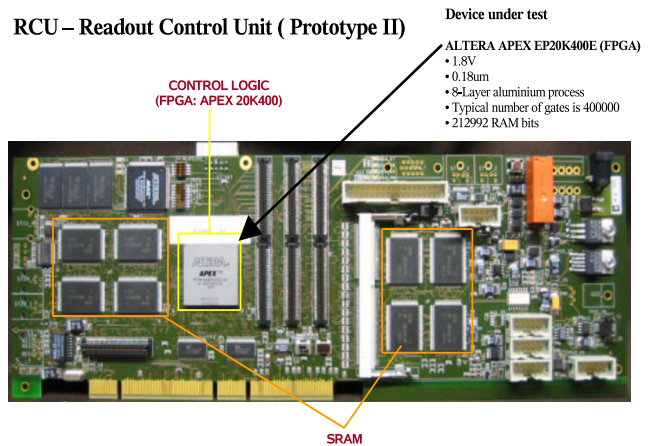


Figure 1: RCU prototype II layout. SRAM is organized in 2 banks with separate data and address lines. The control logic is contained in the on board FPGA (DUT)

tractive in use than the alternative ASICs. FPGA based on on SRAM technology makes it possible to reprogram the device and may shorten the production time of the design. However compared to the radiation tolerant ASICs, the FPGAs is sensitive to Single Event Upsets SEU. Experiencing SEUs during an ALICE experiment run may have fatal consequences. An upset in the configuration RAM can lead to a corrupt design and therefore a loss or stop in the data collection due to a re-programming of the device. It is therefore necessary to investigate the radiation tolerance of the front end electronics. While configuration RAM upsets will have to be repaired by re-configuration of the device, register bit-flip may on the other hand be corrected with different kinds of detecting/correcting coding techniques. For a low rate of upsets during an ALICE lifetime

this may show to be a sufficient solution.

## II. SINGLE EVENT UPSET, SEU

A single event upset [3] corresponds to a soft error appearing in a device due to the energy deposited in silicon by an ionizing particle. The main concern are high-energetic ( $E > 20$  MeV) particles (protons, neutrons, pions) which induce nuclear reactions in the silicon. An incoming proton will not deposit enough charge to cause a SEU through direct ionization. Most protons pass through the device with little effect, however a few incoming energetic protons can collide with a nucleus in the device material. This results in complex nuclear interactions which creates a heavy recoil ion. The heavy ion in turn ionizes the device material which through it travels, and leaves behind a track of electron-hole pairs. If this happens near to for instance a CMOS transistor, the newly created carriers will drift in the electric field in the material and will be collected at a nearby node. If the charge is sufficient to flip the state of the transistor from a binary "1" to a "0" or vice-versa, this will be a Single Event Upset. A SEU is non-destructive and a rewriting or reprogramming of the device will return the device to normal behavior thereafter. A SEU can be induced as a bit flip in a configuration memory cell or in sequential logic as a bit flip in a register. An upset is random in time and all the memory bits have the same probability of being affected.

## III. EXPERIMENTAL ARRANGEMENT

The Oslo Cyclotron [4] is situated at the University of Oslo, Department of physics. It is a Scanditronix MC-35 and can deliver an external proton beam of 29MeV, with beam intensities  $\geq 10$ pA. For our test we have used a beam spot of  $1\text{cm}^2$ . For our test we have used a beam spot of  $1\text{cm}^2$ . The beam distribution is made as uniform as possible by defocusing and using a gold foil placed upstream in the beamline.

### A. Setup and alignment

The DUT, which is mounted on the RCU prototype, is placed in the proton beam with its top surface perpendicular to the beam axis, see fig. 2. It is in turn connected to another RCU card in the PCI bus of a Linux PC (experiment PC) running software for communication and data collection from the DUT. The communication protocol between the two RCU cards is the Slow Control Serial Network [5](SCSN). The SCSN consists of a VHDL block design on the FPGA placed on both RCU cards. This means that there is a possibility of experiencing single event upsets in the SCSN design as well. In future version the communication handling will be moved out of the DUT. For now, a periodic loop back of the output of the SCSN is done to check for upsets related to the communication. Another Linux PC is placed in the control room and is used for

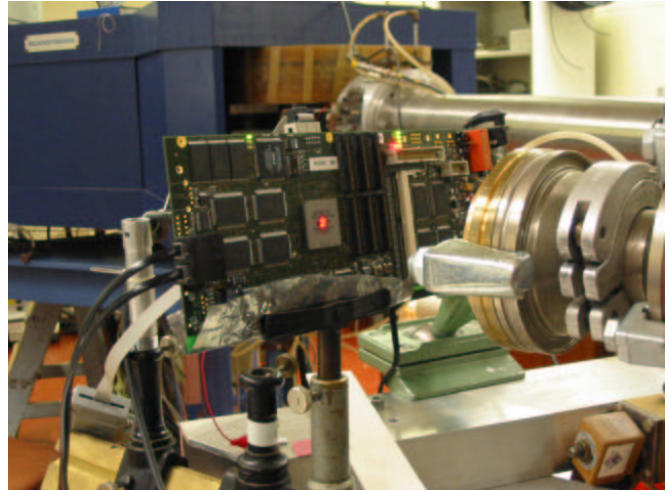


Figure 2: RCU prototype card mounted in the beam path. A laser is used to align the FPGA correctly

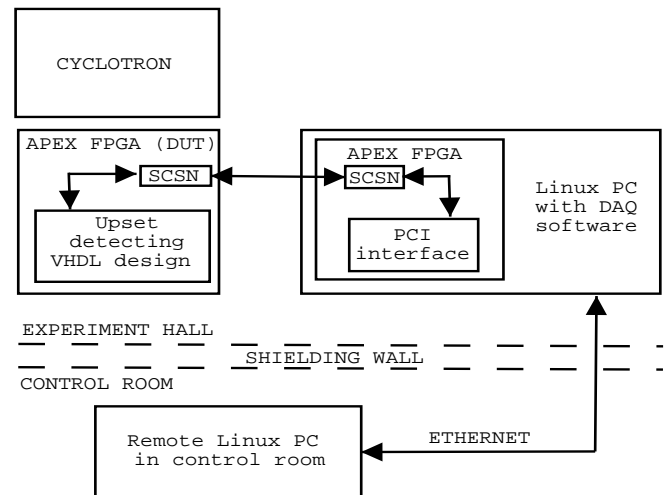


Figure 3: schematic showing an overview of the basic architecture of the test setup

remote control of the irradiation test. Both PCs are connected to Internet and the test can in principle be run from anywhere. In fig. 3 a schematic overview of the setup is shown.

The alignment of the DUT is done by using a laser mirrored in parallel to the beam path.

A camera is placed in the experiment hall and with the help of a monitor in the control room a ceramic viewer with a marking spot is aligned in the beam. A proton beam in the order 10 times the test intensities illuminates the viewer. The marking spot on the viewer is used as a reference for the laser so that the DUT can be securely mounted in the beam path when the beam is off.

## IV. SEU MEASUREMENT

### A. DUT

The device tested was the ALTERA APEX EP20K400E FPGA [6] [7]. This device is fabricated in a 1.8V, 0.18 $\mu$ m, 8-Layer aluminum process. The APEX 20KE device is constructed from a series of MegaLAB structures. Each MegaLAB structure contains 16 logic array blocks (LABs), one Embedded System Block (ESB), and a MegaLab interconnect, which routes signals within the MegaLAB structure. Each LAB consists of 10 logic elements (LEs). The ALTERA APEX EP20K400E FPGA contains 16640 logic elements and 212992 internal RAM bits, and the typical number of gates is 400000. Each logic element has a programmable register, a four-input Look Up Table (LUT) and carry and cascade chains. The RAM bits are divide throughout the device in Embedded System Blocks (ESB). The ESB can implement various types of memory blocks including dual-port RAM, ROM and FIFO. It is housed in a 672-Pin FineLine BGA Package.

### B. Upset detection

The ALTERA FPGA tested does not offer the option to read out the content of the configuration RAM. Therefore the configuration upsets have to be detected indirectly using a design implemented in VHDL code. This means that a bit flip or an error observed will reflect the change in logic due to an upset in a configuration bit, and not the configuration bit flip itself. A 100% use of configuration memory bits is very unlikely, thus configuration upsets that will not influence the behavior and therefore not be detectable, can occur. Thus the result will not give an exact number of configuration bit flips, but only an estimate. It is also hard to say if a detectable change in logic is due to a single or a double bit flip in the configuration RAM. A change in the logic caused by a configuration upset or a single bit flip induced directly in the logic will at first glance have the same appearance. It will only be distinguishable by looking at it over time. While a configuration upset will give a permanent change in the logic, until reprogramming of the device, and therefore be reflected as a stuck at error in the read out, a single bit flip will only be present until the next clock cycle loads a new value into the register. Taken in account the above discussed behavior of upsets, a VHDL design to detect both single bit flips in sequential logic and configuration upsets was designed. Since the ALTERA APEX FPGA contains both logic elements and internal RAM, the design should concern both. The design implemented is a 32 bit wide and 400 bit long shift register in the logic elements, see principle schematic in fig. 4, and a 32 bit wide and 4096 bit deep FIFO in the internal RAM blocks. The shift register uses approximately 90% of the logic elements while the number for the internal RAM bits is 60%

A walking one and zero pattern was shifted through both the shift register and the FIFO. The read out pattern from the design is compared with the expected value and if it differs a

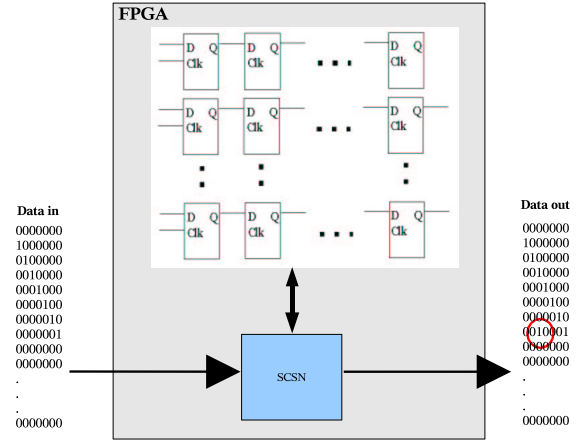


Figure 4: The shift register is implemented in the logic elements of the FPGA. A fixed pattern is shifted through the register and is compared for expected value at the output. The shift register is 32 bit wide and 400 bit long

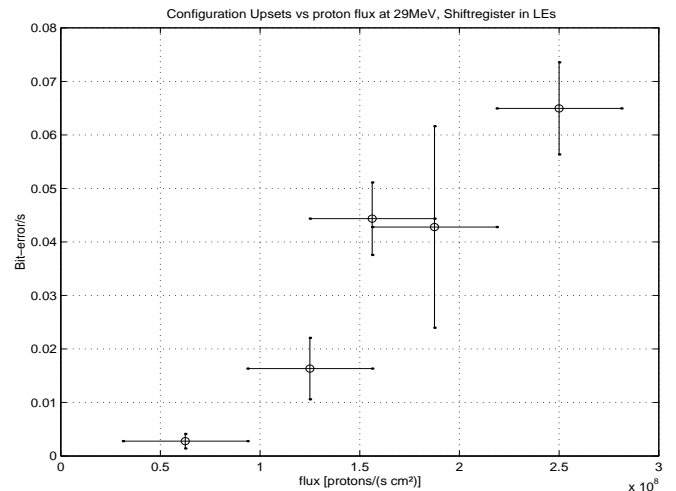


Figure 5: The rate of configuration upsets in logic elements plotted versus the flux

single event upset has occurred.

## V. RESULTS

Irradiation of the FPGA was done with a 29MeV proton beam with fluxes ranging from  $0.63 \cdot 10^8 - 2.5 \cdot 10^8 p/cm^2 \cdot s$ . Several runs were done and the results are plotted in figures fig. 5, fig. 6, fig. 7. The cross-section for the configuration upsets in the logic elements is plotted in fig. 8. The plots for the upsets in the internal RAM is corrected by a factor of 1.7 due to the use of RAM bits is 60%.

Assuming the upsets are random in time and uncorrelated we would expect a linear dependency in the upsets plots and

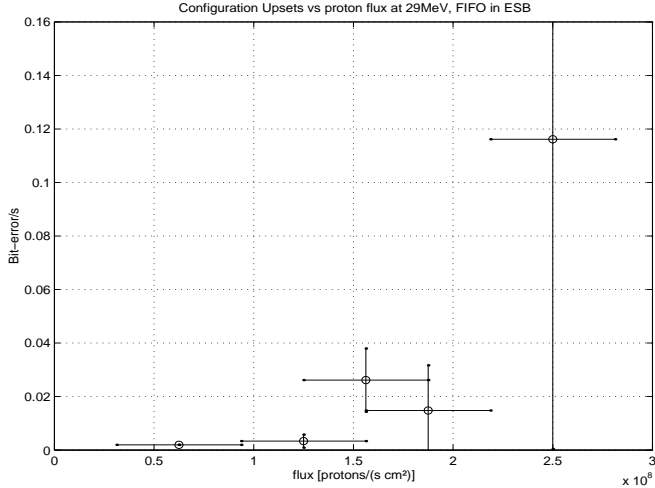


Figure 6: The rate of configuration upsets in internal RAM plotted versus the flux

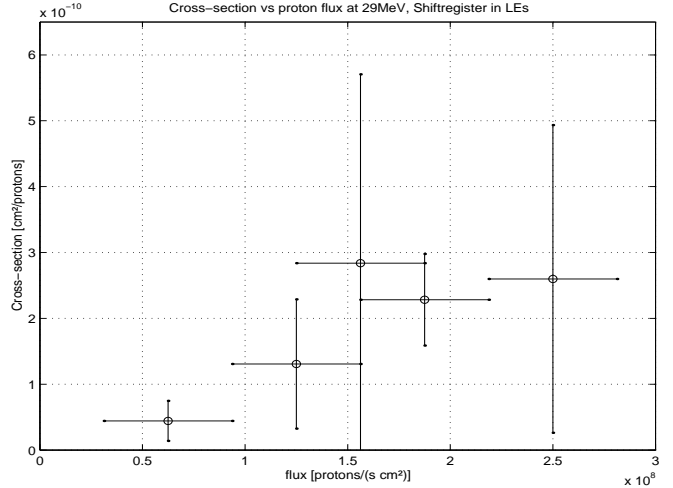


Figure 8: A plot of the cross-section versus the flux for configuration upsets in the logic elements Cross-section  $1.9 \times 10^{-10} \pm 0.8 \times 10^{-10} \text{ cm}^2$

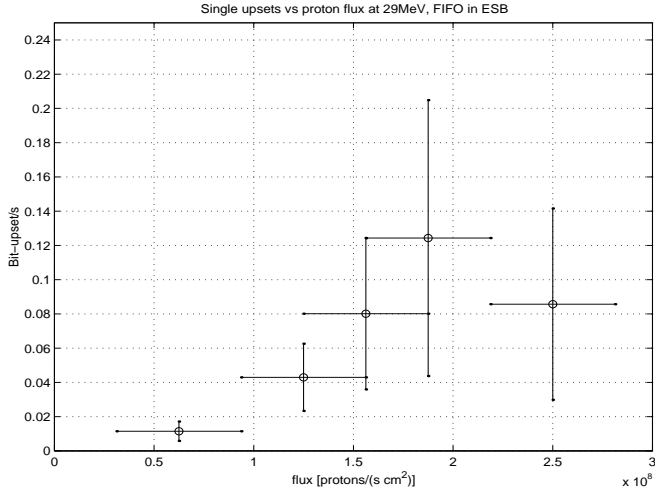


Figure 7: The rate of single upsets in internal RAM plotted versus the flux

a constant value in the cross-section plots. For the configuration upsets in the logic elements we can see the resemblance of a linear plot. However the error bars are considerable due to uncertainties in the measurements.

For these test single bit flips are discovered in the internal RAM only, and the corresponding cross-section is higher than for the configuration upsets in the logic elements. The reason for this might be that the density of SRAM cells in the ESB blocks are much higher than in the logic elements. And therefore the probability of hitting a SRAM cell in the internal RAM is considerably higher.

In the logic elements the SRAM cells will configure the behavior and interconnection of the logic, and this is only done once. For the internal RAM the SRAM cells will be updated every time they are written to. Since the Embedded System

Table 1: Cross-section for configuration upsets

Type	Cross-section [ $\text{cm}^2$ ]
Logic	$1.9 \times 10^{-10} \pm 0.8 \times 10^{-10}$
Internal RAM	$1.5 \times 10^{-10} \pm 0.8 \times 10^{-10}$

Table 2: Cross-section for single upsets

Type	Cross-section [ $\text{cm}^2$ ]
Logic	$< 5.3 \times 10^{-12}$
Internal RAM	$4.1 \times 10^{-10} \pm 2.2 \times 10^{-10}$

Blocks also contain some logic like input registers this might be the reason that we also see configuration upsets in the internal RAM.

## VI. HARDENING INVESTIGATION

As the device sizes decrease the circuits become more sensitive to soft errors as for instance single event upsets. Fault-tolerant techniques have therefore emerged as an important design consideration for FPGA-based systems. The FPGA has become more complex over the last few years and can today implement a whole system on one chip. While a SEU in a RAM or FIFO will only give a loss in some data points, a configuration upset in the logic of the device may cause the functional behavior of the design to change. So different fault-tolerant techniques has to be considered for the control functions and the data storage circuits. A single flip in a storage device can be detected and corrected by using a for instance hamming coding. In logic elements different error detecting techniques can also be used to detect and if possible correct an error. However if the configuration of the logic is affected a solution will be to use redundancy in the circuit. If a part of the design fails an identical part placed elsewhere in the circuit continues the task until this

fails as well. Implementing two or three identical versions of a critical part of the logic may lengthen the lifetime of the device before reprogramming is needed. Introducing this kind of redundancy will of course influence the space requirements. So a priority has to be made with regards to which part of the circuit to protect. If it turns out that fault-tolerant concepts in the VHDL design will not be able to cope with the radiation experienced, one might have to face the reality of changing to radiation tolerant devices such as Flash based ones. Radiation tests of such a device, a ProASIC<sup>P</sup>LUS from ACTEL, is underway.

## VII. CONCLUSIONS

It is hard to draw any final conclusions from the tests so far. For sure single event upsets will have to be considered for the FPGA designs, but there are still a few open questions with regards to the expected radiation levels. At the moment we are planning the next test where the methods and designs will be improved to cope with some of the uncertainties experienced, and to support the preliminary results and to collect more statistics. One important change will be to replace the SCSN communication and have the inputs and outputs of the shift register and FIFO connected directly to input and output pins. Tests will also include Flash based FPGAs. Some more detailed simulations and calculations of the expected radiation levels in the ALICE TPC detector will have to be carried out before one can decide if the rate of upsets during an ALICE run is below a acceptable level.

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