# A CMOS low power, quad channel, 12 bit, 40MS/s pipelined ADC for applications in particle physics calorimetry.

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## *Abstract*

The AD41240 is a 12-bit, four-channel pipelined analog to digital converter fabricated in a rad-tolerant CMOS technology and capable of running at 40 MHz with a power consumption per channel of 150 mW at 2.5V. The converter core uses a 10 stages pipeline with multiple resolution and converts in 5 clock cycles. The component also contains digital logic that allows to effectively extend the dynamic range of the input signal. For instance, when combined with suitable front end amplifiers with gains of 1x, 2x, 4x and 8x, a 15 bit range with a 12 bit precision can be obtained. Digital logic performs the selection of the channel in the correct input range. A special digitally controlled hystereris mode is also available to facilitate measurements of pulse extending over different ranges of amplitude.

The complete chip occupies an area of about 4x4 $mm^2$ and is implemented in a 3-metals commercial ¼ micron technology using radiation tolerant layout rules.

## I. MOTIVATION

Like other electromagnetic calorimeters, the one installed in the CMS experiment requires read-out electronics with a demanding combination of wide dynamic range, good resolution and high speed. The key component in such an electronic chain is the data converter. The LHC environment adds also two new difficult constraints to the choice of a suitable component: first the extreme radiation conditions which render unusable many potential commercial components and second the low power which should be dissipated by the part. While a 40 MHz sampling is required to allow the fitting of the entire pulse as shaped in the preamplification stage, the input signal has a bandwidth of about 5 MHz.

## II. SYSTEM ARCHITECTURE

The architecture of the proposed read-out system is shown in Figure 1. It is essentially based on the fact that a sufficiently low power 12-bit ADC macro cell can be designed in an advanced CMOS technology. Unlike other architectures based on gain switching of a special amplification stage [1], the proposed architecture uses four fixed gain amplifiers followed by a bank of converters. This approach leads clearly to a simpler system, as the range choice is performed digitally.

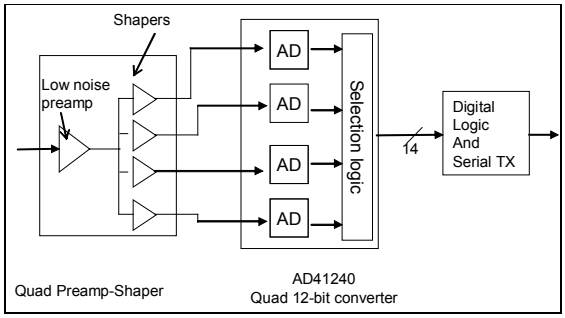



Figure 1: System architecture

The front-end chip used in this application is called MGPA and is described elsewhere at this conference.

The digital selection block allows also more sophisticated channel selections than an analog gain switching would allow. For instance, a hystereris mode is available to keep digitising a given pulse on the scale selected for its peak even when the signal decreases. This feature eliminates discontinuities between different channels, because the measurement of the tail of a given pulse signal can be performed on the range where the peak has been measured.

## III. AD41240 CORE

### *A. Architecture*

The Quad ADC is implemented in fact as two dual 12-bit 40MS/s ADCs, leading to the best arrangement for sharing common parts between the channels. The architecture of the dual data converter channel is illustrated in Figure 2. The input signal is directly sampled and quantized in a 2.5-bit front-end stage, and the corresponding residue is propagated along a 10-bit conventional 1.5-bit/stage pipeline ADC. The reduced signal bandwidth, together with an appropriate design of the sampling networks on the front-end stage, lead to the elimination of the traditional front-end sample-and-hold amplifier (S/H). This results in improvements in the achievable SNR, as well as in savings on power and area.

The specific arrangement of the resolution-per-stage shown in the block diagram of Figure 2 is the result of a careful architecture-level study in search for the best trade-off between performance, modularity and complexity of implementation. In fact, it is well know [2,3,4] that a large resolution in the front-end stage is beneficial in terms of static

linearity, distortion and level of generated spurs, but it is paid in the complexity of the amplifiers needed for the residue amplification. Conversely, lower resolution in the front-end stage affects achievable performance but leads to simpler and more modular implementations. The selected architecture is a good balance between the alternatives mentioned above.

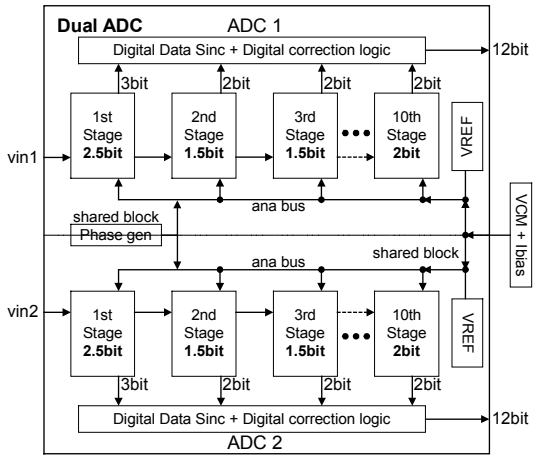
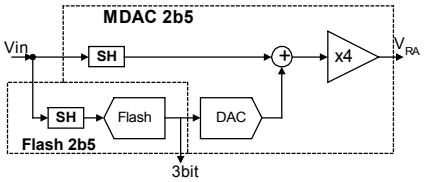


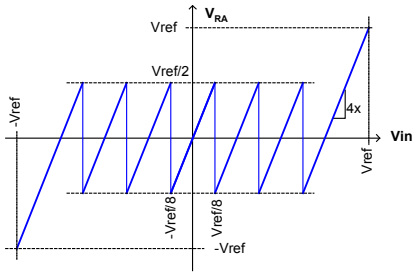

Figure 2: Architecture of a dual 12-bit data converter

## B. *Front-end stage design*

The front-end stage simplified block diagram is presented in Figure 3 (a). It is composed of a 2.5-bit MDAC and a 2.5-bit Flash quantizer implementing the residue transfer characteristic illustrated in Fig. 3 (b). Due to the absence of an input S/H, the sampling paths in both the MDAC and the Flash quantizer were carefully optimised to have matched time constants so as to minimize phase shift errors in the sampled signals. The residual errors due to this double-path sampling operation are recovered by the redundancy and digital error correction, which are normally introduced in the architecture to relax the characteristics of the comparators in the quantizer.




(a)




(b)

Figure 3: (a) Circuit configuration of the 2.5-bit Front-end stage, and (b) corresponding residue transfer characteristic

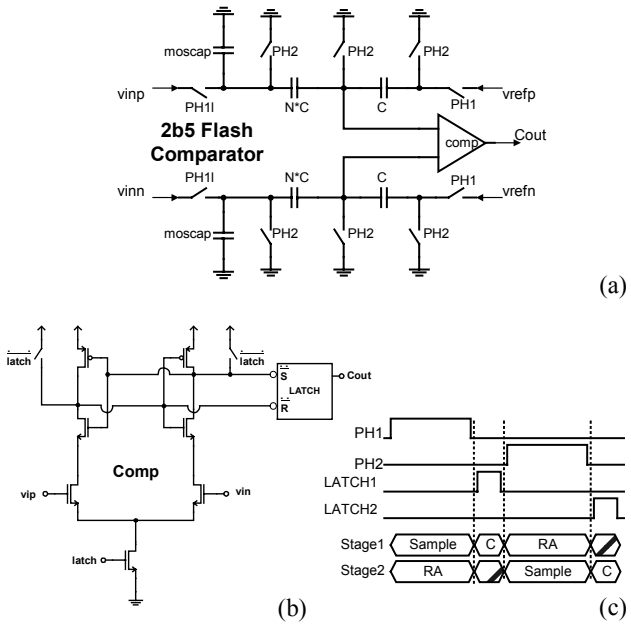



Figure 4: Comparator used in the Front-end stage

The 2.5-bit fully-differential Flash quantizer uses 6 comparators of the type presented in Figure 4 (a) to define the 6 transition voltages present in the residue transfer characteristic of Figure 3 (b). In its most common form, the quantizer uses a taped R-string connected between the reference voltages, Vrefp and Vrefn, to define these transition voltages. Since this leads to higher static power consumption from the references, this implementation uses the input coupling capacitive network in front of each comparator to create the appropriate thresholds. The latched comparator is illustrated in more detail in Figure 4 (b). It is basically an improved version of a dynamic regenerative latch, which greatly reduces kick-back noise.

The fully-differential 2.5-bit MDAC illustrated in single-ended mode in Figure 5 is implemented with an operational amplifier surrounded by two capacitor arrays. During phase 1, the input voltages Vinp and Vinn are sampled on the capacitor arrays, while being compared in parallel to the various transition voltages at the Flash quantizer. During phase 2, the capacitor array is configured in the residue amplifier configuration taking into account the 3-bit information resulting from the quantization of the sampled input voltage performed in phase 1. The topology of the operational amplifier used in the MDAC is presented in Figure 5 (b). It consists of a Gm-multiplier mirrored topology with cascode output branches. The DC gain of this topology was increased by using NMOS regulated cascodes so as to compensate higher output conductance in these devices when compared to those exhibited by the PMOS devices. Native devices with low Vt where introduced in M19-M20 not to adversely affect the output swing. When inserted in the MDAC with all the switches and capacitors around it, this amplifier exhibits a DC gain of 90 dB and a gain-bandwidth product of 260 MHz, while consuming 3.9 mA.

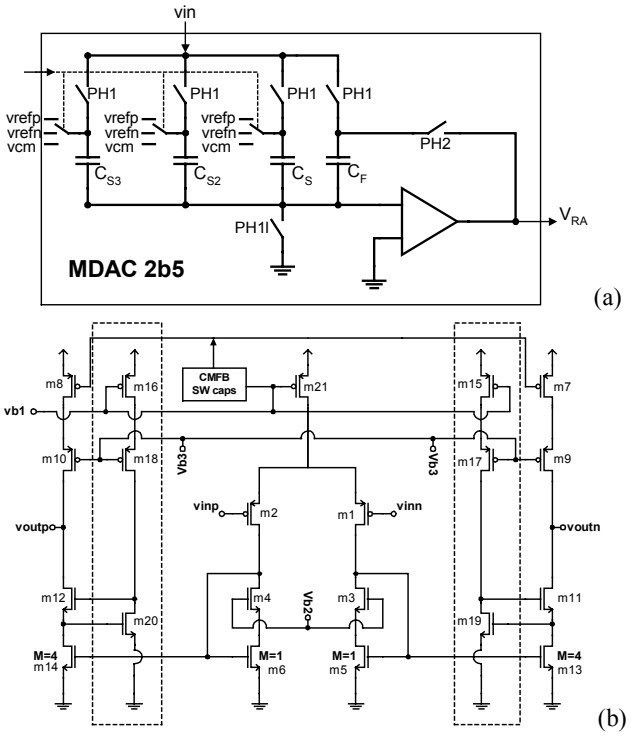



Figure 5: (a) 2.5-bit MDAC configuration used in the Front-end stage, and (b) operational amplifier topology

### C. Backend ADC

The remaining 10-bit, 40MS/s pipeline ADC is implemented in a conventional 1.5-bit/stage arrangement as originally proposed in [5]. The amplifiers in the MDACs have a similar topology as in the front-end stage, but the regulated cascodes were removed and the power dissipation was reduced along the pipeline due to the increasingly relaxed accuracy and noise requirements from the front to the back of the pipeline ADC. The comparators use a purely dynamic regenerative topology as proposed in [6].

### D. Digital range selection

A range selection logic block is located after the last correction stage of the ADC and performs the choice of the range. For this a digital comparator per channel decides if the output of the ADC is close to the top of the corresponding range, and in this case it informs an output multiplexer to select the next non-saturated channel. This selection occurs with a very small delay and does not add any significant latency to the conversion as seen at the output of the chip.

### E. Output bus

To minimize the digital noise created on the board the chip uses LVDS signalling for the input clock line and for the data output bus. The doubling of the signal lines is compensated for by being able to run the output bus in a number of modes summarized in Table 1. At 80 MWords/sec, the output clock still runs at 40 MHz, but data are made available on both edges of the clock.

Table 1: Valid output bus configurations

| Mode | Bus speed [MW/sec] | Number of buses / Bus width |
|---|---|---|
| 0 – Quad ADC | 80 DDR | 2 / 12 |
| 1 – Ecal Direct | 40 | 1 / 14 |
| 2 – Ecal with Hysteresis | 40 | 1 / 14 |
| 3 – Ecal Direct | 80 DDR | 1 / 7 |
| 4 – Ecal with Hysteresis | 80 DDR | 1 / 7 |
| 5 – Transparent (Channels 0-1) | 40 | 2 / 12 |
| 6 – Transparent (Channels 2-3) | 40 | 2 / 12 |

### F. Chip configuration

The mode of operation is configured by setting some CMOS input pins to the appropriate levels. In addition, a power-down mode per channel is available. This allows saving power for the unused channels in applications where not all four channels are used or in applications with a low data rate, where data conversion can be operated in burst mode.

## IV. Implementation and Results

### A. Chip Implementation

The Quad 12-bit 40MS/s ADC was integrated in a rad-tolerant 0.25µm CMOS 1P3M technology. The chip, illustrated by the microphotograph in Figure 6, includes 4 conversion channels, the digital selection logic and LVDS interfaces, as well as a common-mode voltage and bias-current generation block shared by the ADCs. The area per dual ADC pair is less than 4 $mm^2$, and the total die area is 11.8 $mm^2$. Some of the most relevant blocks in the chip were highlighted for a better understanding of the floorplan arrangement. The chip was mounted in a 144-pin fpBGA package, owing it to the excellent performance exhibited by this carrier with respect to the parasitics associated to pins.

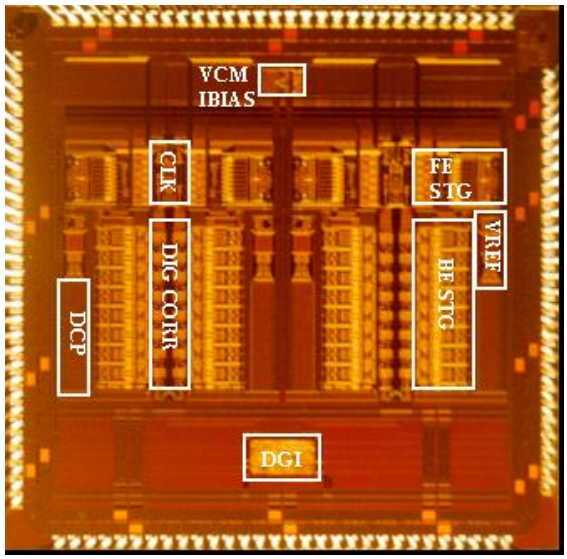



Figure 6: Microphotograph of the Quad ADC chip

### B. *Experimental results*

During the initial tests a performance degradation was detected when the ADCs used the internal reference buffers. These buffers are now subject of a design revision and were externally bypassed in the tests. A number of conventional characterization procedures for ADCs were run over the four channels. The results presented below are obtained with code density tests and FFT spectral analyses when the converters are driven with near full-scale sinusoidal waveforms. Figure 7 shows typical DNL and INL characteristic obtained at 40 MS/s for an input frequency of 2.5 MHz. DNL and INL are within ±0.7 LSB and ±1.5 LSB, respectively. Figure 8 shows a typical FFT spectral analysis obtained in the same conditions as above. SNR and THD are approximately 67 dB and –72 dB, respectively, leading to around 10.8 effective bits. The total power of the Quad ADC excluding the digital logic and I/Os is 412mW, leading to 1.44 pJ/conversion.

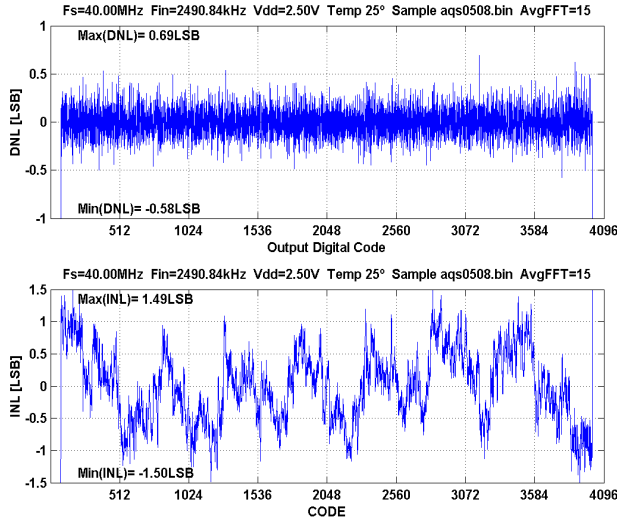



Figure 7: Typical DNL and INL characteristics of one ADC channel

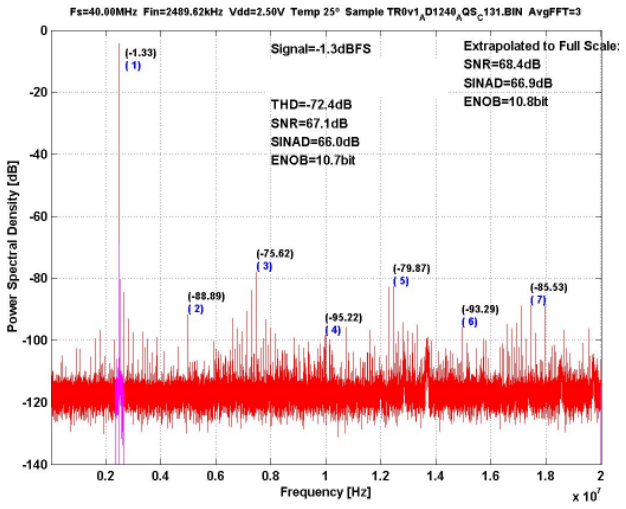



Figure 8: Typical dynamic performance of one ADC channel

## V. SUMMARY

This paper presented a quad 12-bit, 40MS/s ADC system that is sufficiently compact and low power to enable a new approach not considered before for the readout of high dynamic range signals in particle physics calorimetery applications. As it stands now, the system composed of the bank of pre-amplifiers followed by the quad data conversion system shows performance levels never reported before in this type of applications.

The detailed explanation of architecture and circuit topologies was consolidated by experimental results from the testchip integrated in a 0.25µm CMOS commercial technology that is made rad-tolerant by the use of appropriate layout techniques.

## ACKNOWLEDGEMENTS

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## VI. REFERENCES

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