Radiation Effects in FPGAs

J. J. Wang

Actel Corporation, Mountain View, CA 94043, USA
jih-jong.wang@actel.com

Abstract

Total ionizing dose (TID) effects and single event effects (SEE) in antifuse-, Flash-, and SRAM-based field programmable gate arrays (FPGAs) are reviewed. There is a brief discussion of the programmable element impact on the FPGA architecture. In the following sections, most radiation data are from antifuse-based FPGAs. The basic TID mechanisms are introduced and used to explain the anomalies in the FPGAs. Power supply current (I_{CC}) and propagation delay (t_P) are parameters used most often to study the TID effects. SEE is focused on the single event upset (SEU) and its various manifestations on devices. The discussion starts with basic SEU mechanisms in a latch and in a buffer. Clock upset and control logic upset are defined and studied with examples. The consequent hardening for each TID or SEE case is also discussed after the elucidation of the anomalies.

I. INTRODUCTION

FPGA is the densest and most advanced programmable logic device. It enables a designer to implement large digital designs in a device at any time at any location. In general, it has the advantages of high density, high performance, fast turnaround and low cost per design implementation. Since these are the traits ideal for space flight missions, the space community has actively evaluated radiation effects for every new FPGA coming out of the production line. In 1992, a Jet Propulsion Lab (Pasadena, California, USA) lead team published a report recommending the use of several antifuse-based FPGAs for space applications [1]. This report is probably the first published document on radiation effects in FPGAs. The antifuse-based FPGA started to be accepted by the aerospace designers at that time. In later years, the SRAM-based FPGA saw some applications after its single event latch-up (SEL) was solved. In the last few years, the Flash-based FPGA joined the action after its introduction and the subsequent elimination of its SEL susceptibility. Until now, because of its insensitivity, antifuse is still the dominant technology for applying FPGA in very harsh radiation environments.

Fundamentally, the radiation effects of FPGAs are not different from those of any other CMOS-based digital integrated circuits. The basic mechanisms of radiation effects in CMOS devices are well studied and documented. For example, the annual IEEE Nuclear and Space Radiation Effects Conference (NSREC) is one of the best sources for radiation effects in electronics. The main logic reasoning or detective work is usually to correlate the radiation-induced "anomalies" in a device with these basic mechanisms. Each FPGA has its unique architecture, and each has its unique anomalies.

This paper starts with a brief discussion of the relationship between the programmable elements, or switches, with the architecture, performance, and radiation tolerance. This part is a synopsis of a previous presentation by an Actel colleague [2]. TID effects and single event effect (SEE) will then be presented in separate sections. Major portion of the data will be on Antifuse-based FPGAs. Flash-based FPGA has not been studied much because it is only few years old. The SRAM-based FPGAs is difficult to study because radiation can alter its configuration. The scope of the presentation covers the parameter changes due to irradiation, error rates in storage elements, and functionality. Relevant basic mechanisms are presented and used to explain the device behaviors influenced by radiation. In some cases, radiation hardening by design is applied once the device behavior is understood.

II. IMPACT OF PROGRAMMABLE ELEMENTS ON FPGA DEVICES

An FPGA device consists of electrically programmable interconnections and logic modules. The programmability is accomplished by turning on/off a switch controlling the connection of two wires. There are three distinctively different switch technologies, SRAM, Flash, and antifuse. The area and performance of the switch essentially determines the architecture of the particular kind of FPGA.

The wires in SRAM-based FPGA are very expensive because the switch is large and slow. The logic module has to be as large as possible to minimize the number of wires. Typically, each logic module is equivalent to about 20 logic gates. Also for the sake of saving wires, the logic module is designed symmetrically so that all inputs are the same. The choice is the 4 x 4-RAM array, also known as the 4-input LUT (look up table).

The wires in Flash-based FPGA are significantly cheaper because the switch is smaller. A Flash switch cell is about one-seventh the area of an SRAM cell. Consequently, the logic module can be very fine and asymmetrical. In the only commercially available Flash-based FPGAs, the ProASIC and ProASIC-Plus, the choice is a flip-flop. It can also be configured to a 3-input combinational logic.

Antifuse-based FPGA has the cheapest wires. Its switch is one-tenth the area of an SRAM switch. The logic module is small, about 3.5 equivalent logic gates, and asymmetrical. Multiplex-based logic is the choice of the logic module in general purposed antifuse FPGAs. Additional flip-flops are

also included to facilitate the sequential logic circuits in the designs.

The place-and-route of FPGA has to be automatic for a large design whose input is usually in a format of high-level hardware description language, such as VHDL or Verilog. Vendors of FPGA all offer software for the automation. In this software development, the hardest and most creative part is place-and-route. Apparently more switches and wires will ease the creation of automatic place-and-route. Thus, SRAM-based FPGA is the most difficult in software development. Flash and antifuse-based FPGAs are much easier. Also, because the place-and-route of Flash and antifuse-based FPGAs is similar to that of the alternative hardwired ASIC design, many ASIC techniques can be implemented with small modifications.

As for the physical programming of a switch, SRAM is obviously the easiest. A key advantage is the use of the operational V_{CC}. Programming a Flash switch needs high voltage, approximately 17 V. Antifuse switch is programmed at a high voltage scaled with the operational V_{CC}, about three to four times of the V_{CC}. Pass transistors are needed in the programming-network to control the voltage distribution so that only the desired antifuse is programmed.

Technologically, SRAM-based FPGA is usually one generation ahead because a standard CMOS process manufactures it. The usage of the most advanced technology compensates the cost of wires somewhat. However, the scaling in recent years is slowing down that may eventually homogenize the manufacturing technology for the logic in all three kinds of FPGAs.

The differences of radiation sensitivities in different technology based FPGAs also originate in the switches. For TID, the antifuse switch is completely immune. The sensitivity of the device is determined by the CMOS logic part. The SRAM switch is CMOS logic. Compared to an antifuse-based counterpart, its sensitivity is increased because the added effects on the switches. Also, the hardening by design in SRAM-based is very expensive area-wise because most, if not all, the switches have to be hardened. The TID sensitivity of a Flash-based FPGA will likely determined by the floating gate switches [3]. However, the study of this subject has just begun because the device is only few years old.

The non-volatile antifuse and Flash switches are insensitive to SEE. The logic modules thus determine the sensitivity of the device. SRAM-based FPGA has the biggest disadvantage in that its switch is very sensitive to the single event upset (SEU). For example, even in real time operation, cosmic-neutron induced soft errors in the SRAM switches can be detected at a typical ground location anywhere. Table 1 shows the errors and cross-section per bit of 0.15 μm SRAM switches at sea level, 5,200 ft and 12,250 ft [4].

Hardwired SEU hardenings of non-volatile switch based FPGAs are economically viable because only the logic modules need to be hardened. SRAM-based is difficult to be SEU hardened by hardware solutions. So far, there is no solution without very expensive area penalties. Some software mitigation techniques were proposed and used. However, due to the complexity of the SEU effects on the SRAM-based FPGA, its understanding and subsequent hardening are still open for research at this moment. Table 2 summarizes important characteristic comparisons described in this section.

Table 1 Neutron induced SEU in SRAM switches

V_{CC}	Altitude	No of switches	Hours	Errors	Cross section (cm^2)
1.5	Sea level	1958546400	3246	4	3.15E-14
1.5	5200	1958546400	8645	18	3.18E-14
1.5	12250	1958546400	2084	24	3.20E-14

Table 2 Comparison of different technology based FPGAs

Switch	SRAM	Flash (EEPROM)	Antifuse
Switch Control	Volatile memory	Non-volatile floating gate NMOS	Non-volatile metallic link
Re-configuration	Fast	Slow	Not available
	Operation V_{CC}	High voltage (20V)	
	Unlimited times	Limited times (~1000)	
	Re-configurable data processing	Off-line	
SEU	Switch very sensitive to SEU	Switch not sensitive to SEU	Switch immune to SEU
TID	Switch has CMOS TID	Switch has typical Flash TID	Switch immune to TID

III. Total Ionizing Dose Effects

A. Basic TID Mechanisms

The radiation-induced charge trapping in the oxide layers over the silicon produces the TID effect in advanced CMOS circuits. Figure 1 [5] shows the charge generation, transport and trapping in a biased oxide layer. In sub-micron devices, the hole trapping near the Si/SiO_2 interface is the primary effect.

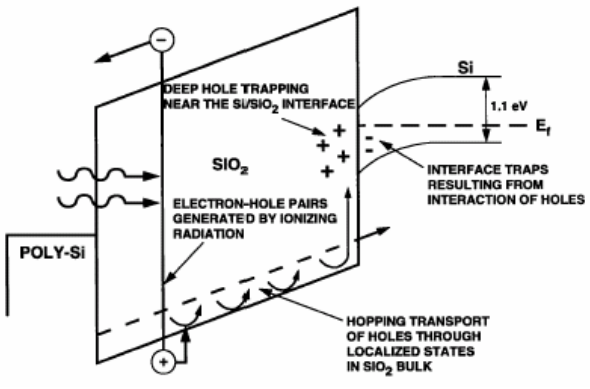

Figure 1: The charge generation, transport and trapping in a biased oxide layer. The primary effect in sub-micron device is the hole trapping near the Si/SiO_2 interface [5].

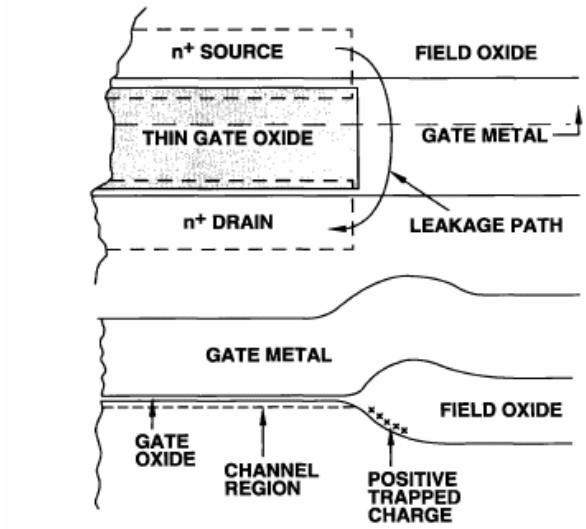

Figure 2: Schematic layout showing the edge leakage path in NMOSFET [6].

The hole trapping near the Si/SiO_2 interface can induce the charge inversion in the silicon at the interface and consequently create parasitic leakage paths. There are two kinds of leakage paths. Figure 2 [6] illustrates the edge-leakage path between the drain and source at the edge of a NMOSFET. The other kind, called field-leakage path is between any two n+-junctions separated by a field oxide. The edge leakage is usually more serious than the field leakage because the shorter path length. In typical pre and post-irradiation I_{DS}-V_{GS} curves of a NMOSFET (Figure 3), two radiation-induced components can be identified, the I_{DS} shift due to the holes trapping and creation of interface traps in the gate oxide area, and the shift due to field and edge leakage. These data were measured on old technology using thick gate oxide. In sub-micron devices studied in this paper, the I_{DS} shift due to the gate oxide is negligible because the oxide thickness is too thin to trap net charges and the interface quality is too good to be activated by radiations. For a PMOSFET, the leakages are reduced because the silicon surface is induced to favor the accumulation.

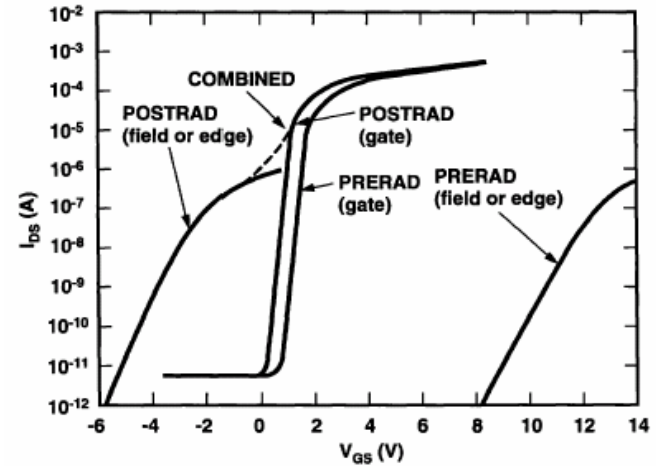

Figure 3: I_{DS} versus V_{GS} of a NMOSFET showing each component of radiation induced leakages [6].

B. TID Effects in Antifuse-based FPGA

For the purpose of screening, the measurement of TID effects of antifuse-based FPGAs usually follows the military testing standard TM1019 [7]. Figure 4 shows a simplified testing flow. A logic design composed of many sub-circuits is programmed into the device under test (DUT). As shown in Table 3, the AC/DC electrical parameters are measured at the inputs or outputs of these sub-circuits. Among them the I_{CC}, propagation delay, and power-up transient current are most affected parameters. One of them often was the first gone out of spec and determined the tolerance of the DUT. The measured radiation effect also depends on the bias and dose rate. Unless otherwise specified, the data presented in the rest of this section is irradiated at static bias of V_{CC} with a dose rate of approximately 1 krad(Si)/day. The radiation is gamma ray generated by a Co-60 source.

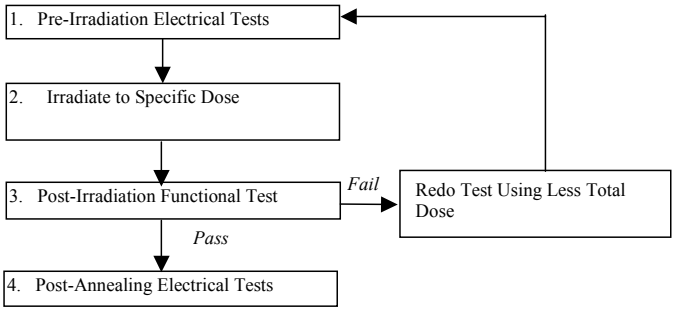

Figure 4: Flow chart showing a simplified TM1019 used for TID testing antifuse-based FPGAs.

Table 3 The parameters for TID testing antifuse-based FPGAs

Parameter	Logic Design
1. Functionality	All key architectural functions
2. I_{CC}	DUT power supply
3. Input Threshold (V_T)	Input buffer
4. Output Drives (V_{OH}/V_{OL})	Output buffer
5. Propagation Delays	String of inverters
6. Transition Time	D flip-flop output
7. Power-up Transient	DUT power supply

I_{CC} is the most important parameter for monitoring TID effects. Both the radiation-induced edge and field leakage directly reflect on it as an increasing background. This component of I_{CC} is not linear with respect to the dose. The leakage paths are turned on by trapped charges proportional to the total dose in a similar fashion as a MOSFET. As I_{CC} increases, the power dissipation will increase and heat up the device. The higher temperature will lead to higher I_{CC}. The temperature will be balanced by heat exchange with the ambient. This temperature component usually kicks in when I_{CC} exceeds 100 mA. As long as I_{CC} is not too high, these two components distribute uniformly across the chip area and cause no functional failures or permanent damages. If a critical circuit in the device fails at certain total dose level, I_{CC} can suddenly jump at this level, and functional failure is usually accompanied with it.

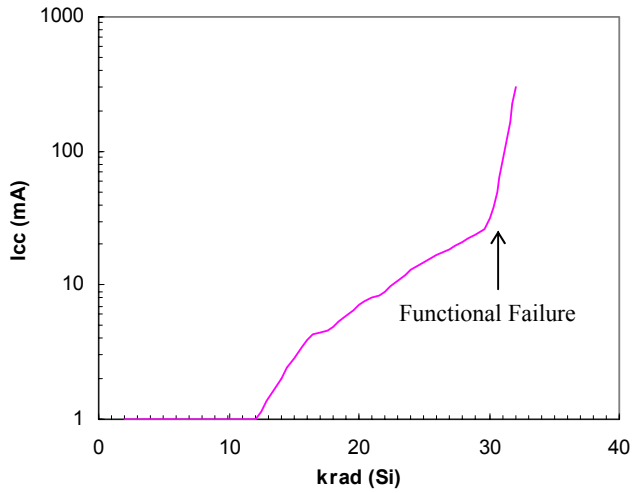

Figure 5: In-flux I_{CC} of a 0.8 µm A1460A antifuse-based FPGAs. A sudden increase of I_{CC} was observed with functional failure.

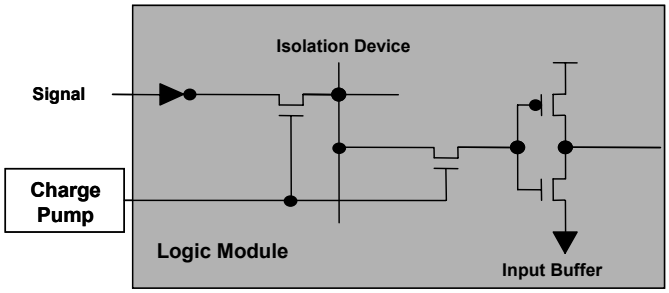

Figure 6: Schematic showing the isolation devices for isolation high voltage from logic module during programming.

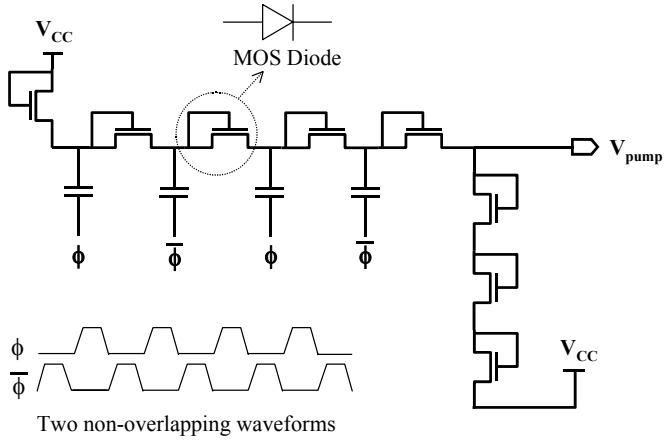

Figure 7: Schematic showing the Dickson charge pump used in antifuse-based FPGAs.

Figure 5 shows such a case, where the I_{CC} is plotted against the total dose for a 0.8 µm, A1460A device. Near 30 krad, I_{CC} increases drastically and at about the same time the device stops functional. The root cause of this anomaly can be tracked down to the failure of a circuit called charge pump that controls the functionality of the device globally. As shown in Figure 6, the charge pump generates a voltage high than V_{CC} to open the isolation transistors so signals can go through the logic modules without degradation. This isolation scheme is to protect logic modules from the applied high voltage during programming. A classical Dickson charge pump circuit [8] is used (Figure 7) in antifuse devices. The radiation-induced edge leakage will increase reverse current leakage in the NMOS diode and consequently degrade V_{pump} and finally cause a functional failure in the device. The I_{CC} jump is due to the totem-pole current in the logic modules when the "high" signal degrades significantly below V_{CC}.

The propagation delay (T_{PD}) always degrades by radiation. The rationale cannot be qualitatively stated. Since there is little incentive to quantify it by performing a detailed SPICE simulation, it is accepted empirically. For technologies before 0.25 µm, there was no device failed T_{PD} before functional failure occurred. The pass/fail criterion of T_{PD} is 10% degradation. In 0.25 µm RT54SXS device, abnormally high propagation degradation was observed (Figure 8). Failure analysis revealed that the root cause again was the degradation of V_{pump}. The NMOS diode leakage in charge pump in this device was already fixed, and the result reflected on the high dose tolerance for functionality. However, the leakage paths in pass transistors from V_{pump} to the ground cause the degradation. These pass transistors are used to discharge the V_{pump} node during the programming. They are turned off during operation. These leakage paths were stopped and the improved result is shown in Figure 9. Note that Figure 8 uses longer buffer strings than those of Figure 9.

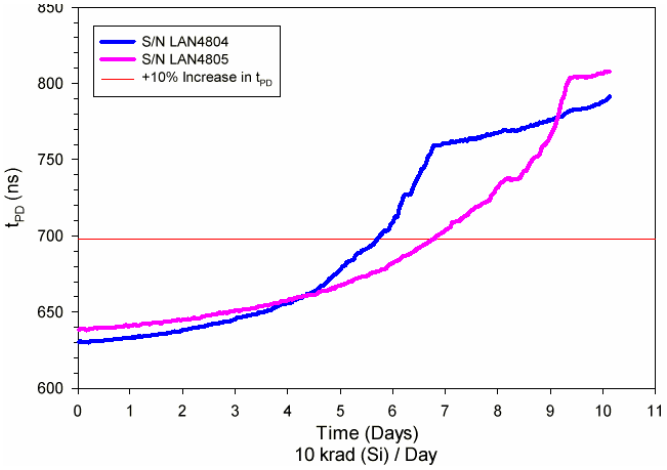

Figure 8: In-flux propagation delays of two pre-fixed 0.25 µm RTSX72S devices with serial number of LAN4804 and LAN4805.

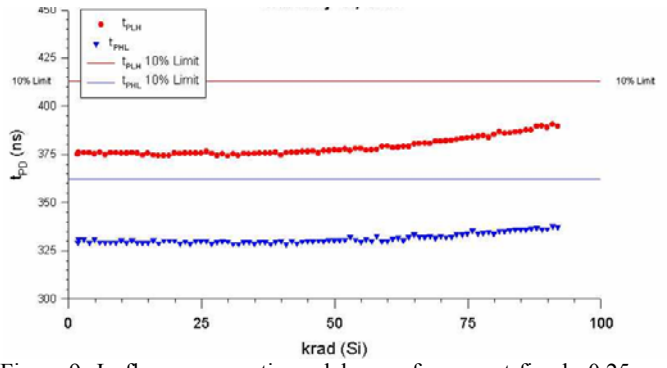

Figure 9: In-flux propagation delays of a post-fixed 0.25 µm RTSX32S device. T_{PLH} and T_{PHL} is measured low-to-high and high-to-low transition respectively.

Because of the weight premium in space flight crafts, the power supply has limited current drive capability. The transient current during power up can lock the supply and consequently cause mission failure. An early test [9] indicated that a modest radiation could induce a large transient current in the 1 µm A1280A device. One more time, charge pump degradation was suspected as the root cause. However, the behavior was dependent on the dose rate. As shown in Figure 10 [10], post-irradiation annealing at room temperature can reduce the radiation-induced transient to negligible. So in a low dose-rate environment such as space, this transient current is only a testing artifact. In later technologies, when low dose rate of 1 krad(Si)/day was used for irradiation, no significant radiation-induced power-up transient current was ever observed.

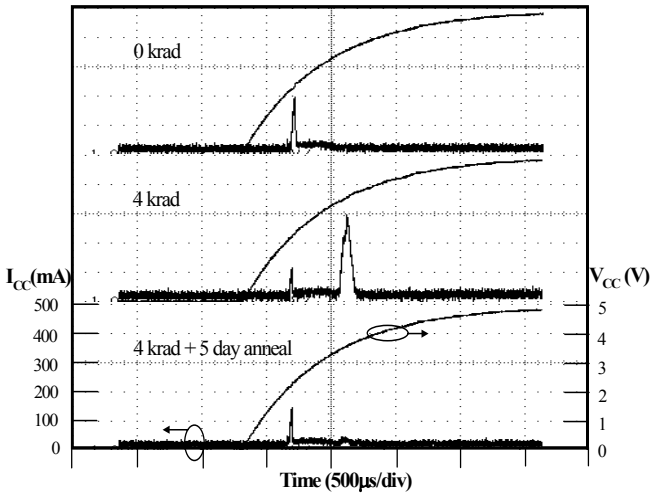

Figure 10: Startup transient current of a 1 µm A1280A device, measured pre and post-4 krad(Si)-irradiation, and also after 5 days of biased room temperature annealing [10].

C. TID Effects in Flash-based FPGA

So far, Flash-based devices have not been completely tested. The preliminary test results indicate distinctive abnormality, which is obviously attributed to the radiation effect on the floating-gate switch. Figure 11 shows the in-flux I_{CC} and propagation delay of the 0.25 µm A500K050 device. The cause of I_{CC} jump at the end of the experiment is not investigated yet. Radiation-induced degradation of Flash switches is conjectured to cause the significant propagation delay degradation with total dose. Since the Flash-switches directly pass the signal, the degradation of the switch threshold voltage (V_{TH}) by radiation-induced charge leakage in the floating gate can slow down the signal drastically. Also the radiation-induced traps in the floating gate can potentially impact the charge retention and consequently cause a long-term reliability issue (Figure 13). However, up to now, the radiation effect on the floating gate transistor is not well understood. A literature [2] predicted that it will limit the floating gate memory device to applications below 100 krad(Si).

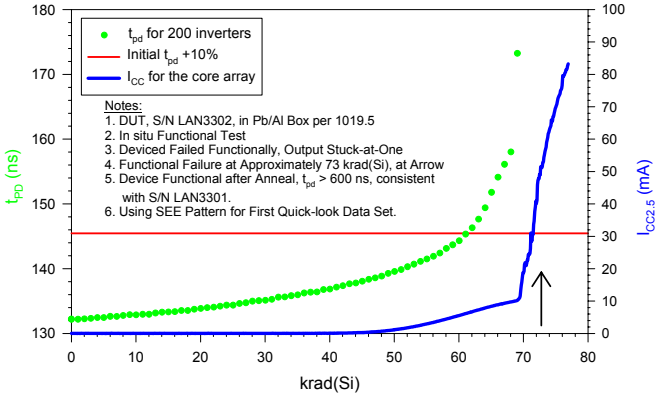

Figure 11: In-flux propagation delay and I_{CC} of a Flash-based 0.25 µm A500K050 device.

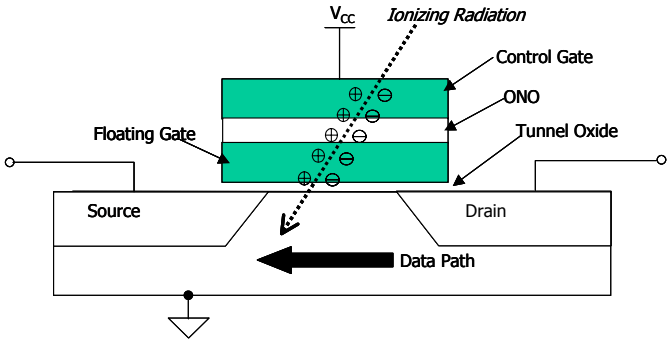

Figure 12: Schematic showing the effect of a heavy ion striking the floating gate transistor of the Flash switch.

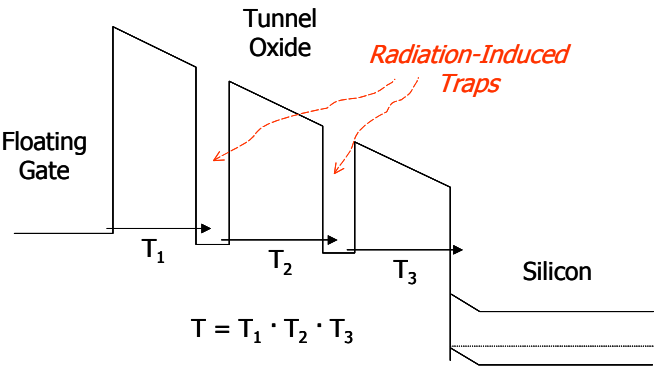

Figure 13: Energy band diagram showing the radiation induced traps and their effects on assisted-tunneling mechanisms.

D. TID Effects in SRAM-based FPGA

There is not much published literature on TID effects on SRAM-based FPGAs. A recent ESA report [11] indicates that after about 50 krad(Si) of gamma irradiation a power up failure occurred in the 0.22 µm XQVR300 device. A follow-up test [12] confirmed that even a high current power supply could not alter this result. Figure 14 shows the in-flux I_{CC} in one of the DUT. The root cause of this abnormality is not publicly known.

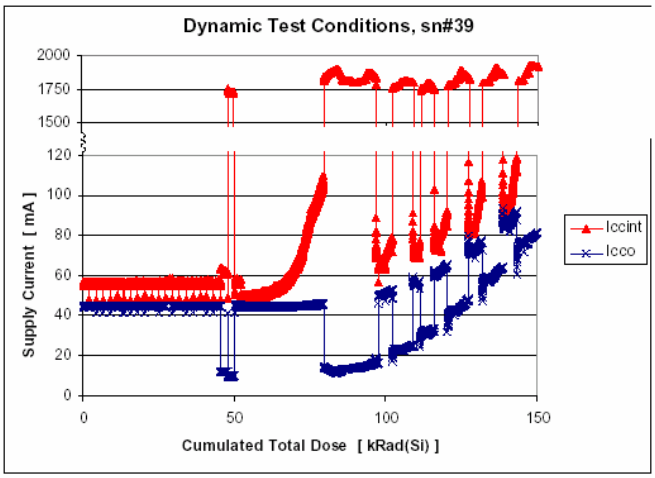

Figure 14: In-flux I_{CC} of a SRAM-based 0.22 µm XQVR300 device, the oscillation of the current is due to recycling power [11].

IV. Single Event Effects

Among various single event events, ones such as SEL causing hard errors are usually forbidden to occur in critical applications. However, SEL is a simple issue. Since its source is the PNPN parasitic in the CMOS structure, the complexity doesn't grow with the complexity of FPGAs. Also, the scaling decreases V_{CC} and alleviates the susceptibility of the SEL in the newer devices. On the other hand, SEU grows more complex and more susceptible as the scaling, function, and performance of FPGAs advance. Many new anomalies observed in new devices can be tracked down as SEUs in critical storage elements controlling the device function. In literatures, sometimes they were called single event functional interrupt (SEFI). The following presentation will focus on the SEU and its various manifestations in FPGAs.

A. Basic SEU Mechanisms

Two basic mechanisms are defined here. Figure 15 shows the occurrence of the SEU in a CMOS latch or SRAM cell. When ion strikes at the reverse biased drain junction of the NMOSFET in the "off" state, it causes the node voltage dropping from high to low. This transition propagates along the feedback loop and tries to rewrite the state. In the mean time there is a recover process that the "on" PMOSFET keeps pulling the struck node back to the original high state. The competition between the feedback process and recover process governs the SEU response. If the feedback process is longer, the node is recovered. If the recover process is longer, the node changes state and an SEU occurred.

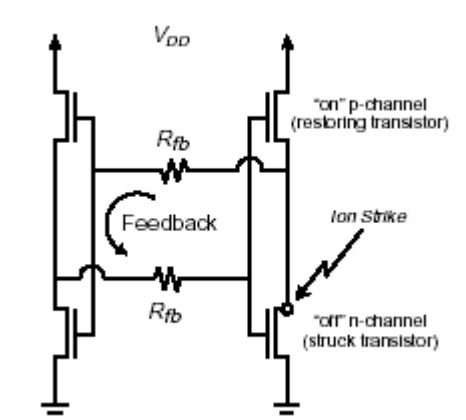

Figure 15: Competition between the feedback process and Recover process governs the SEU response of a latch (or SRAM cell) [13].

Figure 16 defines a general SEU. If the ion-strike-induced transient pulse can propagate through the network and result any error in a storage element, an SEU occurred. This type of SEU is often referred as combinational logic SEU, SET, or SET-induced SEU. This paper will refer it as SET for simplicity.

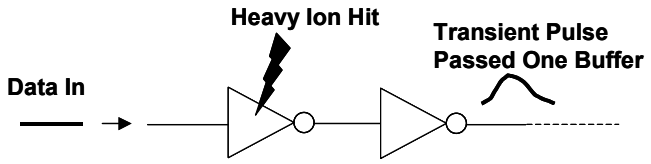

Figure 16: SET occurs when the ion induced pulse can propagate through the circuit network [14].

B. SEU in Antifuse-based FPGA

1) Testing Methodology

Simple testing designs are used to observe SEUs in antifuse-based FPGAs. Figure 17 shows the core concept in a block diagram. It originates from NASA Goddard Space Flight Center [15]. The DUT design consists of first-in-first-out (FIFO) shift registers. The data pattern of '1', '0', or checkerboard generated by an I/O-counter board is clocked into DUT. The standard data rate and clock frequency are 1 MHz. The output of each FIFO is checked with a control data pattern by a control chip to generate error pulses. The error pulses are then sent back and counted by the counter board. The I/O-counter board resides in a central controlling PC. Figure 18 shows an example of DUT board, on which the DUT, control chip and RS422 interfaces can be identified.

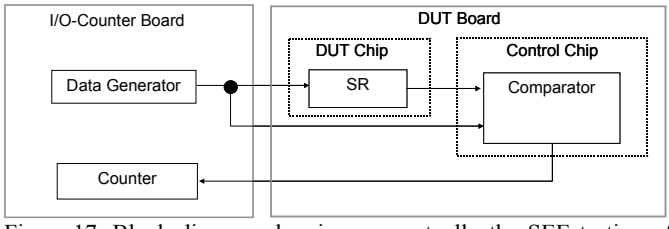

Figure 17: Block diagram showing conceptually the SEE testing of antifuse and Flash-based FPGAs. I/O-counter board resides in a central command controlling PC.

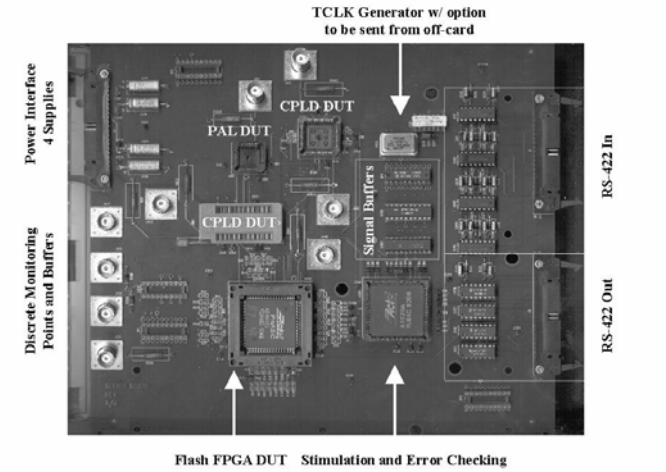

Figure 18: Photograph showing a SEE testing board for a Flash FPGA, arrows indicating DUT, control chip and a clock generator.

2) *SEU in Storage Elements*

The SEUs in storage elements were tested extensively in antifuse FPGAs [16]. The aforementioned basic mechanisms have already explained the behavior. The analysis and error-rate prediction in a radiation environment can be found, for example in Messenger's textbook [17].

3) *Clock Upset*

Clock upset was first observed in 1.0 µm RH1020 device [18]. Only checkerboard pattern can detect it. An SET occurring in the global clock network induces this anomaly. The SET changes the phase of the checkerboard pattern and produces an error burst. Figure 19 shows it schematically. The clock upset causes the error jump on top of the accumulated errors due to SEUs in flip-flops. This error jump has the maximum height of the number of bits in the shift register. Figure 20 shows the actual data. The shift register DOH consisting of triple-module-redundant (TMR) flip-flops only has jumps due to clock upsets, while the simple register DOS has both flip-flop SEUs and clock upsets. The sensitive sub-circuit in the clock network was identified and hardened. Figure 21 shows the result that the cross section of the clock upset in hardened device decreases significantly.

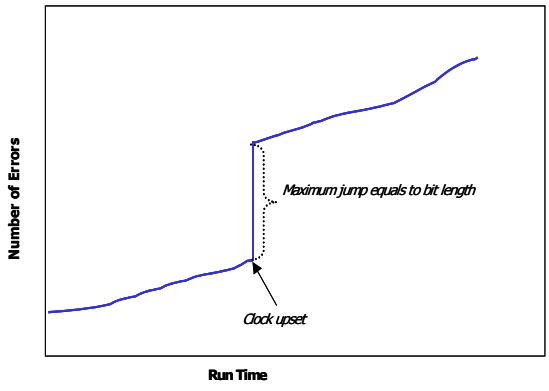

Figure 19: Schematic showing the in-flux SEU errors. The background continuous increase is due to SEUs in flip-flops, and the error jump is due to a clock upset.

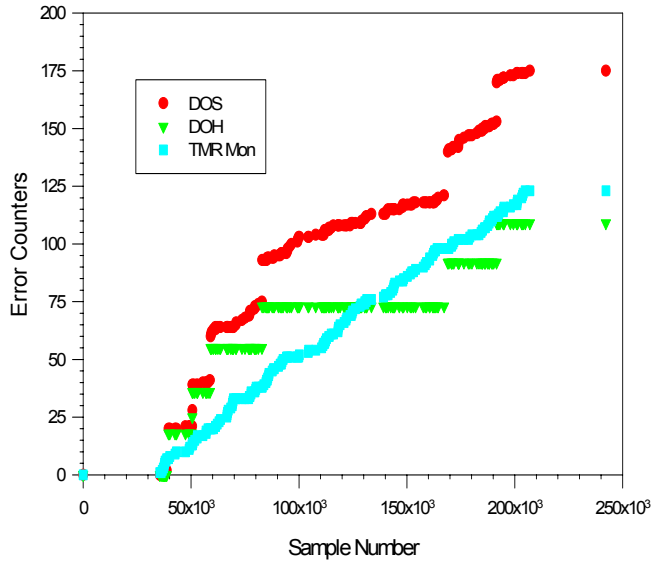

Figure 20: In-flux SEU errors. A TMR-flip-flops constructed shift register DOH shows only error jumps due to clock upsets, while a regular shift register DOS shows both flip-flop SEUs and clock upsets. Also notice that each clock upset occurred simultaneously in both DOH and DOS [20].

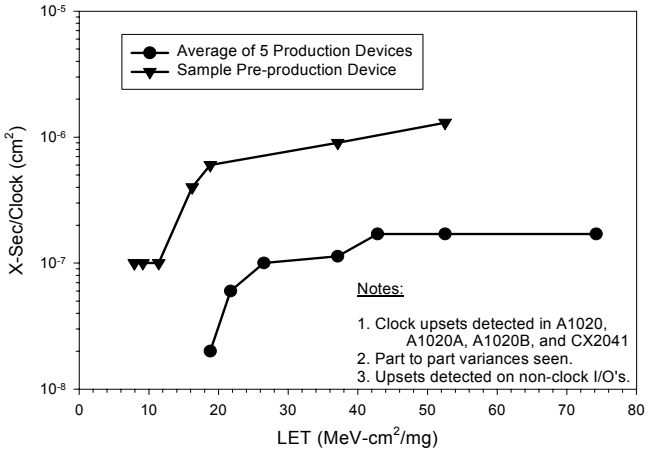

Figure 21: Comparison of pre and post-fixed RH1020 devices. Bottom curve was measured on the device after clock network was redesigned [20].

4) *Control Logic Upset*

The SEU in the state machine of the control logic in antifuse FPGAs can cause various anomalies. They often need careful circuit and logic analysis to be unambiguously identified. Two examples, JTAG upset and startup sequencer (SS) upset will be presented in the following.

JTAG refers to the circuitry built according to IEEE standard boundary-scan architecture [19]. It enables operations such as sampling the inputs, driving external pins, or presenting inputs to the core logic. As shown in Figure 22, the scan cells form a shift register. A test-access-port (TAP) controller commands the test interface and registers with a sixteen-state sequencer. During operation, TAP controller has to be reset to disable the JTAG. Unfortunately, hard reset by grounding a TRSTB pin is optional in the IEEE standard. If

TRSTB pin is not hardwire grounded, an SEU in TAP controller can activate the JTAG function and cause unpredictable effects on the device operation. Fig 23 shows the power supply current during JTAG upset in a proto-type 0.5 µm SX16 device. The I_{CC} of 5 V I/O power supply and 3.3 V logic-core power supply increased drastically and remained until power was recycled. This phenomenon is quite similar to latch-up. An extra TRSTB pin for reset grounding eliminates JTAG upset completely. Further details of JTAG upset can be found in a previous publication [20].

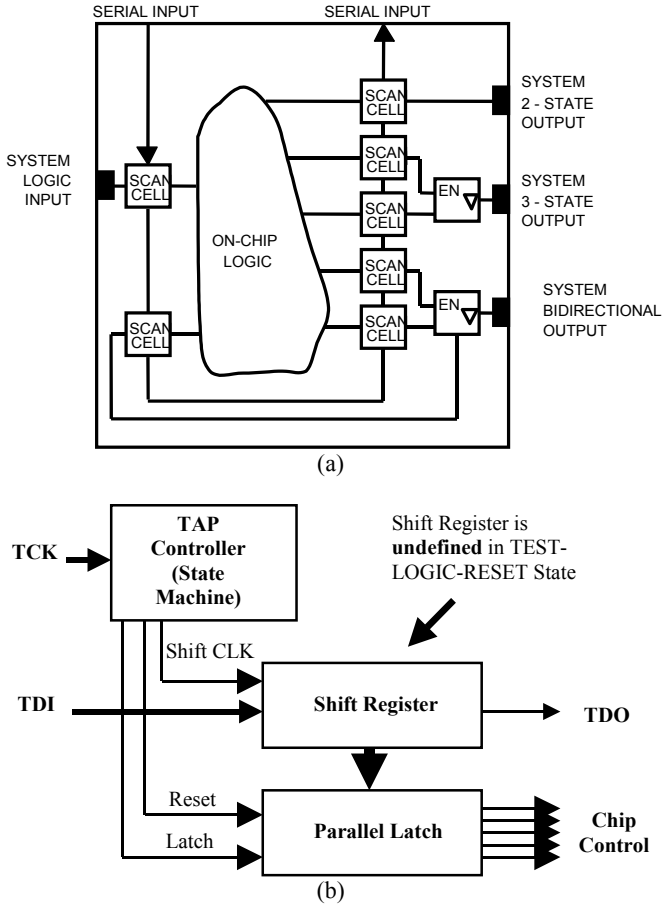

Figure 22: The schematics of the JTAG circuit, (a) shows the JTAG circuit construction on the chip, and (b) shows the block diagram of its state machine.

The SS upset is conceptually very similar to the JTAG upset. In state-of-the-art 0.15 µm AX family, SS is used to sequence the startup of various circuits to avoid the transient current. Figure 24 shows the function of one of the flip-flops in the SS. This TSSFF1 gates the input signal of the user FF. During operation, all the bits in the SS should be reset to '1'. An SEU in TSSFF1 will lock the input data of the user flip-flop to '0' and generate errors. In summary, SEUs in SS can have 8 different scenarios. One of them locks the device, and consequently power recycling is needed to recover the device function. However, once it is identified, it is straightforward to eliminate this SS upset by doubly redundant. The hardened version of the AX family, the RTAXS family has been tested without the SS-upset anomaly. Further details of SS upset can be found in a upcoming publication [21].

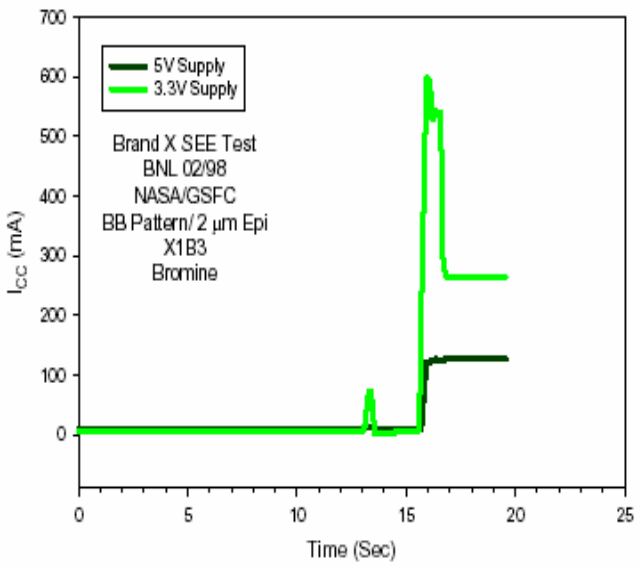

Figure 23: In-flux I_{CC} during heavy ion testing. JTAG upset can induce high current, which jumps up and down depending on the state of the JTAG state machine.

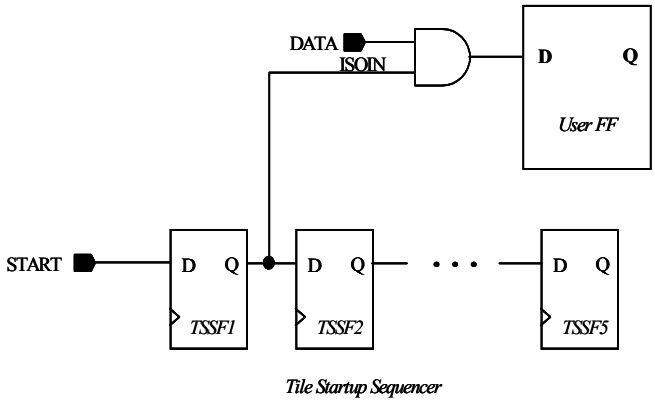

Figure 24: Schematic showing the startup sequencer controlling the data input to a user flip-flop.

5) SEU Hardening

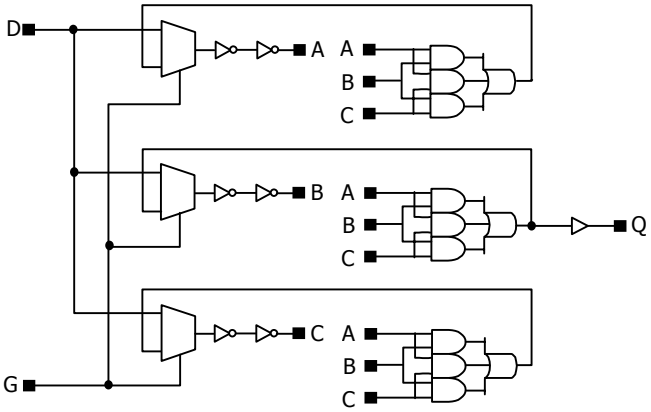

Figure 25: Schematic of an asynchronously TMR latch.

The flip-flops in an antifuse-based FPGA can be economically hardened by design (HBD. An asynchronously TMR latch has been implemented in both the master and slave of the flip-flops in 0.25 µm RTSXS devices. Figure 25 shows

the schematic of the asynchronously TMR latch. The hardened flip-flop has significant less SEU susceptibility. This technique has been extended to the recent 0.15 µm RTAXS devices. Preliminary test result (Figure 26) shows a similar hardening effect.

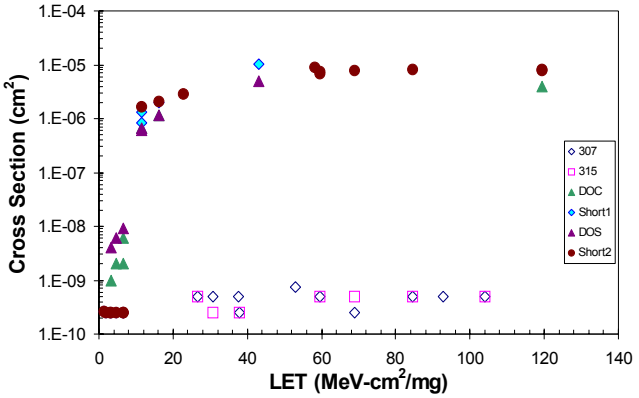

Figure 26: Preliminary SEU data of hardened RTAXS. The data in the bottom forming a horizontal line is measured from hardened device.

C. SEE in Flash-based FPGA

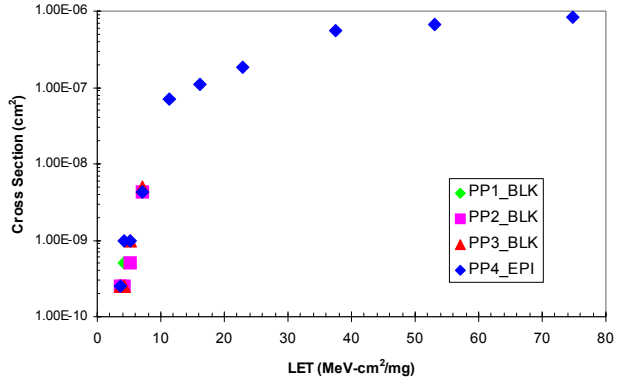

Figure 27: SEU data of a 0.22 µm APA750 device. Each different legend represents a different DUT.

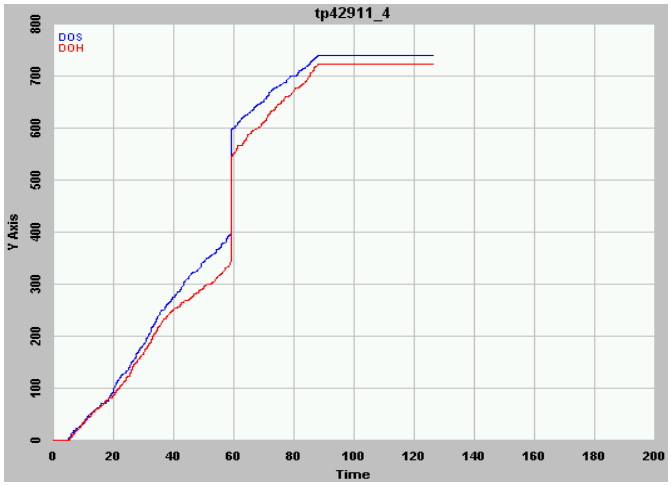

Figure 28: In-flux SEU errors of a 0.22 µm APA750 DUT. DOS and DOH each represents a shift register of 200 bits. A clock upset caused error jump occurs simultaneously in both shift register.

The first Flash-based FPGA device family, the ProASIC is prone to SEL. The new device, ProASIC^{PLUS} has improved reliability in every aspect. Using epi-substrate, it was tested for LET up to 104 MeV•cm^2/mg without SEL. The testing methodology is similar to that of the antifuse-based. Figure 27 shows the cross section per bit versus LET in the 0.22 µm APA750 device. Clock upsets were also observed. As shown in Figure 28, where a clock upset cause the simultaneously error jumps in both the DOS and DOH shift registers. Further test result to determine the threshold of the clock upset for is shown in Figure 29, where the threshold of clock upset is identified as between 18 to 20 MeV•cm^2/mg. Additional, there were no observable single event effects on the Flash-based switches.

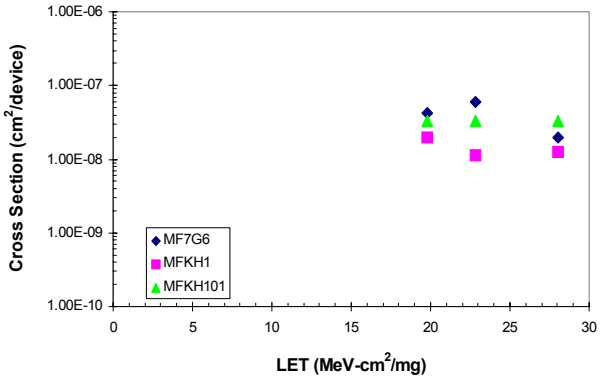

Figure 29: Cross section of clock upset versus LET measured in ProASIC Plus devices. The threshold is between 18 and 20 MeV•cm^2/mg.

D. SEE in SRAM-based FPGA

The SEU in SRAM switches (or configuration bits) dominates the SEE in SRAM-based FPGAs. However, the configuration malfunction masks the individual SEU anomaly and renders the unambiguous interpretation very difficult. For example, an upcoming paper [22] still tries to identify each SEU anomaly in the 0.22 µm Virtex XCV300 device manufactured by Xilinx. In general, 10% of configuration-bit upsets cause functional failures. However, the latency of uncorrected configuration bits is difficult to evaluate. Venders offer error software techniques such as detection and correction (EDAC) schemes to reduce the susceptibility.

VI. Conclusions

The radiation effects in non-volatile-switch based FPGAs, i.e. antifuse and Flash-based can be understood unambiguously by the basic mechanisms. Their hardening by hardware design is economically viable and has been done in state-of-the-art devices. Due to the sensitivity of the configuration bits, the radiation effects in volatile, SRAM switch based FPGA are difficult to analyze. Their hardening by hardware design is also difficult to justify by cost concerns.

VII Reference

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