CPPM, IN2P3-CNRS et Université d'Aix-Marseille II

Synchronization of optical links using the GOL with the TLK2501 or StratixGX buffers

LHCb Technical Note

Issue: 1
Revision: 0

Reference: LHCb 2004-012
Created: 2 February 2004
Last modified: 16 February 2004

Prepared by: E. Aslanides, J.P. Cachemiche, J. Cogan, B. Dinkespiler, P.Y. Duval, R. Le Gac, O. Leroy, P.L. Liotard, M. Menouni, L Tocco and A. Tsaregorodtsev

Abstract

In this note we clarify the synchronization design for optical links when using the GOL on the emission side, the TLK2501 deserializer from Texas Instrument or a StratixGX FPGA on the reception side. We conclude with few requirements.

Document Status Sheet

1. Document title: Synchronization of optical links using the GOL with the TLK2501 or StratixGX buffers			
2. Document Reference Number: LHCb 2004-012			
3. Issue	**4. Revision**	**5. Date**	**6. Reason for change**
1	0	2 February 2004	• First draft

Table of Contents

1 Introduction

In LHCb optical links, serializers are used to encode 32 bits words in a serial stream. The frequency of input words is 40 MHz, while the frequency of the output stream is 1.6 Ghz.

Once encoded in serial stream the words boundaries, i.e. the limits between two consecutive words, cannot be detected by the receiver without a specific procedure. This procedure is required either at power-up or if the synchronization is lost.

It is based on the emission of a specific IDLE sequence by the emission side.

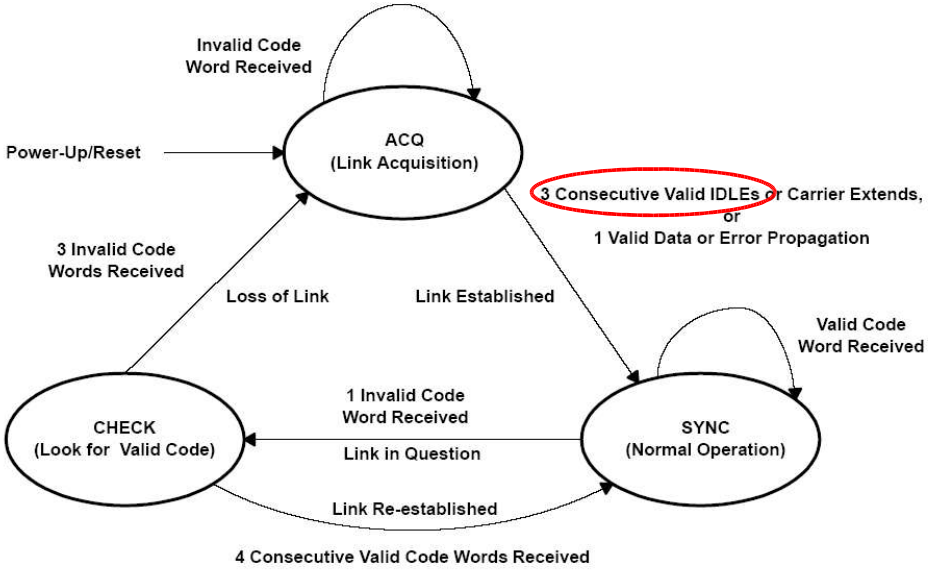

Figure 1: Resynchronization principle according to TI documentation

The TLK2501 documentation [1] is ambiguous on this aspect. It makes allusion to the use of **three consecutive 16 bits IDLE cycles** as shown in Figure 1. This requirement also appears in the Gigabit Ethernet standard [2] on which the TLK2501 is based, as can be seen on Figure 2. In our initial Optical Link Specification [3] we only specified **two** (or one 32 bits IDLE cycle).

In this note we clarify the procedure allowing to synchronize the GOL[1] with the TLK2501[2]. In addition, we also study the case where the TLK2501 receiver is

1 Information based on explanations received from the GOL designers

2 Information based on explanations received from the TLK2501 Field Application Engineers

replaced by deserializers directly included in a StratixGX FPGA[3].

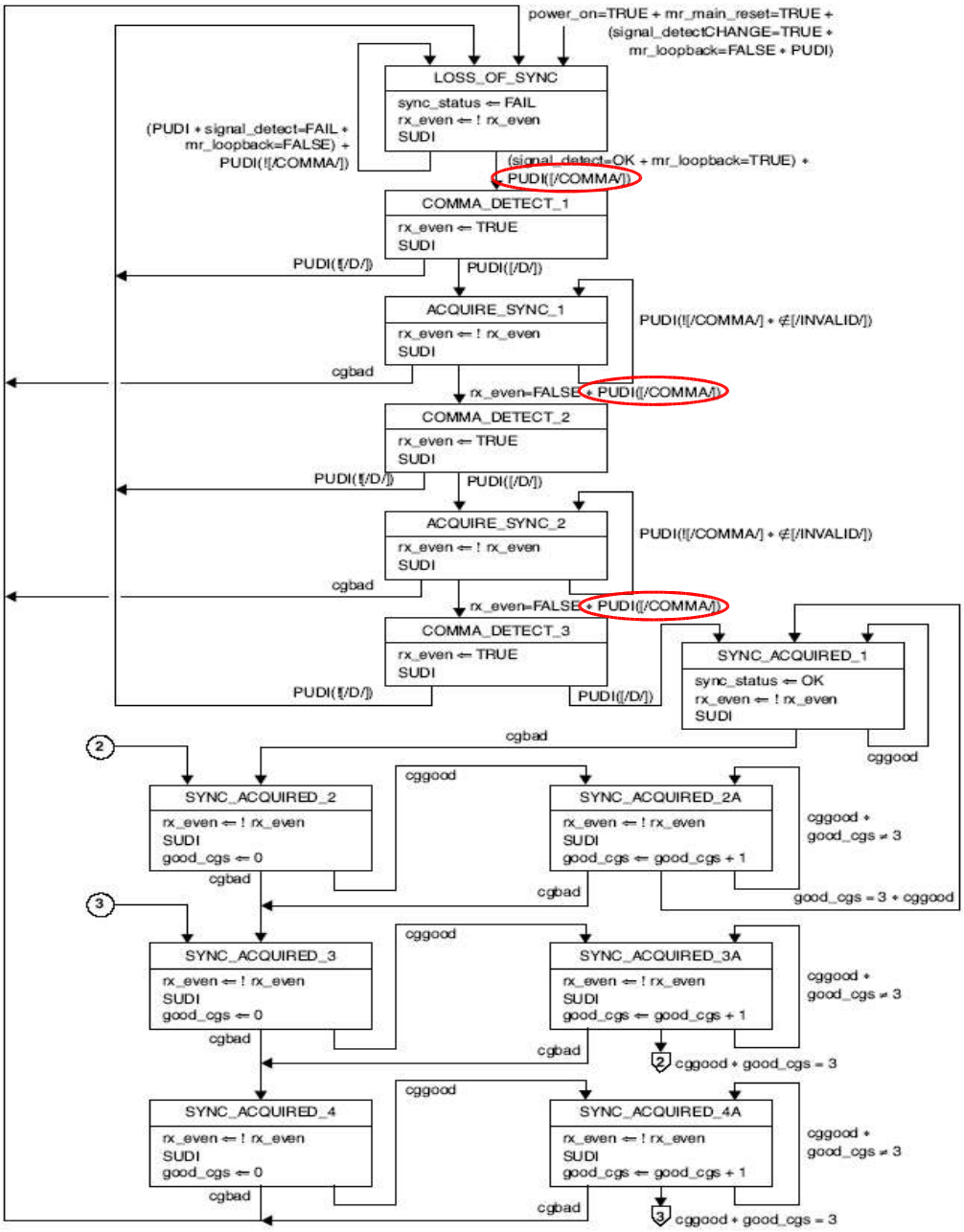

Figure 2: Gibabit Ethernet synchronization principle extracted from the IEEE802.3 standard

When in the LOSS_OF_SYNC state, it can be seen that three consecutive ordered sets are expected before the state machine can go in the SYNC_ACQUIRED state

3 Information based on the Altera documentation, explanations received from the StratixGX Field Application Engineers and simulations made with Quartus.

2 Synchronization principle for the TLK2501

The GOL as well as the TLK2501 are based on the physical layer of the IEEE802.3 standard. Data transmitted are encoded according the 8b10b scheme given in Annex 1.

We remind that the 8b10b scheme encodes 8 bits words into 10 bits words. The 10 bits codes are chosen to contain:

- either 6 zeros and 4 ones;
- or 4 zeros and 6 ones;
- or 5 zeros and 5 ones;

The purpose of this encoding is to balance the number of ones and zeros transmitted and therefore to avoid the apparition of a DC level. However to achieve this an additional mechanism is required. Each 8 bit data word has two complementary representations in the 10 bit space: a positive and a negative one. To choose between them the running disparity is computed dynamically by counting the number of *one* bits and the number of *zero* bits. If for example the disparity of data already sent is negative (more zeros than ones) the positive value of the next code is chosen (more ones than zeros). This equilibrates the quantity of zeros and ones transmitted.

The 8b10b encoding maps 256 characters tagged as data (Dx.y) and 12 additional characters tagged as controls (Kx.y) as shown in Annex 1. Controls characters are forced on the emission side by asserting or de-asserting control signals[4]. The way it is done depends on the emission device.

To find words boundaries in the bit stream code, the TLK2501 uses a comma character whose binary value is 0011111. This value is included in the positive version of the /K28.5/ code (0011111010). The particularity of this code is that it cannot be included in any other code nor in any combination of codes chosen within the 8b10b dictionary.

The Gigabit Ethernet standard recommends the emission of 3 consecutive IDLE ordered sets to synchronize the receiver. There are two kinds of IDLE ordered sets: [K28.5, D5.6] named /I1/ and [K28.5, D16.2] named /I2/ according to the standard.

4 For example TX-ER and TX_DV on a TLK2501, Tx_Er and Tx_En on a GOL

The sequence of order sets follows the following rule :

- If the running disparity before the first IDLE ordered set is positive, a /I1/ will be chosen as shown in Table 1 ;
- If the running disparity before the first IDLE ordered set is negative, an /I2/ will be chosen as shown in Table 2 ;
- For the two next IDLE ordered sets a /I2/ will be systematically chosen.

Ordered set	/I1/		/I2/		/I2/	
Character	K28.5	D5.6	K28.5	D16.2	K28.5	D16.2
8b10b code	110000 0101	101001 0110	**001111 1**010	100100 1010	**001111 1**010	100100 1010
8 bits value code	BC	C5	BC	50	BC	50
Running disparity Initial value +	-	-	+	-	+	-

Table 1 : IDLE sequence for initial running disparity positive

Ordered set	/I2/		/I2/		/I2/	
Character	K28.5	D16.2	K28.5	D16.2	K28.5	D16.2
8b10b code	**001111 1**010	100100 1010	**001111 1**010	100100 1010	**001111 1**010	100100 1010
8 bits value code	BC	50	BC	50	BC	50
Running disparity Initial value -	+	-	+	-	+	-

Table 2 : IDLE sequence for initial running disparity negative

The disparity after a /I1/ ordered set changes its sign, while it is the same after a /I2/ ordered set. By judiciously choosing /I1/ or /I2/in function of the initial running disparity, we can force a negative running disparity at the end of the first IDLE ordered set, and **t**he positive comma is therefore systematically present at the second and third IDLE ordered set.

Note that **only 2 consecutive IDLE ordered sets are necessary and sufficient for the TLK2501 to get the alignment** because it uses the positive comma to synchronize.

The state machine shown in Figure 1 must be interpreted as follows: when in ACQ state, the TLK2501 counts the number of IDLE ordered sets received; if three IDLE ordered sets are consecutively received it goes in SYNC state; if less ordered cycles are received, it goes in SYNC state as soon as it receives a valid data word. Thus the TLK2501 is able to find word boundaries with only **two** consecutive ordered sets if they are emitted according to rules stated above.

3 Synchronization principle for a Stratix GX

The StratixGX [5] includes High Speed Buffers (HSB) with serialization/ deserialization capabilities similar to the TLK2501 ones. It can be configured according various standards including Gigabit Ethernet. In this case 3 consecutive ordered sets are required for synchronization.

However the StratixGX buffer can also be configured in manual mode allowing more flexibility.

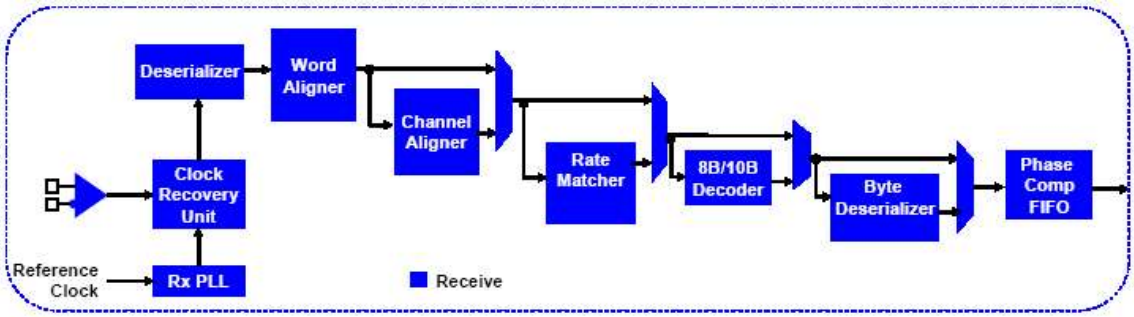

Figure 3: StratixGX receiver block

The Word Aligner of a receiver block shown in Figure 3 contains a Pattern Detector. The Pattern Detector matches a pre-defined comma to detect the byte-boundary. If the comma is found, a signal (*rx_patterndetect*) is asserted for the duration of one clock cycle to signify that the comma exists in the current word boundary.

Both positive and negative disparities are checked in this mode. For example if a /K28.5/ (b'0011111010) pattern is specified as the comma, the *rx_patterndetect* will be asserted if b'0011111010 **or** b'1100000101 is detected in the incoming data.

In manual mode, the synchronization procedure is as follows : when the signal commanding the synchronization (*rx_enacdet*) is high, the word aligner is going to detect the specified comma and re-align the byte boundary when needed. When the comma is detected, the *rx_patterndetect* signal is asserted and a *rx_syncstatus* signal is also asserted for one clock cycle to signify that the word boundary has been synchronized. When this condition is met, the *rx_enacdet* signal must be deasserted by the user's logic. This causes the current word boundary to be locked.

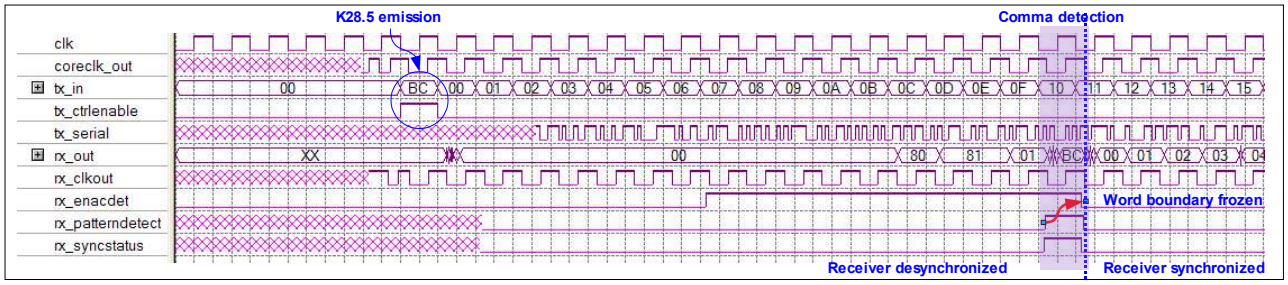

Figure 4: Resynchronization of a StratixGX buffer operating in 8 bits mode with a single comma word (K28.5)

On the simulation shown in Figure 4 one can notice that all this synchronization process can be executed on detection of a single 8 bits word. **By adding appropriate logic inside the FPGA**, it is possible to synchronize on one or two predefined 16 bits IDLE ordered set, for example on the occurrence of either /I1/ or /I2/ just like in the TLK2501.

Because it can detect a positive as well as a negative coma**, the StratixGX is able to synchronize on a single IDLE 16 bits cycle** instead of 2 for the TLK2501.

4 IDLE cycle management for the GOL

The GOL chip has a 32 bits data input operating at 40 MHz and 2 control signals: Tx_En and Tx_Er.

The production of IDLE ordered sets is obtained by de-asserting the Tx_En input. As the data path is 32 bits, the de-assertion of Tx_En during one cycle at 40 MHz corresponds to the emission of two consecutive ordered sets. The GOL follows the Gigabit Ethernet rules concerning the running disparity. Therefore the IDLE cycles emitted during one cycle will be [/I1/, /I2/] or [/I2/, /I2/] according to the detected parity. These two ordered sets are sufficient for a TLK2501 or a Stratix GX to synchronize.

5 Recommendations

The synchronization sequence is an **essential operation** for the correct functioning of the pipelines located behind the deserializers. For this reason, the following recommendations go beyond the strict minimum described above. This is the price to pay for securing this feature.

Even if the assertion of Tx_En during a single cycle at 40 MHz[5] is sufficient to synchronize the receiving end, it is felt that making this number of cycles programmable could be a security in the case where external perturbation would jeopardize the synchronization sequence.

Moreover, in the case where a specific initialization would be required prior to start the processing, the time at which the Data Valid on the receiving TLK2501 rises should be programmable. As the Data Valid is the image of the Tx_En on the GOL, this is equivalent to make programmable the time at which the Tx_En rises.

This can be achieved in programming the start and stop time of the Tx_En signal.

A possible implementation could be that the device driving the Tx_En signal on the emission board had two 16 bits registers accessible by the ECS: one with the number of the machine cycle at which the Tx_En signal must be asserted, a second with the number of the machine cycle at which the Tx_En signal must be de-asserted.

In the example shown in Figure 5, the start value is programmed to 3549 and the end value is programmed to 0. This way we obtain a 16 cycles large de-asserted Tx_En signal with a rising edge toggling synchronously with the first valid data of the machine cycle.

5 Be aware that clock cycles are not the same on the StratixGX (160 MHz), on the TLK2501 (80 MHz) and on the GOL (40 MHz). The assertion of Tx_En during one cycle on the COL corresponds to the reception of 2 cycles on the TLK2501 and 4 cycles on the StratixGX.

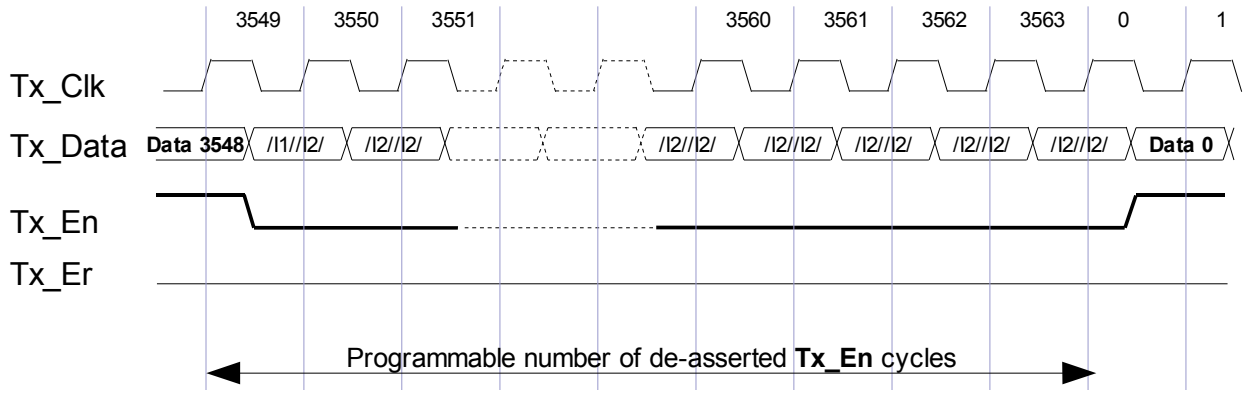

Figure 5: Example of TX_En management on the GOL side for a running disparity negative at end of cycle 3548

6 Conclusion

We have clarified the behaviour of the TLK2501 on the reception side.

The initial specification of the Optical link interface [3] correctly described the number of cycle during which Data Valid has to be de-asserted for allowing the processing board devices to re-synchronize.

However it is recommended to reinforce the security of the synchronization process which appears as a key issue for the correct operation of the downstream electronics . This could be reached by making programmable both the beginning and end of the Tx_En signal de-assertion on the GOL side.

Annex 1: 8b10b code

Valid data code-groups

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD – abcdei fghj	Current RD + abcdei fghj
D0.0	00	000 00000	100111 0100	011000 1011
D1.0	01	000 00001	011101 0100	100010 1011
D2.0	02	000 00010	101101 0100	010010 1011
D3.0	03	000 00011	110001 1011	110001 0100
D4.0	04	000 00100	110101 0100	001010 1011
D5.0	05	000 00101	101001 1011	101001 0100
D6.0	06	000 00110	011001 1011	011001 0100
D7.0	07	000 00111	111000 1011	000111 0100
D8.0	08	000 01000	111001 0100	000110 1011
D9.0	09	000 01001	100101 1011	100101 0100
D10.0	0A	000 01010	010101 1011	010101 0100
D11.0	0B	000 01011	110100 1011	110100 0100
D12.0	0C	000 01100	001101 1011	001101 0100
D13.0	0D	000 01101	101100 1011	101100 0100
D14.0	0E	000 01110	011100 1011	011100 0100
D15.0	0F	000 01111	010111 0100	101000 1011
D16.0	10	000 10000	011011 0100	100100 1011
D17.0	11	000 10001	100011 1011	100011 0100
D18.0	12	000 10010	010011 1011	010011 0100
D19.0	13	000 10011	110010 1011	110010 0100
D20.0	14	000 10100	001011 1011	001011 0100
D21.0	15	000 10101	101010 1011	101010 0100
D22.0	16	000 10110	011010 1011	011010 0100
D23.0	17	000 10111	111010 0100	000101 1011
D24.0	18	000 11000	110011 0100	001100 1011
D25.0	19	000 11001	100110 1011	100110 0100
D26.0	1A	000 11010	010110 1011	010110 0100
D27.0	1B	000 11011	110110 0100	001001 1011
D28.0	1C	000 11100	001110 1011	001110 0100
D29.0	1D	000 11101	101110 0100	010001 1011
D30.0	1E	000 11110	011110 0100	100001 1011
D31.0	1F	000 11111	101011 0100	010100 1011
D0.1	20	001 00000	100111 1001	011000 1001
D1.1	21	001 00001	011101 1001	100010 1001
D2.1	22	001 00010	101101 1001	010010 1001
D3.1	23	001 00011	110001 1001	110001 1001
D4.1	24	001 00100	110101 1001	001010 1001
D5.1	25	001 00101	101001 1001	101001 1001
D6.1	26	001 00110	011001 1001	011001 1001
D7.1	27	001 00111	111000 1001	000111 1001
D8.1	28	001 01000	111001 1001	000110 1001
D9.1	29	001 01001	100101 1001	100101 1001
D10.1	2A	001 01010	010101 1001	010101 1001
D11.1	2B	001 01011	110100 1001	110100 1001
D12.1	2C	001 01100	001101 1001	001101 1001
D13.1	2D	001 01101	101100 1001	101100 1001
D14.1	2E	001 01110	011100 1001	011100 1001
D15.1	2F	001 01111	010111 1001	101000 1001
D16.1	30	001 10000	011011 1001	100100 1001
D17.1	31	001 10001	100011 1001	100011 1001
D18.1	32	001 10010	010011 1001	010011 1001
D19.1	33	001 10011	110010 1001	110010 1001
D20.1	34	001 10100	001011 1001	001011 1001
D21.1	35	001 10101	101010 1001	101010 1001
D22.1	36	001 10110	011010 1001	011010 1001
D23.1	37	001 10111	111010 1001	000101 1001
D24.1	38	001 11000	110011 1001	001100 1001
D25.1	39	001 11001	100110 1001	100110 1001
D26.1	3A	001 11010	010110 1001	010110 1001
D27.1	3B	001 11011	110110 1001	001001 1001

(continued)

Valid data code-groups

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD – abcdei fghj	Current RD + abcdei fghj
D28.1	3C	001 11100	001110 1001	001110 1001
D29.1	3D	001 11101	101110 1001	010001 1001
D30.1	3E	001 11110	011110 1001	100001 1001
D31.1	3F	001 11111	101011 1001	010100 1001
D0.2	40	010 00000	100111 0101	011000 0101
D1.2	41	010 00001	011101 0101	100010 0101
D2.2	42	010 00010	101101 0101	010010 0101
D3.2	43	010 00011	110001 0101	110001 0101
D4.2	44	010 00100	110101 0101	001010 0101
D5.2	45	010 00101	101001 0101	101001 0101
D6.2	46	010 00110	011001 0101	011001 0101
D7.2	47	010 00111	111000 0101	000111 0101
D8.2	48	010 01000	111001 0101	000110 0101
D9.2	49	010 01001	100101 0101	100101 0101
D10.2	4A	010 01010	010101 0101	010101 0101
D11.2	4B	010 01011	110100 0101	110100 0101
D12.2	4C	010 01100	001101 0101	001101 0101
D13.2	4D	010 01101	101100 0101	101100 0101
D14.2	4E	010 01110	011100 0101	011100 0101
D15.2	4F	010 01111	010111 0101	101000 0101
D16.2	50	010 10000	011011 0101	100100 0101
D17.2	51	010 10001	100011 0101	100011 0101
D18.2	52	010 10010	010011 0101	010011 0101
D19.2	53	010 10011	110010 0101	110010 0101
D20.2	54	010 10100	001011 0101	001011 0101
D21.2	55	010 10101	101010 0101	101010 0101
D22.2	56	010 10110	011010 0101	011010 0101
D23.2	57	010 10111	111010 0101	000101 0101
D24.2	58	010 11000	110011 0101	001100 0101
D25.2	59	010 11001	100110 0101	100110 0101
D26.2	5A	010 11010	010110 0101	010110 0101
D27.2	5B	010 11011	110110 0101	001001 0101
D28.2	5C	010 11100	001110 0101	001110 0101
D29.2	5D	010 11101	101110 0101	010001 0101
D30.2	5E	010 11110	011110 0101	100001 0101
D31.2	5F	010 11111	101011 0101	010100 0101
D0.3	60	011 00000	100111 0011	011000 1100
D1.3	61	011 00001	011101 0011	100010 1100
D2.3	62	011 00010	101101 0011	010010 1100
D3.3	63	011 00011	110001 1100	110001 0011
D4.3	64	011 00100	110101 0011	001010 1100
D5.3	65	011 00101	101001 1100	101001 0011
D6.3	66	011 00110	011001 1100	011001 0011
D7.3	67	011 00111	111000 1100	000111 0011
D8.3	68	011 01000	111001 0011	000110 1100
D9.3	69	011 01001	100101 1100	100101 0011
D10.3	6A	011 01010	010101 1100	010101 0011
D11.3	6B	011 01011	110100 1100	110100 0011
D12.3	6C	011 01100	001101 1100	001101 0011
D13.3	6D	011 01101	101100 1100	101100 0011
D14.3	6E	011 01110	011100 1100	011100 0011
D15.3	6F	011 01111	010111 0011	101000 1100
D16.3	70	011 10000	011011 0011	100100 1100
D17.3	71	011 10001	100011 1100	100011 0011
D18.3	72	011 10010	010011 1100	010011 0011
D19.3	73	011 10011	110010 1100	110010 0011
D20.3	74	011 10100	001011 1100	001011 0011
D21.3	75	011 10101	101010 1100	101010 0011
D22.3	76	011 10110	011010 1100	011010 0011
D23.3	77	011 10111	111010 0011	000101 1100

(continued)

Valid data code-groups

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD – abcdei fghj	Current RD + abcdei fghj
D24.3	78	011 11000	110011 0011	001100 1100
D25.3	79	011 11001	100110 1100	100110 0011
D26.3	7A	011 11010	010110 1100	010110 0011
D27.3	7B	011 11011	110110 0011	001001 1100
D28.3	7C	011 11100	001110 1100	001110 0011
D29.3	7D	011 11101	101110 0011	010001 1100
D30.3	7E	011 11110	011110 0011	100001 1100
D31.3	7F	011 11111	101011 0011	010100 1100
D0.4	80	100 00000	100111 0010	011000 1101
D1.4	81	100 00001	011101 0010	100010 1101
D2.4	82	100 00010	101101 0010	010010 1101
D3.4	83	100 00011	110001 1101	110001 0010
D4.4	84	100 00100	110101 0010	001010 1101
D5.4	85	100 00101	101001 1101	101001 0010
D6.4	86	100 00110	011001 1101	011001 0010
D7.4	87	100 00111	111000 1101	000111 0010
D8.4	88	100 01000	111001 0010	000110 1101
D9.4	89	100 01001	100101 1101	100101 0010
D10.4	8A	100 01010	010101 1101	010101 0010
D11.4	8B	100 01011	110100 1101	110100 0010
D12.4	8C	100 01100	001101 1101	001101 0010
D13.4	8D	100 01101	101100 1101	101100 0010
D14.4	8E	100 01110	011100 1101	011100 0010
D15.4	8F	100 01111	010111 0010	101000 1101
D16.4	90	100 10000	011011 0010	100100 1101
D17.4	91	100 10001	100011 1101	100011 0010
D18.4	92	100 10010	010011 1101	010011 0010
D19.4	93	100 10011	110010 1101	110010 0010
D20.4	94	100 10100	001011 1101	001011 0010
D21.4	95	100 10101	101010 1101	101010 0010
D22.4	96	100 10110	011010 1101	011010 0010
D23.4	97	100 10111	111010 0010	000101 1101
D24.4	98	100 11000	110011 0010	001100 1101
D25.4	99	100 11001	100110 1101	100110 0010
D26.4	9A	100 11010	010110 1101	010110 0010
D27.4	9B	100 11011	110110 0010	001001 1101
D28.4	9C	100 11100	001110 1101	001110 0010
D29.4	9D	100 11101	101110 0010	010001 1101
D30.4	9E	100 11110	011110 0010	100001 1101
D31.4	9F	100 11111	101011 0010	010100 1101
D0.5	A0	101 00000	100111 1010	011000 1010
D1.5	A1	101 00001	011101 1010	100010 1010
D2.5	A2	101 00010	101101 1010	010010 1010
D3.5	A3	101 00011	110001 1010	110001 1010
D4.5	A4	101 00100	110101 1010	001010 1010
D5.5	A5	101 00101	101001 1010	101001 1010
D6.5	A6	101 00110	011001 1010	011001 1010
D7.5	A7	101 00111	111000 1010	000111 1010
D8.5	A8	101 01000	111001 1010	000110 1010
D9.5	A9	101 01001	100101 1010	100101 1010
D10.5	AA	101 01010	010101 1010	010101 1010
D11.5	AB	101 01011	110100 1010	110100 1010
D12.5	AC	101 01100	001101 1010	001101 1010
D13.5	AD	101 01101	101100 1010	101100 1010
D14.5	AE	101 01110	011100 1010	011100 1010
D15.5	AF	101 01111	010111 1010	101000 1010
D16.5	B0	101 10000	011011 1010	100100 1010
D17.5	B1	101 10001	100011 1010	100011 1010
D18.5	B2	101 10010	010011 1010	010011 1010
D19.5	B3	101 10011	110010 1010	110010 1010

(continued)

Valid data code-groups

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD – abcdei fghj	Current RD + abcdei fghj
D20.5	B4	101 10100	001011 1010	001011 1010
D21.5	B5	101 10101	101010 1010	101010 1010
D22.5	B6	101 10110	011010 1010	011010 1010
D23.5	B7	101 10111	111010 1010	000101 1010
D24.5	B8	101 11000	110011 1010	001100 1010
D25.5	B9	101 11001	100110 1010	100110 1010
D26.5	BA	101 11010	010110 1010	010110 1010
D27.5	BB	101 11011	110110 1010	001001 1010
D28.5	BC	101 11100	001110 1010	001110 1010
D29.5	BD	101 11101	101110 1010	010001 1010
D30.5	BE	101 11110	011110 1010	100001 1010
D31.5	BF	101 11111	101011 1010	010100 1010
D0.6	C0	110 00000	100111 0110	011000 0110
D1.6	C1	110 00001	011101 0110	100010 0110
D2.6	C2	110 00010	101101 0110	010010 0110
D3.6	C3	110 00011	110001 0110	110001 0110
D4.6	C4	110 00100	110101 0110	001010 0110
D5.6	C5	110 00101	101001 0110	101001 0110
D6.6	C6	110 00110	011001 0110	011001 0110
D7.6	C7	110 00111	111000 0110	000111 0110
D8.6	C8	110 01000	111001 0110	000110 0110
D9.6	C9	110 01001	100101 0110	100101 0110
D10.6	CA	110 01010	010101 0110	010101 0110
D11.6	CB	110 01011	110100 0110	110100 0110
D12.6	CC	110 01100	001101 0110	001101 0110
D13.6	CD	110 01101	101100 0110	101100 0110
D14.6	CE	110 01110	011100 0110	011100 0110
D15.6	CF	110 01111	010111 0110	101000 0110
D16.6	D0	110 10000	011011 0110	100100 0110
D17.6	D1	110 10001	100011 0110	100011 0110
D18.6	D2	110 10010	010011 0110	010011 0110
D19.6	D3	110 10011	110010 0110	110010 0110
D20.6	D4	110 10100	001011 0110	001011 0110
D21.6	D5	110 10101	101010 0110	101010 0110
D22.6	D6	110 10110	011010 0110	011010 0110
D23.6	D7	110 10111	111010 0110	000101 0110
D24.6	D8	110 11000	110011 0110	001100 0110
D25.6	D9	110 11001	100110 0110	100110 0110
D26.6	DA	110 11010	010110 0110	010110 0110
D27.6	DB	110 11011	110110 0110	001001 0110
D28.6	DC	110 11100	001110 0110	001110 0110
D29.6	DD	110 11101	101110 0110	010001 0110
D30.6	DE	110 11110	011110 0110	100001 0110
D31.6	DF	110 11111	101011 0110	010100 0110
D0.7	E0	111 00000	100111 0001	011000 1110
D1.7	E1	111 00001	011101 0001	100010 1110
D2.7	E2	111 00010	101101 0001	010010 1110
D3.7	E3	111 00011	110001 1110	110001 0001
D4.7	E4	111 00100	110101 0001	001010 1110
D5.7	E5	111 00101	101001 1110	101001 0001
D6.7	E6	111 00110	011001 1110	011001 0001
D7.7	E7	111 00111	111000 1110	000111 0001
D8.7	E8	111 01000	111001 0001	000110 1110
D9.7	E9	111 01001	100101 1110	100101 0001
D10.7	EA	111 01010	010101 1110	010101 0001
D11.7	EB	111 01011	110100 1110	110100 1000
D12.7	EC	111 01100	001101 1110	001101 0001
D13.7	ED	111 01101	101100 1110	101100 1000
D14.7	EE	111 01110	011100 1110	011100 1000
D15.7	EF	111 01111	010111 0001	101000 1110

(continued)

Valid data code-groups

Code Group Name	Octet Value	Octet Bits HGF EDCBA	Current RD –	Current RD +
			abcdei fghj	abcdei fghj
D16.7	F0	111 10000	011011 0001	100100 1110
D17.7	F1	111 10001	100011 0111	100011 0001
D18.7	F2	111 10010	010011 0111	010011 0001
D19.7	F3	111 10011	110010 1110	110010 0001
D20.7	F4	111 10100	001011 0111	001011 0001
D21.7	F5	111 10101	101010 1110	101010 0001
D22.7	F6	111 10110	011010 1110	011010 0001
D23.7	F7	111 10111	111010 0001	000101 1110
D24.7	F8	111 11000	110011 0001	001100 1110
D25.7	F9	111 11001	100110 1110	100110 0001
D26.7	FA	111 11010	010110 1110	010110 0001
D27.7	FB	111 11011	110110 0001	001001 1110
D28.7	FC	111 11100	001110 1110	001110 0001
D29.7	FD	111 11101	101110 0001	010001 1110
D30.7	FE	111 11110	011110 0001	100001 1110
D31.7	FF	111 11111	101011 0001	010100 1110

Valid control code-groups

K Code	Octal value	8-Bit code HGF_EDCBA	10-Bit code RD- abcdei_fghj	10-Bit code RD+ abcdei_fghj
K28.0	1C	8'b000_11100	10'b001111_0100	10'b110000_1011
K28.1	3C	8'b001_11100	10'b001111_1001	10'b110000_0110
K28.2	5C	8'b010_11100	10'b001111_0101	10'b110000_1010
K28.3	7C	8'b011_11100	10'b001111_0011	10'b110000_1100
K28.4	9C	8'b100_11100	10'b001111_0010	10'b110000_1101
K28.5 (1)	BC	8'b101_11100	10'b001111_1010	10'b110000_0101
K28.6	DC	8'b110_11100	10'b001111_0110	10'b110000_1001
K28.7	FC	8'b111_11100	10'b001111_1000	10'b110000_0111
K23.7	F7	8'b111_10111	10'b111010_1000	10'b000101_0111
K27.7	FB	8'b111_11011	10'b110110_1000	10'b001001_0111
K29.7	FD	8'b111_11101	10'b101110_1000	10'b010001_0111
K30.7	FE	8'b111_11110	10'b011110_1000	10'b100001_0111

References

[1] TLK2501 – 1.6 to 2.5 GHz deserializer -Texas Instrument - Revision July 2003 - http://focus.ti.com/lit/ds/symlink/tlk2501.pdf

[2] IEEE 802.3 standard - Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications

[3] ODE muon trigger OL specification – EL Aslanides et al. - draft version – 27 September 2002 – LHCb note in preparation

[4] GOL reference manual – P. Moreira et al. - Version 1.4 - May 2002 - http://proj-gol.web.cern.ch/proj-gol/gol_manual.pdf

[5] StratixGX family data sheet – November 2003 - http://www.altera.com/literature/ds/ds_sgx.pdf