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CRYOGENIC TESTING OF HIGH CURRENT BY-PASS DIODE STACKS FOR THE PROTECTION OF THE SUPERCONDUCTING MAGNETS IN THE LHC

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Abstract

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ABSTRACT

For the protection of the LHC superconducting magnets, about 2100 specially developed by-pass diodes were manufactured by DYNEX SEMICONDUCTOR LTD (Lincoln, GB) and about 1300 of these diodes were mounted into diode stacks and submitted to tests at cryogenic temperatures. To date about 800 dipole diode stacks and about 250 quadrupole diode stacks for the protection of the superconducting lattice dipole and lattice quadrupole magnets have been assembled at OCEM (Bologna,Italy) and successfully tested in liquid helium at ENEA (Frascati, Italy). This report gives an overview of the test results obtained so far. After a short description of the test installations and test procedures, a statistical analysis is presented for test data during diode production as well as for the performance of the diode stacks during testing in liquid helium, including failure rates and degradation of the diodes.

INTRODUCTION

For the protection of the LHC superconducting dipole and quadrupole magnets of the LHC by-pass diodes will be used besides current breakers, dump resistors, and heaters. The by-pass diodes will be installed in the magnet cryostat subjecting them to superfluid helium temperatures and radiation flux. They are high current silicon rectifier diodes connected in parallel to the superconducting magnets thus creating an electrical by-pass in case the magnet quenches. All superconducting lattice magnets will be equipped with by-pass diodes, one by-pass diode across each twin-aperture dipole and by-pass diode across each single quadrupole aperture.

This paper will give an overview of the test results obtained for a large number of series diodes whose design resulted from the testing of numerous prototype and pre-series

FIGURE 1. Dipole diode stack

FIGURE 2. Quadrupole diode stack

diodes [1]. Although the diodes are operated in the LHC in super-fluid helium at 1.9 K, the tests have been carried out in liquid helium at about 4.2 K as the electrical properties of the diode are similar at 1.9 K and at 4.2 K.

The diodes were mounted in adequate stacks as shown in Fig.1 and Fig. 2, mainly consisting of the copper heat sinks to absorb the generated power and the clamping system to keep the diodes under a clamping force of about 40 kN. In each dipole diode stack one diode is mounted so as to by-pass the two lattice dipole apertures whereas one quadrupole diode stack contains two diodes mechanically in series but electrically separated to by-pass each lattice quadrupole aperture.

The mass of the dipole diode stack is about 60 kg and about 50 kg for the quadrupole diode stack. During testing, each diode package must be able to conduct an ultimate current of 13 kA peak with a nominal decay time constant of 120 s for the dipole diode and of about 50 s for the quadrupole diode. In order to avoid the penetration of humidity into the diode capsule, the diodes were not vented during testing. However, just before final installation into the cold mass of the superconducting magnets the metallic rim on two opposite sides of the capsule was cut off. Thus, the possibility can be excluded that, during the long term operation in super-fluid helium, some liquid may become enclosed, creating a potentially explosive overpressure when it vaporises due to the by-pass current during a superconducting magnet quench.

OPERATING AND TEST CONDITIONS

TABLE 1 shows the operation conditions for the by-pass diodes for the superconducting lattice dipole and quadrupole magnets and the test conditions the diodes were submitted to before installation into their cold masses. The irradiation test conditions are the subject of a separate paper at this conference [2].

The temperature difference of about 150 K for the maximum wafer temperature during

TABLE 1: Operating- and test conditions for dipole- and quadrupole by-pass diode stacks

	Dipole diode operating conditions	Dipole diode test conditions	Quadrupole diode operating conditions	Quadrupole diode test conditions
Peak current I_o [kA]	13	13	13	13
Time constant □ [s]	105	120	45	50
Rise time to I_o [s]	0.5	0.5	0.5	0.5
Dumped Energy/diode [MJ]*	1.4	1.7	0.65	0.72
Turn-on voltage range [V]	$1.2 > V_{to} > 10$	$1.2 > V_{to} > 10$	$0.06 > V_{to} > 10$	$0.06 > V_{to} > 10$
Minimum blocking voltage [V]	> 14	> 200	> 1.5	> 200
Maximum wafer temperature [K]	450	~ 300	450	~ 300
Max. electrical contact resistance between diode and heat sink [μΩ]	< 5	< 5	< 5	< 5
Maximum radiation dose during 20 years of operation [Gy]	~ 1000		~ 2700	
Maximum radiation fluence during 20 years of operation [n/cm^2]	~ 2 10^{13}		~ 3 10^{12}	

*The dumped energies are given for a non-irradiated diodes at I_o = 13 kA

testing and in operation will provide a sufficient large enthalpy reserve in case the forward bias voltage increases due to radiation effects [2].

SERIES PRODUCTION OF DIODES

The diode is a unique design specially developed by DYNEX for cryogenic, high-radiation applications. A Junction Termination Extension (JTE) is used to constrict electrical fields during reverse voltage blocking to the silicon bulk. This reduces the reliance of the silicon surface on the passivation interface, which is highly stressed at 1.9 K. To minimise conduction losses, which increase as high levels of radiation reduce carrier lifetime, the diode has a punch-through structure with an n-base of only 6-14 μm. By experimentation Dynex was able to deduce the limits of n-base width to achieve the specification of a minimum 550 V reverse voltage capability and a maximum of 700 V. The large area and thin silicon design provide a high current capability for the 13 kA quench protection application.

These design features were successfully demonstrated in both prototype diodes and the pre-series diodes. The manufacturing challenge was to achieve the necessary process control to meet the narrow n-base with high production yields for 2100 diodes.

The 170 μm N+ junction, 48 μm P+ junction and the 230μm thickness of the silicon have combined processing tolerances of the order of the required n-base. Production data collected from each batch is shown in Figure 3, together with design and development sample data showing the relationship between n-base width and reverse voltage. Excellent process control resulted in only 2% of diffused wafer batches being rejected for out-of-range n-base widths.

For the specified high current forward voltage (V_f) measurements to currents of 14 kA and pulse width 200 μs, Dynex constructed a purpose designed equipment. The test yield achieved on this was 98.5 %. In addition the DC avalanche test resulted in a rejection rate of only 0.5 % below 550 V, and 0.1 % greater than the agreed 700 V upper limit, demonstrating the effect of the close control of n-base width. Other manufacturing yields

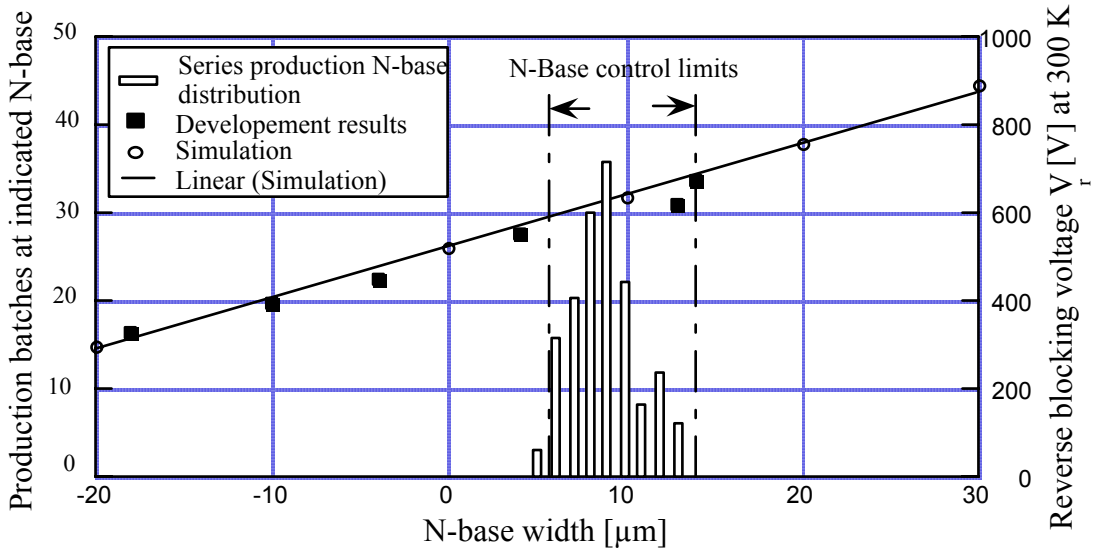

FIGURE 3. Graph of design reverse voltage vs N-base width, along with production batch distribution.

were typical of classical power semiconductor diodes.

TEST PROCEDURE AND TEST FACILITY

The cryogenic tests consist of measurements of the forward- and reverse bias voltage characteristics at 77 K and at 300 K and of endurance test cycles at liquid helium temperature [3].

The forward voltage diode characteristic is measured by submitting the diode to short semi-sinusoidal current pulses (of about 200 µs) at increasing current levels from 500 A to 14 kA as already described earlier in detail.

The measurements of the reverse voltage characteristic are carried out at 300 K, 77 K and also at liquid helium temperature. The maximum reverse breakdown voltage V_{rmax}, is defined as the highest value of anode-cathode voltage in reverse bias before reaching the upper reverse current limit $I_{rmax} = 1mA$.

The main experimental facility is devoted to the endurance test cycles. Each diode stack is submitted to 10 current pulses. During each pulse the current is linearly raised to about 13 kA within 0.5 s and then decaying exponentially with $\tau = 50$ s for quadrupole diode stacks and with $\tau = 120$ s for dipole stacks, according to the diode operating conditions in case of magnet quench in the LHC. During each endurance cycle the anode-cathode voltage, the temperature of the copper heat sinks and the contact resistance between anode-heat sink and cathode-heat sink are measured.

Finally, the maximum wafer temperature and its variation during the endurance cycle is deduced by means of an algorithm based on the relationship between forward voltage at constant current and temperature in the range between about 70 K and 350 K, thus using the diode itself as a temperature sensor [1].

In order to test at least 10 diode stacks per week, three cryostats - each of them housing four quadrupole or four dipole diode stacks electrically connected in series - are used, allowing the cool-down, testing and warm up of 12 stacks in parallel.

For the measurement of diodes forward voltage characteristics at 300 K and 77 K under adiabatic conditions, a fast current pulse generator furnishes the short semi-sinusoidal current pulses up to about 14 kA peak and 200 µs pulse length [3].

An accurate d.c. power converter of low output voltage ripple, rated at 14 kA and 16V, is devoted to the endurance cycles test [3]. The d.c. output can be connected to one of the three current outlets by a motor-driven switch with three positions, connecting the power supply to the selected cryostat.

As the turn-on voltage of one diode amounts up to about 7 V at liquid helium temperature, resulting in a turn-on voltage of about 56 V for four quadrupole diode stacks with 8 diodes electrically in series, and the main power converter can supply only 16 V, a commercial 100 A/100 V d.c. power supply is used for the turn-on of the diodes. This turn on power supply is connected in parallel to the endurance power supply via adequate de-coupling diodes.

TEST RESULTS

Forward bias characteristics of series diodes

The turn-on voltage of the series diodes is measured at 4.2 K before each endurance current pulse with a sampling rate of 10 ms of the data acquisition system, resulting usually in lower average and minimum turn-on voltages compared to measurements with a sampling rate of 0.5 ms as it was carried out on several series diode samples at 1.8 K and at 4.2 K at CERN. With a sampling rate of 10 ms of the data acquisition system, the real turn-on voltage cannot always be detected as the fast voltage peak is too short. The turn-on voltage measured at 1.9 K is only insignificantly higher than at 4.2 K as shown in TABLE 2.

TABLE 2. Turn-on voltages measured at 1.9 K and at 4.2 K with different sampling rates

	Series diodes at 4.2 K and with 10 ms sampling rate	Sample diodes at 4.2 K with 0.5 ms sampling rate	Sample diodes at 1.9 K with 0.5 ms sampling rate
V_{tomin} [V]	2.7	5.5	5.6
V_{tomax} [V]	6.2	6.3	6.5
$V_{to\text{-}aver.}$ [V]	4.2	5.7	6.1

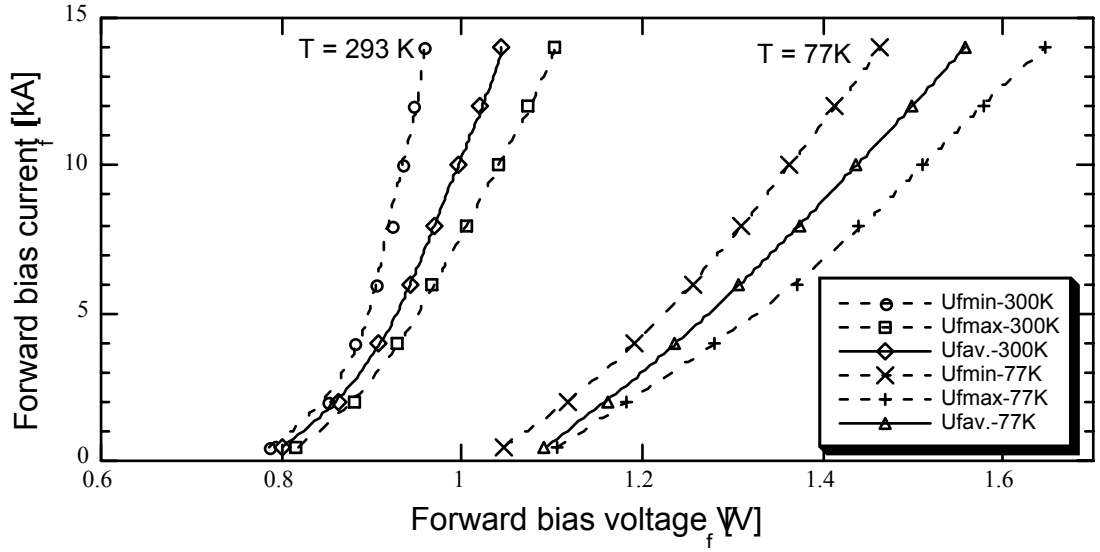

FIGURE 4. Measured forward voltage characteristics $I_f = f(V_f)$ of series diodes at 293 K and at 77 K. The dotted curves show the minimum and maximum values.

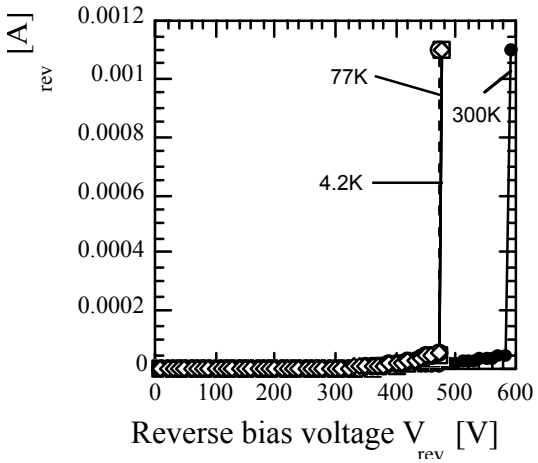

FIGURE 5. Typical reverse bias voltage characteristics measured at 4.2 K, 77 K, and at about 300 K.

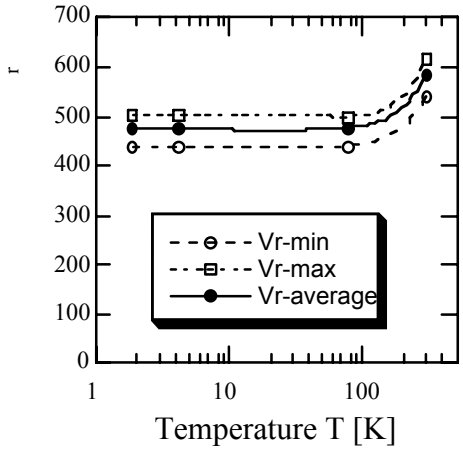

FIGURE 6. Measured reverse bias voltage Vr versus temperature with I_{tmax} = 1 mA

The forward bias characteristics of the series diodes have been measured at about 300 K and at 77 K before and after the endurance testing, as shown in Figure 4, with a short pulse generator under quasi-adiabatic conditions. The temperature in the diode wafer increased by about 2 K at 77 K and I_f = 14 kA due to self-heating, whereas at 300 K the self-heating is negligibly small.

Reverse bias characteristics of series diodes

The reverse voltage was measured on all diode stacks at 4.2 K before the endurance test, after the fifth run, and after the last run, at 1.8 K in sampling mode only on some stacks.

As shown in Figure 5 and Figure 6 the reverse voltage at liquid helium temperatures is almost the same as at 77 K. It is sufficient to measure the reverse voltage at 77 K to know the reverse voltage at liquid helium temperatures.

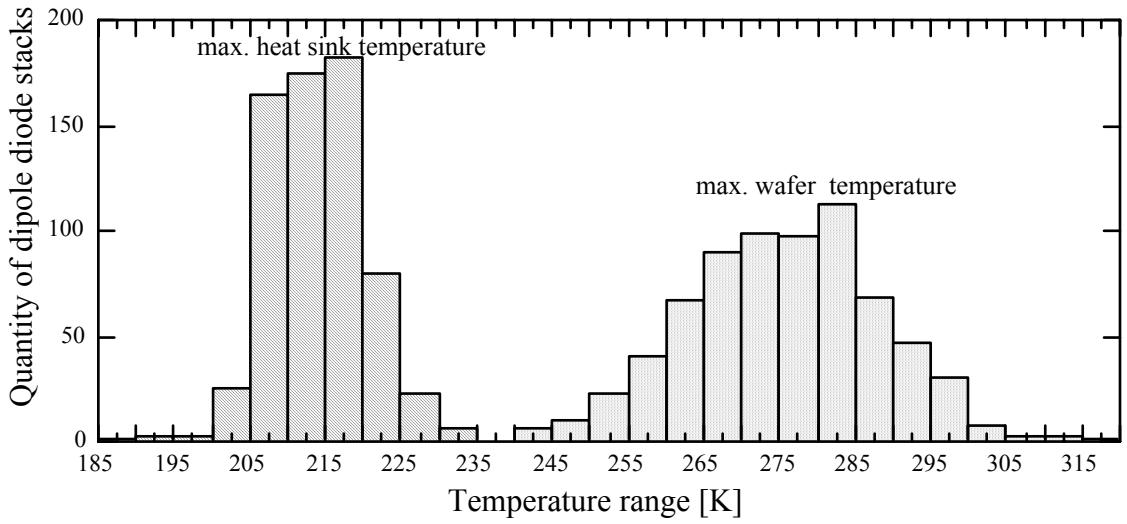

FIGURE 7. Histogram of the measured maximum wafer- and heat sink temperature for dipole diode Stacks

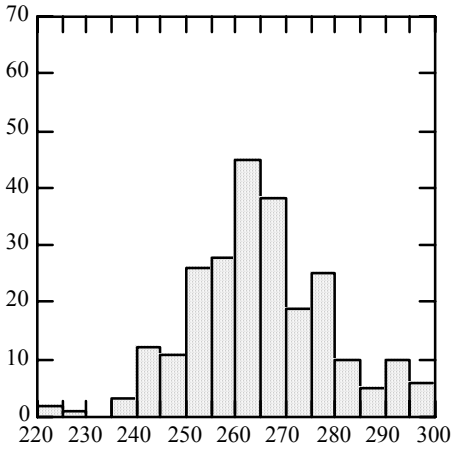

FIGURE 8. Histogram for the maximum wafer temperature of the lower diodes in the quadrupole diode stacks.

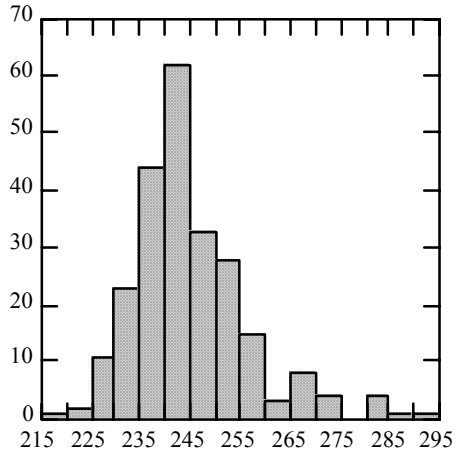

FIGURE 9. Histogram for the maximum wafer temperature of the upper diodes in the quadrupole diode stacks

Endurance test results for dipole diode stacks

As shown in Figure 7, the maximum wafer temperature for the dipole diode stacks amounts to about 280 K in average and the maximum heat sink temperature to about 215 K in average. The maximum wafer temperature occurs about 30 s after the initial current rise, the maximum heat sink temperature at the end of the endurance current pulse.

The very few diode stacks, exceeding the specified maximum wafer temperature limit of 300 K, were either dismounted and re-assembled again or the diode was changed.

Endurance test results for quadrupole diode stacks

Due to the lower dumped energy, the average wafer temperature of the quadrupole diode stacks is about 20 K lower for the upper diode and about 40 K lower for the bottom

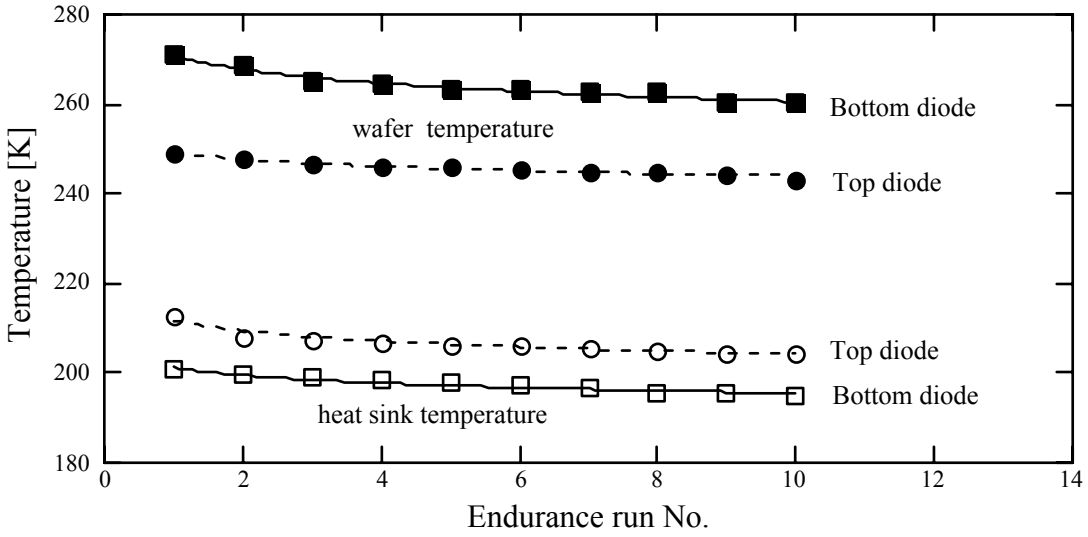

FIGURE 10. Average wafer and heat sink temperatures versus endurance run No. for quadrupole diode stacks.

diode compared with the dipole diode stacks as shown in Figure 8 and Figure 9.

The lower wafer temperature of the upper diode in Figure 10 can be explained by the heat exchange with the evaporating helium at the beginning of the endurance run. The higher temperature for the heat sinks of the top diode, at the end of each endurance pulse, is mainly due to the heat leaking in through the current leads which are no longer cooled.

A training effect, mainly a decrease of temperature with the number of current pulses, has been observed during the ten endurance current pulses as shown in Figure 9. It can be explained by the settling (reduction) of thermal contact resistances during the thermal cycling. Similar results have been obtained also for the dipole diode stacks.

FAILURES

The majority of failures (21) were observed during the measurements of the reverse bias voltage V_r. The measured reverse bias voltage V_r at reverse bias current I_r = 1 mA was below the specified lower limit of 200 V. The failed units were returned to Dynex for failure analysis. The failures were found to be caused by thick regions of polyimide passivation on the edge of the diode wafer which cracked during cool down and thermal cycling. This degradation occurred on a small series of diodes only. Dynex implemented a modification to its operator instructions to decrease the thickness of polyimide and correct the problem for subsequent batches.

A small quantity of diode stacks (22) had to be refused because the measured electrical contact resistances between the diode and the Ni-plated Copper heat sinks exceeded the specified upper limit of 5 μΩ. After dismounting, cleaning, and remounting of the diode stack, significantly lower contact resistances were measured.

On a very few diodes (3) the forward bias characteristic changed during the endurance testing towards high forward voltages and the upper limit of the specified maximum wafer temperature was exceeded. The diodes were dismounted and replaced by new diodes.

CONCLUSIONS

Up to now about 800 dipole diode stacks and about 250 quadrupole diode stacks have been successfully assembled. Into these diode stacks about 1300 of the 2100 diodes have been mounted and successfully tested. The production of the diodes is finished and all diodes are supplied to the stack manufacturer OCEM.

The routine testing of diode stacks continues smoothly without major problems at ENEA. The test results, obtained so far, meet the requirements of the Technical Specification for the testing of the diode stacks. The supply of tested stacks to CERN is well within the schedule.

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