The Front-End Electronics for LHCb calorimeters

C.Beigbeder, R.Bernier, D.Breton, T.Cacéres,
P.Cros, A. Hrisoho, V. Tocut, K. Truong

Laboratoire de l'Accélérateur Linéaire
BP 34 – 91898 Orsay Cedex - France

1. ABSTRACT

The electronics for the electromagnetic and hadronic calorimeters of LHCb is under design. The 32 channel front-end board offers the complete front-end and readout electronics for every channel including original shaping, 12bit-40MHz ADC, digital filtering and latency for level 0 and level 1 triggers. The clipped PM input signal is integrated within 25ns, but also delayed then subtracted to itself 25ns later what allows performant pile up independence. This board also includes the first processing levels of the L0 calorimeter trigger.

A 16 channel prototype board has been designed and used at CERN in test beam last summer.

2. INTRODUCTION

The electromagnetic and hadronic calorimeters currently designed for LHCb are lead-scintillator sandwiches employing the "Shashlick" technology. The output of the plastic fibers is equipped with phototubes. The readout system will have to deal with 6000 channels for the Ecal and 1500 for the Hcal.

3. REQUIREMENTS

The main requirement for LHCb electronics is the pile-up rejection. Indeed the residue of a previous signal on the current sample has to be less than 1% after 25ns. This implies to work both on the PM signal and on the shaping. Shaped data has to be sampled at 40MHz on 12 bits then to undergo pedestal subtraction for rejecting LF noise and to be transcoded within LUTs into energy over 8 bits for trigger data and 12 bits for readout data. The latter has to be buffered during the L0 latency, to be derandomized and then rebuffered for the level 1 latency. After the level 1 trigger, an extended zero suppression has to be performed before sending the formatted event to the DAQ.

There are also trigger elements sitting in the front-end crate. The first stages concern the seek for local maxima inside groups of 512 channels, with a validation by the Preshower and Pad Chamber data.

4. FRONT-END OVERVIEW

Fig 1 describes the Front-End crate and its main interconnections. The PM side elements are connected to the Front-End board through 10 meters of coaxial cables. There are 16 FEBs in the crate, each receiving 32 signals. The output of these boards are connected to the custom backplane, sending signals using LVDS levels to the Event Filter. This board is in charge of performing the advanced zero suppression and the event formatting after level 1. Data is then sent to the DAQ through optical links. The Crate Controller is in charge of driving the serial link which is used for loading the hardware and of distributing the TTC signals. At last, the Trigger Validation Board receives the local maxima coming out from the FEB, then validates it with the Pad Chamber and Preshower information and finally searches for the residual maxima over the two half crates. The resulting words are sent to the Trigger Main Selection crate through optical links.

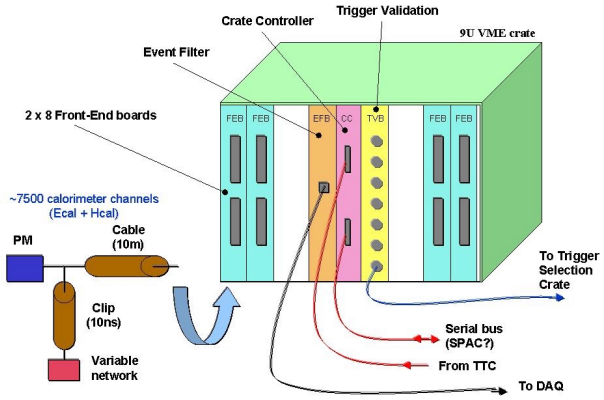

Fig 1 : overview of the Front-End Crate

5. THE FRONT-END BOARD

Fig 2 shows the block diagram of the 32 channel Front-End board. This is a 9U board using VME mechanics but deserting the VME bus. This one will be replaced by a serial bus which has still to be defined.

Let's follow the main data path inside the board. It starts with the four 8-channel coaxial input connectors. Then signals goes into the PM and cable compensation before entering the analog chip. After a 12bit ADC conversion, data undergoes a pedestal subtraction with the smallest of the two previous samples. This subtraction is intended to reduce the high bandwidth noise of the integrator, and the two samples are used not to degrade the pile-up rejection. Then data is converted into energy

within two LUTs, one for the trigger which outputs 8 bit words, the other for the readout data which outputs 12 bit words in a pseudo floating format. The latter data is then sent to the L0 latency pipeline, L0 derandomizer and L1 latency buffer. After L1 trigger, it is sent across the backplane using LVDS levels towards the Event Formatter.

At the right top of the board, trigger data is first added in squares of 4 cells while preserving the original granularity, then filtered looking for the local maximum on the board. The latter is sent with its address (total of 13 bits) using LVDS levels towards the Trigger Validation Board.

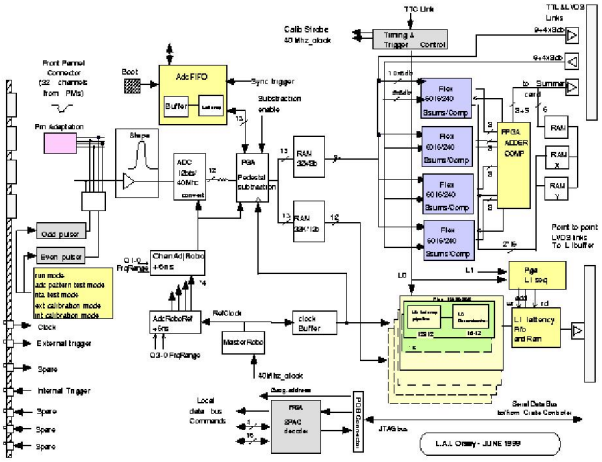

Fig 2 : block diagram of the Front-End board

Beside those data paths, some utility functions have been implemented. One can adjust the sampling time of every ADC on the board thanks to programmable delay chips with a precision of 1 ns. A functionnal analog calibration has also been implemented to allow checking of the complete readout chain. This has already been useful during the test beam operations.

6. THE FRONT-END ELEMENTS

The purpose of those elements is to shape the PM pulses in less than 25ns to avoid electronics pile-up. The specifications on both extremities are the following :

- At the input : the PM maximum current is 20mA over 25 ohms.
- At the output : the ADC input dynamic range is 1V under 250 ohms.
- The residue after 25 ns has to be smaller than 1%.
- The sampling area should cover +- 3ns with a 1% precision.
- The RMS noise has to be < 1 ADC count (250uV).
- The deterioration of the statistic fluctuation due to the apparatus has to stay under a factor 2.

To fulfil the above requirements, two problems will have to be solved. The first one concerns the PM signal. If one looks at Fig 3, the PM output current has a fast rise time but a slow decay that goes over at least the two consecutive samples at 40 MHz. It thus needs to be pulled to zero after 10ns to ensure the zero pile-up requirement. The remaining area is on the order of 60% of the original one.

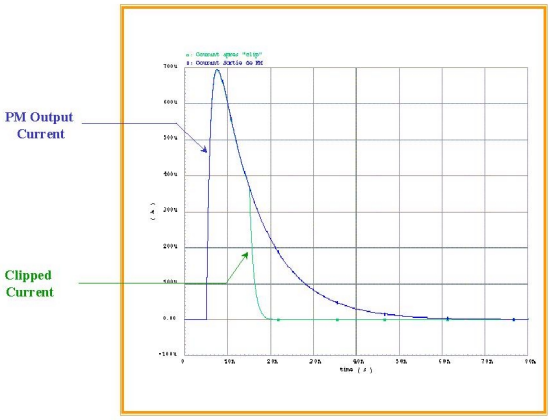

Fig 3 : PM output pulse

To realize this cut on the signal, the clipping circuit on the left of Fig 4 will be used. It consists in a short 1 meter cable located at the output of the PM base. It derivates the signal towards a variable network which will send back a inverted part of the signal. As both the source and reflected signals are negative exponentials, their superposition leads to zero. The demonstration is given on the top plot of Fig 5.

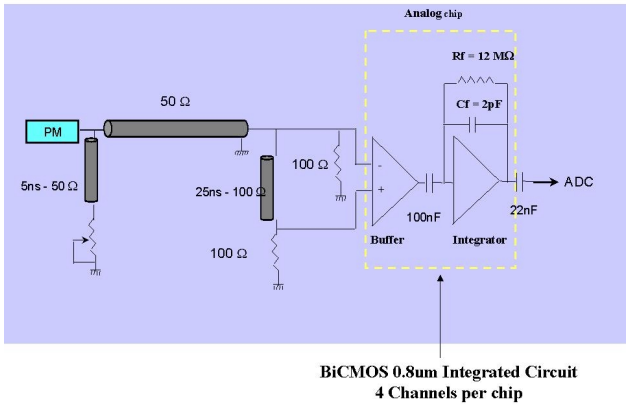

Fig 4 : Front-End Electronics

Now that the input signal has been shaped, we have to measure the energy deposited in the calorimeter. The corresponding information is the area of the PM signal. The best way to measure it without deteriorating too much the statistic fluctuation is to integrate this signal in a capacitor (Cf). The induced difficulty becomes to empty this capacitor. Two ways are possible :

- Use a switch mounted in parallel but this system induces a dead time when the capacitor is being emptied, what implies the use of two integrators in parallel and a multiplexor.

- Subtract in a linear way the signal to itself thanks to a specific configuration.

The latter is the chosen solution. The configuration appears in the middle of Fig 4. The input signal of the analog chip is derivated, delayed by 25ns, then subtracted to itself thanks to the differential buffer. The latter has also in charge the division of the input current to adapt it to the small value of Cf which ensures a fast rise time to the integrator.

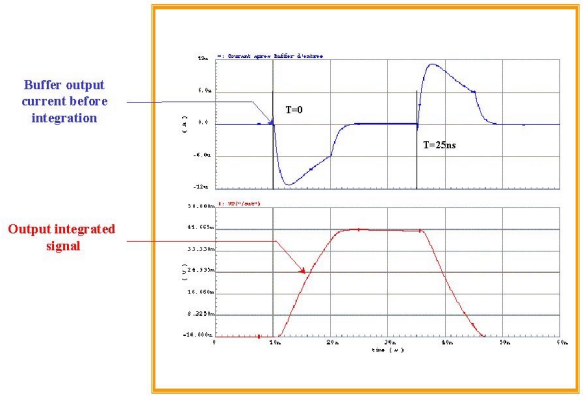

Fig 5 : simulated input and output pulses of the integrator

Between the buffer and the integrator, there is an external AC coupling that allows to separate the DC levels. The small value of Cf allows to load it fast and to offer a nice plateau at the top of the signal (see bottom plot of Fig 5).

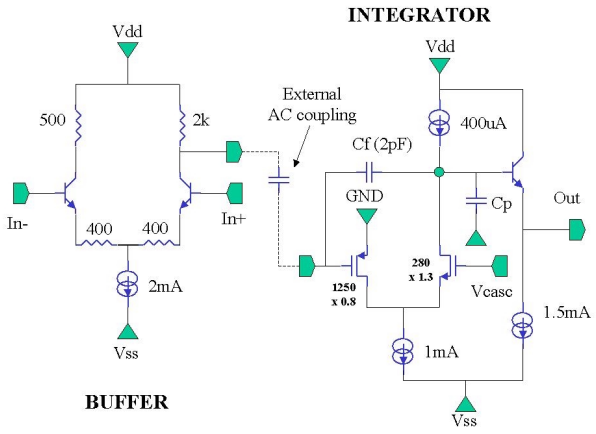

Fig 6 : schematics of the analog chip.

Fig 6 shows the schematics of the analog chip. The 2K resistor at the output of the buffer is used for replacing a 1mA current source that would produce an offset current and more noise with the same power supplies than the resistor. Obviously, the buffer has a current output as the input impedance of the integrator is small (200 ohms) compared to the 2K of the resistor.

The integrator schematics is based on a cascode amplifier. Its open loop gain is high (60dB), it's fast as there is no Miller effect on the input PMOS, and it produces very low noise. On the other hand, there is a need for an emitter follower at the output not to degrade the gain by the charge impedance. In our case, as the charge is only 350 ohms, another follower has been mounted on the board using discrete elements. The decay time of the integrator is linked to the 2K resistor what leads to a value of 6us.

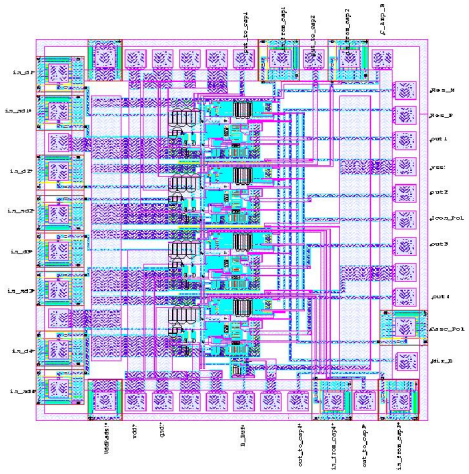

Fig 7 : layout of the analog chip

Fig 7 shows the layout of the current version of the analog chip. Up to now, three versions have been submitted in only 6 months. This is due to the pression of the test beam of last summer. The main difficulty that appeared was a resistor in the gate access to the input PMOS of the integrator. This was due to a bad polysilicon design and introduced noise and instability in the chip response. This problem was fixed and the chips received two days before the test beam were fully operationnal. When mounted on test bench at LAL, the chip offered the results shown in Fig 8.

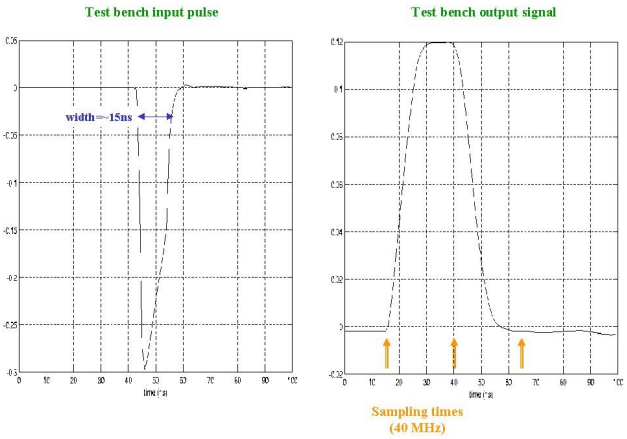

Fig 8 : real signals on test bench

On this plot, the input pulse derives from a generator and is clipped as the real PM signal. The output signal shows a nice flat top in concordance with the simulations. The global preliminary results from this test bench are given in Fig 9.

Simulation Results :			Current Test Bench Results :
Dynamic Range :	1.4V	<=>	1.4V
Non Linearity :	0.5%	<=>	to be measured
Residue after 25 ns :	<0.5%	<=>	<1% (undershoot ~3%)
RMS Noise after subtraction	1 ADC Channel (ie 250uV)	<=>	1.2 ADC Channels (ie 300uV)
Power Consumption :	40mW / Channel	<=>	38mW / Channel
Open-Loop Gain :	~60dB	<=>	~60dB
gm (Input PMOS) = 34mA / V			gm (Input PMOS) = 18mA / V
Fall Time :	6us	<=>	6us
Rise Time (?) :	1.2ns	<=>	5.5ns
Input Impedance (?) :	90Ω	<=>	240Ω
Deterioration of statistic fluctuation	< 2	<=>	< 1.2

Fig 9 : first results from the test bench

These results show a good adequation between simulation and real circuit, except for the gm of the input transistor. This is due to simulation models and also explains the mismatches in the rise time and the input impedance of the integrator.

7. THE PROTOTYPE FRONT-END BOARD

The prototype FEB shown on Fig 10 is a 16 channel board which has been designed targeting the test beam of last summer. It comprises the same readout chain excepting the L1 buffer. Moreover, some extra functionnalities as the spying of the raw data at the output of the ADCs have been implemented. This allows to crosscheck offline the subtracted data with their source.

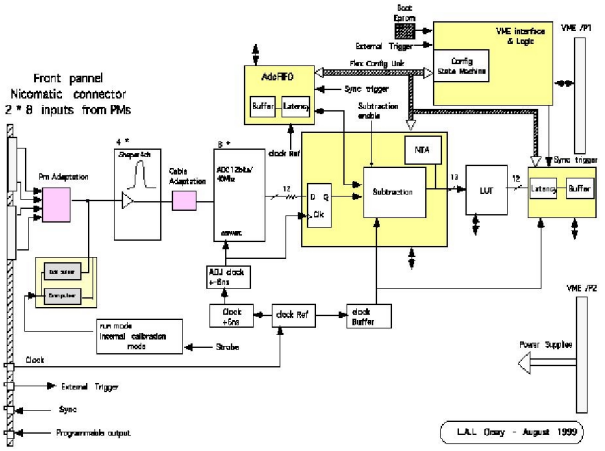

Fig 10 : prototype of the Front-End board

Another interesting purpose of this board is the configuration state machine implemented in the VME interface Altera. It allows to configure all the other FPGAs on the board in an interactive way, permitting to debug the board easily (even far from home through ftp) and also to modify the functionnality of the FPGAs for test purposes.

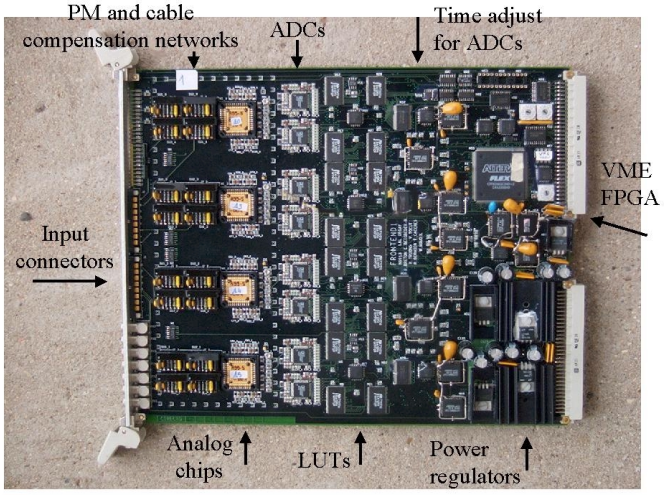

Fig 11 : top layer of the prototype FEB

Fig 11 offers a picture of the board. On the left side, one can see the 2 x 8 channel input connectors, followed by the PM and cable compensation networks and the delay lines. The four 4 channel analog chips are followed by half the ADCs and the LUTs. All the big FPGAs (10K50 and 6K16) are on the other side of the board, together with the other half of the ADCs.

8. THE TEST BEAM ENVIRONMENT

This board was installed on test beam in the setup shown in Fig 12.

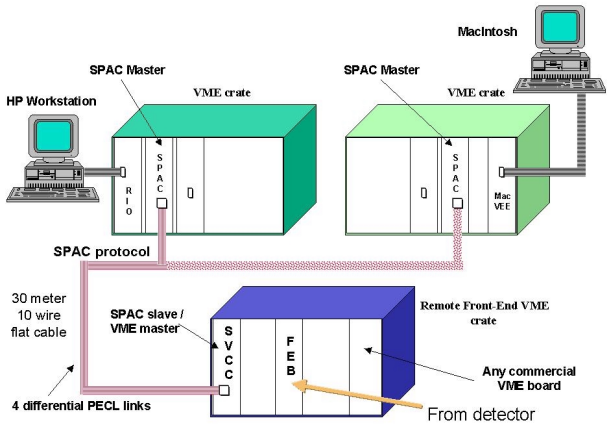

Fig 12 : test beam setup at CERN

One can remark here that two VME master crates can be connected to the remote electronics. This is intended for debugging and monitoring purposes. Indeed, when electronics is installed at CERN for test beam, local DAQ still needs to be debugged. The MacIntosh interactive test software, which also provides data acquisition, and the possibilities of live insertion of the SPAC bus thus allow to start the debugging phase of the hardware while permitting crosscheck of the readout data with the one read by the standard DAQ. This is then a very efficient way of setting up the system in a very short time.

9. TEST BEAM RESULTS

The first measurements made on test beam were related to the signal coming from the PMs. It is plotted on top of Fig 13.

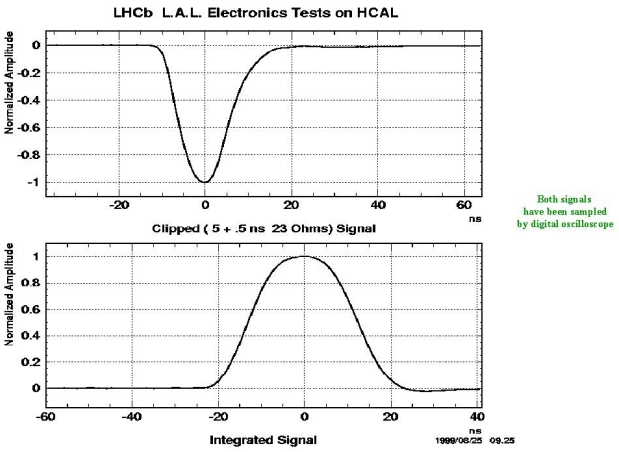

Fig 13 : real signals on test beam

One can remark that the width of the signal is much larger than on test bench. This was due to some problems with the quality of the fiber inside the Shashlick and of the microcoaxial cable. Nevertheless, the shape at the output of the integrator (bottom plot) looks quite good with a large top where sampling can be clean.

The following step was to compare the new 40MHz electronics with the "old" LeCroy one. Data was thus taken on the same channel through the two different paths. The comparison is plotted on Fig 14.

On this plot, one can compare 2 different readout channels for the same PM.

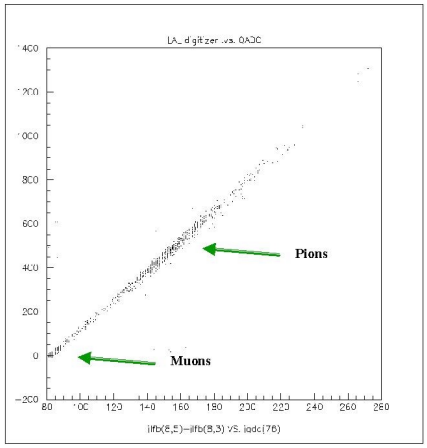

Fig 14 : new electronics vs LeCroy ADCs

The straight line proved the good level of functionnality of the new electronics and data was then taken with the latter.

Fig 15 presents the results of an ECal run. 6 samples are plotted successively. The signal is centered on the sample 5 (third one). On the sample 3, one can observe the noise distribution. This corresponds to a RMS of 2.5 ADCC. The sample 4 shows that the signal is wider than on the Fig 13 as there is already some data 25ns before the peak. This was due to some problems with the PM used at this occasion.

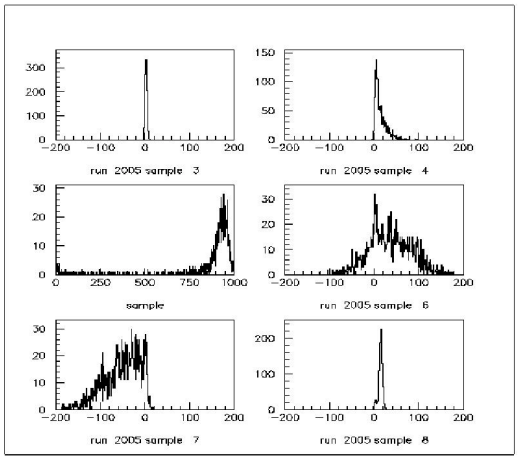

Fig 15 : 6 samples from an Ecal run

On the samples 6 and 7 appears the result from the subtraction of the smallest of the two previous samples. On sample 8, we're back to the baseline.

10. NEXT STEPS OF THE DEVELOPMENT

The previous measurements made on test beam prove the consistency of the electronics which has been designed. We are currently concentrating on the various noise sources to reduce the total noise on the board under 1.5 ADCC.

The next steps of the developments for this electronics are the following :

- Concerning the Front_end Board :
  - A new version of the analog chip including a second emitter follower by early 2000
  - Implementation of the trigger part of the board
  - Study of the L1 buffering hardware
  - Extension to a 9U/32 channel board
- Study of the fast backplane using LVDS signals
- Study of the Event Filter (which provides advanced zero suppression and event formatting)
- Study of the Crate Controller (which includes serial access bus and TTC)
- Study of the Trigger Validation Board (which prepares the candidates for the L0 trigger Main Selection Crate)

11. REFERENCES

For completing the information given in this paper, one could have a fruitful look to the following notes :

- J.Christiansen, "Requirements to the L0 front-end electronics", LHCb technical note, July 30th 1999
- C.Beigbeder et al., "A Joint Proposal for the Level 0 Calorimetric Triggers", LHCb 99-017, June 7th 1999
- D.Breton et al., "SPAC : Serial Protocol for the Atlas Calorimeter ", www.lal.in2p3.fr/technique/se/spac