Status report on the Alice prototype TPC with Ring-Cathode Readout

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Abstract

As part of the ALICE R&D project a small prototype TPC has been built and tested using Pb-Pb interactions at the SPS. It incorporates a novel readout using C-shaped cathodes for better coupling to the sense wires. Newly developed 4-channel preamp/shaper dice are mounted directly to the readout board using a new technique (tape-automated bonding, TAB). Direct digitisation by commercial low power ADCs with subsequent zero suppression implemented into a field programmable gate array (FPGA) has been tested with the aim to incorporate this functionality into a single ASIC thus allowing later on-detector installation. For the transfer of the data a newly developed full duplex optical data link was used.

Details of the detector design, construction and readout are presented together with results from bench and beam tests.

Contents

1 Introduction

The Heavy Ion Experiment Alice at the LHC will have to cope with unprecedentedly high particle fluxes. Charged particle rapidity densities of up to 8000 have been predicted at midrapidity.

The main tracking detector of ALICE will be a TPC. Improvements in the design of the readout modules and electronics are mandatory to achieve the requested double track resolution and particle identification by dE/dx measurement as well as longterm stability under those conditions.

In 1992 the research project RD-32 was started at CERN [1] to investigate low diffusion gas mixtures, novel designs for readout chambers and analog frontend electronics and explore new techniques for high volume data readout and data reduction. One of the results of these investigations was the development of a readout scheme for wire chambers incorporating ring shaped cathode elements. Due to the better coupling of the charge signal to the readout the signals observed are larger by about a factor four compared to the classical TPC readout. A new 4-channel preamplifier/shaper in bipolar technology optimized for low power consumption and high baseline stability completed this development.

In the course of further studies it was demonstrated on small prototypes that the original concept using small closed rings could be replaced by open C-shaped structures making it easier to insert the sense wire plane without loosing the advantages of the ring design. In addition a scheme could be developed to produce a sufficient amount of rings to equip a reasonably large prototype.

In 1996 work started to incorporate the new developments into a fully operational detector prototype and test it under realistic conditions.
The main goals of this project were:

- Proof of the capabilities of the new design under experimental conditions allowing chamber operation at lower gas gains thus ensuring better stability of operation at high currents
- Demonstrate the baseline stability of the new preamp/shaper and gain experience with the new bonding technique (TAB) where the dice are mounted directly to the readout board
- Development of a new gating scheme avoiding the traditional wire planes and thus reduce chamber weight
- Explore the possibilities of industrial methods to reduce cost for serial production

An agreement was reached with NA49 to set up the detector in front of the Main TPCs of NA49 with the Lead beam passing through the detector. Part of the phase space not covered by NA49 would become accessible. The prototype could thus contribute to the physics output of NA49. As a consequence the readout of the prototype had to be matched to NA49 requirements.

In the following details of the design, all steps of the production and results of bench tests as well as results of the Lead beam test will be shown.

2 The Ring-Cathode Chamber

In figure 1 a schematic cross section through the ring-cathode chamber (RCC) is shown.

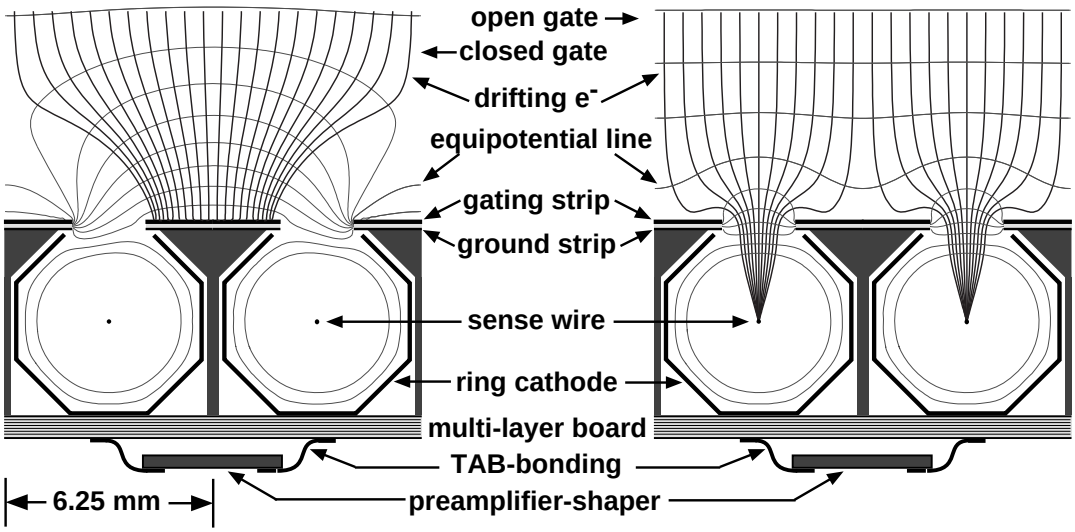


Figure 1: Schematic cross section of the readout board with ring cathode elements and preamp/shaper chips. In addition equipotential lines and drift lines for electrons are shown. Left part: gate closed, right part: gate open.

The ring elements are positioned on a multilayer board. Four rings are coupled electrically to one preamp/shaper channel which is bonded directly to the backside of the board. Conducting strips are inserted between the open sides of the rings. Variation of their potential allows to separate the amplification region from the drift region and thus provide the same function as a gating grid.

2.1 Cathode Rings

The cathode rings for the ALICE TPC prototype consist of 80 μm copper foil bent into the shape of seven sides of an octagon with 6mm diameter at the inner corners and a width of 2.65mm (fig. 2). 51 cathode rings are held together at a distance of 0.5mm by 1x0.1mm Vetronite strips glued to the 3rd and 5th side of the octagons, thus forming a ring cathode element of 137.2mm length (fig. 3). The 51 copper foils are initially held together by frames of the same foil which come in sets of five such units from the etching process.

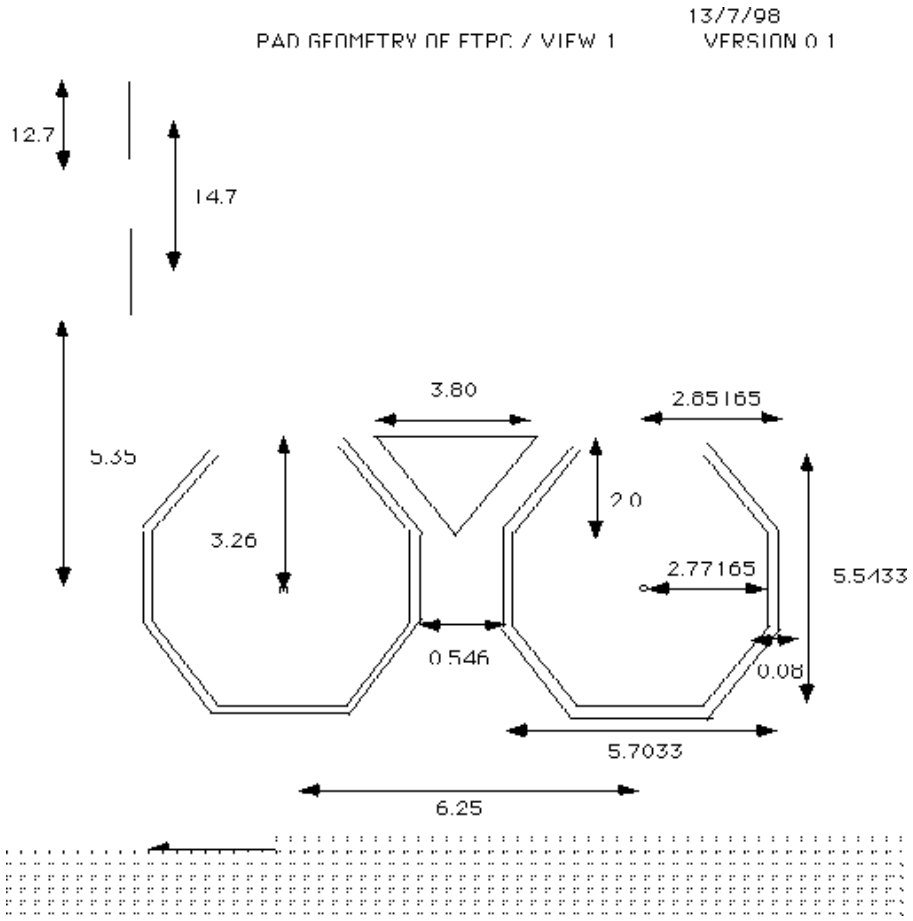


Figure 2: Actual dimensions of the ring-cathode elements.

2.1.1 Production

In a first step, cathode element frames are selected and cut from the original five-unit-sets. In the preparation for the strip glueing, two Vetronite strips are placed in the corresponding grooves of a glueing tool and held down by magnetic clamps at both ends. The foil positioning pins are placed in their holes in the glueing tool, and rapid Araldit is mixed on paper stretched over a flat aluminum plate. After the preparation of a homogeneous layer of 0.1x50x200mm of glue (with the the help of a glue spreading tool) a precision comb is used to transfer a well defined quantity of glue on 51 precisely defined positions on each Vetronite strip. The foil is then lowered on the positioning pins, the strip position is corrected if necessary and brass weights are placed on top of the foil to apply some force during the hardening of the glue. Subsequently the comb and the glue spreader are cleaned with alcohol and paper. When the remaining glue on the paper has hardened sufficiently, the weights and the positioning pins are removed and the foil with the Vetronite strips is put aside.

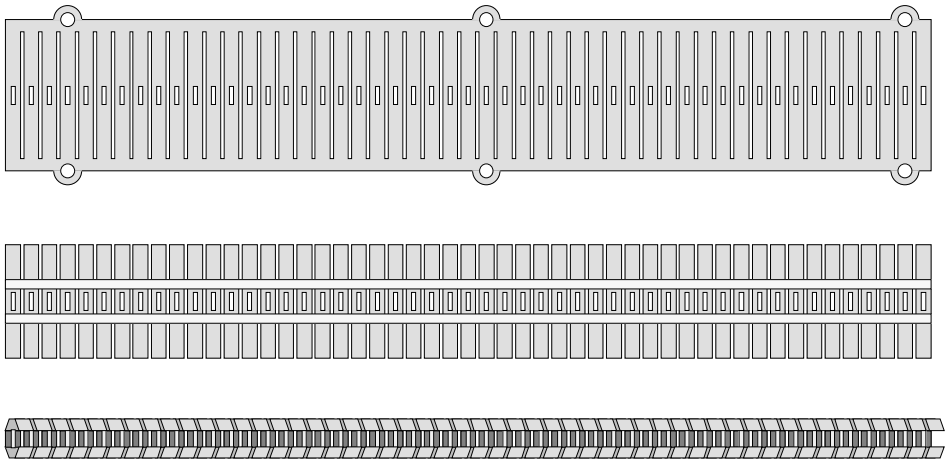


Figure 3: Ring-cathode elements before glueing of the Vetronite strips (top), after glueing and cutting (center), and after bending (bottom).

One day after the glueing process, when the Araldit has hardened out completely, the excess Vetronite is removed with a side cutter, and the edges of the copper foil are cut off with the help of a precision cutting tool. Then the elements are placed in the bending tool and pressed against an octagonal template. After verification of the bending uniformity by eye the completed cathode elements are stored for subsequent positioning on the chamber boards.

2.1.2 Time Budget

On average, a net working time of 10 minutes per ring-cathode element is required for the production process described above, i.e. 2 min selection, cutting, and handling, 2 min bending, and 6 min glueing. The glueing process is done for two elements in parallel and can be performed every 20 minutes, 12 of which are needed for preparation, glueing and cleaning. The remaining 8 minutes can be used for the other steps of the production process as well as for short breaks. With the described procedure, a total production rate of 50 pad elements per day (of 51 cathode rings each) can be achieved conveniently by one person.

2.1.3 Mounting on the Readout Board

A readout module of the ALICE TPC prototype carries 18x148=2664 cathode rings. 2x18 cathode elements with 51 pads and 18 elements with 46 pads are glued sequentially to the readout board. A precision comb similar to that used for the cathode element production is used to transfer a well defined quantity of Araldit to the PCB. A positioning tool allows to place and hold the cathode element accurately with respect to the copper footprint on the board during the glue curing (about 15 min). After completion of a readout board, the location of the cathode pads with respect to the footprint is controlled with a measuring microscope. A summary of the measurements of the precision of the mounting can be found in [2]. Finally, each pad is contacted to the footprint with a drop of conductive glue which is applied by hand using a piece of wire. The contacting takes two hours per readout board.

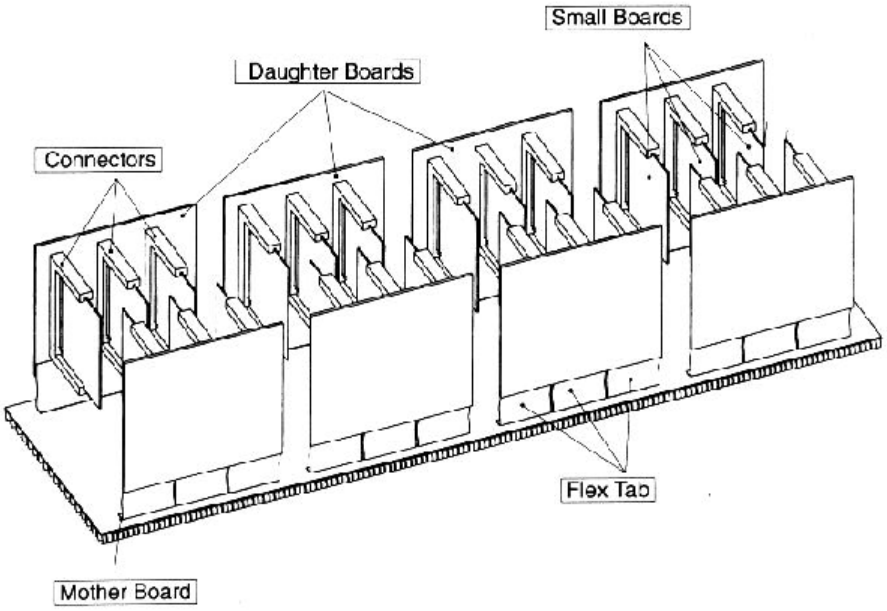


Figure 4: Perspective view of multi-layer board with attached flex TAB , daughter boards, connectors and small boards.

2.2 Gating Structure

The RCC prototype was constructed with the aim of using the minimum number of wire planes . Therefore no gate wire-plane but gating strips were used to gate the RCC prototype. The gate-strips are positioned between ring elements and consist of Cu-Vetronite sandwich (see also fig. 43) With this architecture the mechanical forces on the readout body are minimized compared to the traditional wire planes which need a mechanical reinforcement in the order of 1200 N/m**2 for a wire plane with a 1 mm wire pitch.

In the gate-opened position all strips are on a common voltage (offset voltage). With this negative offset voltage the electrons are forced to enter the amplification wires. To close the gate odd and even strips (neighbouring strips) are set to positive resp. negative voltages relative to the offset voltage (δV or bias voltage). In this dipole field the electrons are attracted by the positive strip and do not anymore reach the amplification wires. The positive ions that move back from the sense wires and pass through the opening of the ring are as well attracted by the gating elements. In the experiment the switching time has to be as small as possible. In general the drift velocity multiplied with the switching time determines the information loss of the TPC. The switching of the voltages does unfortunately introduce a ringing on the preamps. This ringing increases with δV (bias voltage) and can only be minimized by introducing an additional ground layer to increase the decoupling of the gating structure from the preamps.

2.3 Multilayer Board

The multilayer board (MB) was designed as a gas tight and flat mechanical support structure for the pad elements. Furthermore the preamp/shapers were bonded directly on the backside of the MB and all distribution of low voltages are done within the different layers (comp. Fig. 13) and the connection to the following stages is provided (comp. Fig. 4).

Before final assembly several test boards have been produced to control the mechanical tolerances and check for gas leaks. Since the gas tightness was one of the most crucial

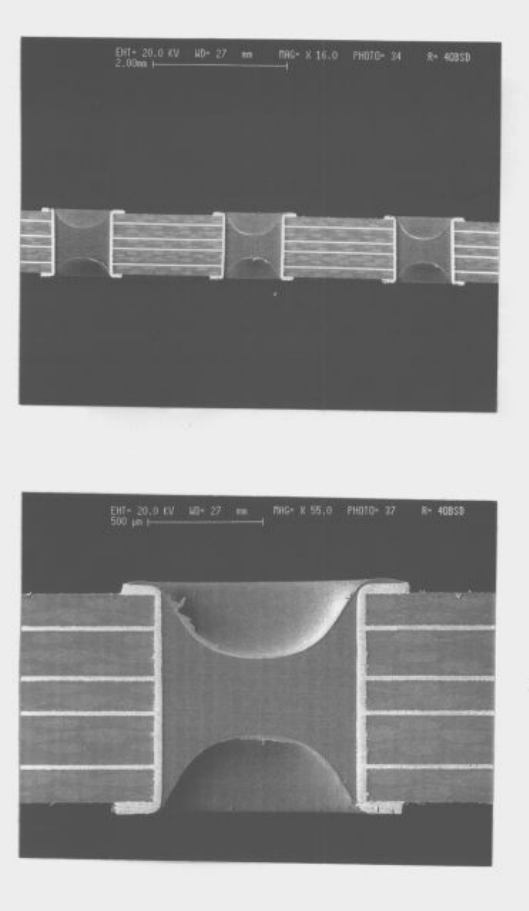


Figure 5: Radiograph of the MB showing the filling of the holes with epoxy.

items the glue of the contact holes were controlled with a radiograph (Fig. 5).

3 Field Cage

The design of the field cage has been guided by the following criteria :

- no insulating surfaces exposed to the drift volume
- single layer electrostatic field structure
- functional separation of field cage and gas envelope
- minimization of overall material thickness
- 100 μm geometrical precision of all field cage elements over the full volume

The basic elements for the electrostatic field electrodes are aluminized Mylar strips of $25\mu m$ thickness and 1/2 inch width. The mylar strips are suspended on ceramic tubes placed vertically in the corners of the rectangular field cage; to ensure mechanical stability the ceramic tubes are glued to epoxy supports (fig. 6). The epoxy support with the ceramic tubes were finally mounted on an aluminum support frame.

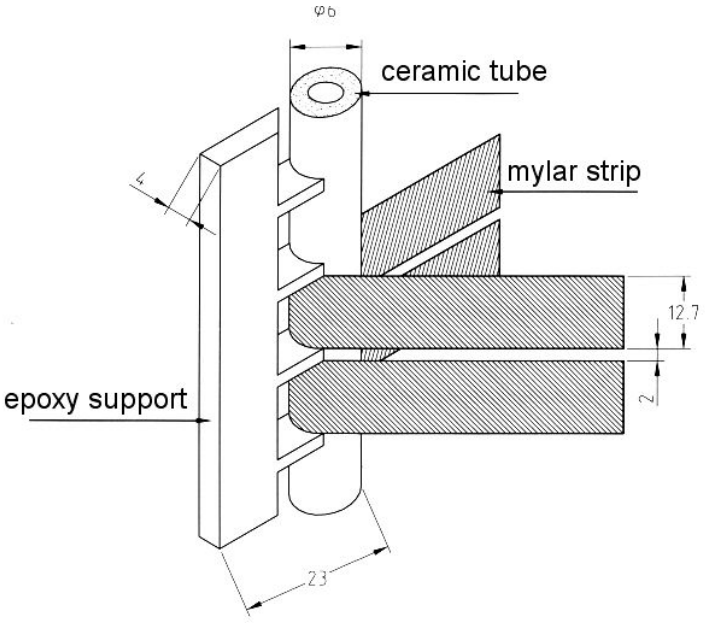


Figure 6: Support for the mylar strips of the RCC field cage

The field cage was designed to be operated even with the Lead beam passing through the sensitive gas volume. It was therefore divided into two halves separated by a gap of 1 cm to avoid field distortion due to the high ionization deposit of the Lead ions. (fig. 7)

The gas envelope is made of a single layer Mylar foil of 125 μ thickness and is completely separated from the drift field structure. The sense wire plane is directly mounted to the field cage support frame (base plate) and the RCC readout modules are inserted from below into the field cage wire structure. (compare Fig. 8).

4 Preamp/Shaper

The preamp shaper is optimized for the characteristic signal which is induced by the positive ions created during the amplification process close to the wire of the RCC. The basic design of the chip was developed within the RD32 project starting in 1992. The aim was to design a circuit with a baseline restoration better than 1 permille after 2 μs. Furthermore a very low power consumption that allows the mounting of the chip very close to the detector readout plane (pad plane) was envisaged. For the production of the chip the radiation hard bipolar process from HARRIS was chosen. In November 1997 the first 4-channel chips were cut from the wafers of a multichip project and tested at CERN. From this run approx. 350 chips were finally selected according to specification and later used for the RCC prototype. The technical specifications of the chip are summarised in table 1.

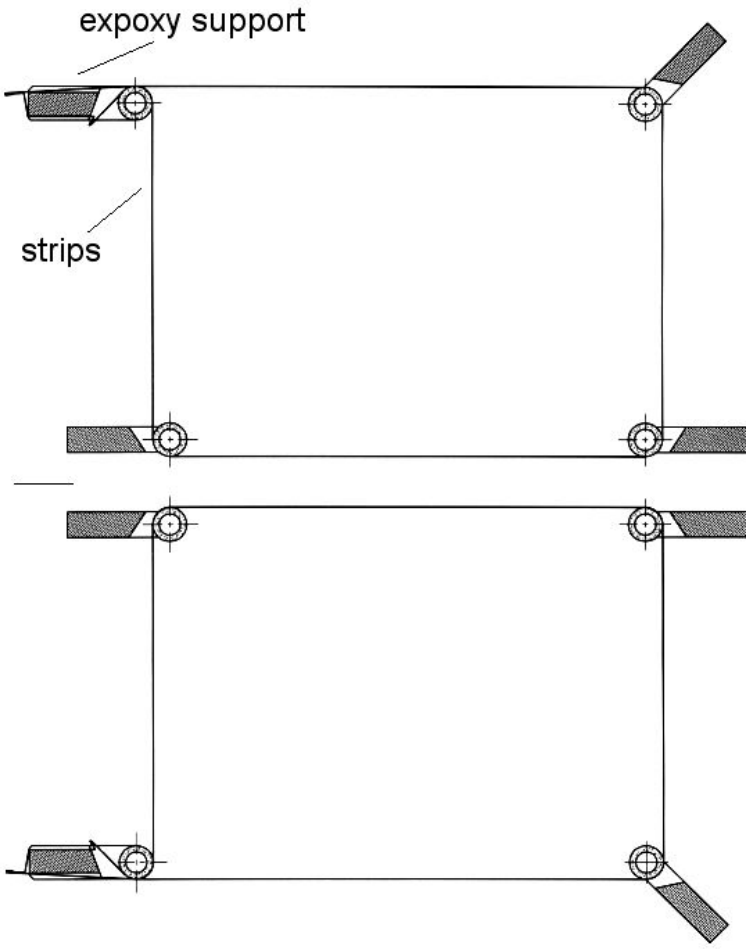


Figure 7: Top view of the field cage indicating the separation of the drift volume into two halves. The beam enters from the left and passes through the gap.

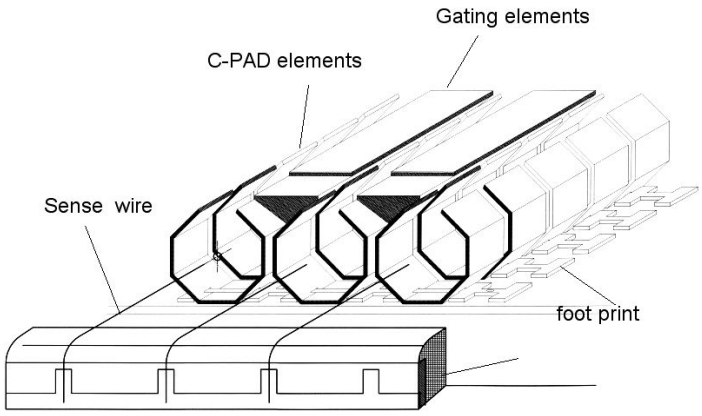


Figure 8: Wire plane mounted on the field cage base plate

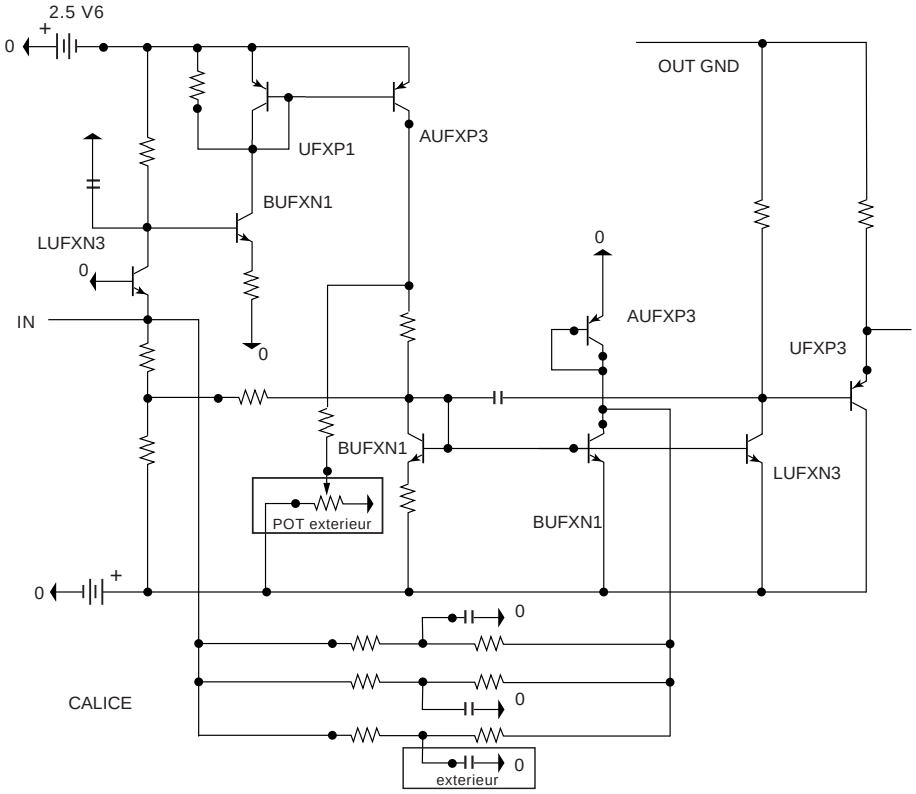


Figure 9: Circuit diagram of the PASA chip.

Process	UHF1	Nr. of channels	4
Die size	2.6 mm*2.7 mm	Package	S024/TAB
Supply voltage	+2.5 V/-2.5 V	Nr. of Adjust pot	4
Power consumption (total)	30 mW	Power consumption/channel	7.5 mW
Input impedance (DC)	150 Ω	Input impedance (at 1 MHz)	300 Ω
Conversion gain	10 mV/fC	Output dynamic range	2 V
PSRR on VCC	-30 dB	PSRR on VEE	-10 dB
Linearity	1 %	Crosstalk	50 dB
Shaping time	225 ns	Shaping capacitor/channel	1 external
Tail cancellation (1 to 4 us)	$< 2*10^{-3}$	Tail cancellation (> 4 us)	$< 0.5*10^{-3}$

Table 1: Parameters of the preamp/shaper chip.

The layout of the chip is shown in Fig. 9, the chip after production is shown in Fig. 10.

The response of the chip when connected to a small test RCC is shown in Fig. 11.

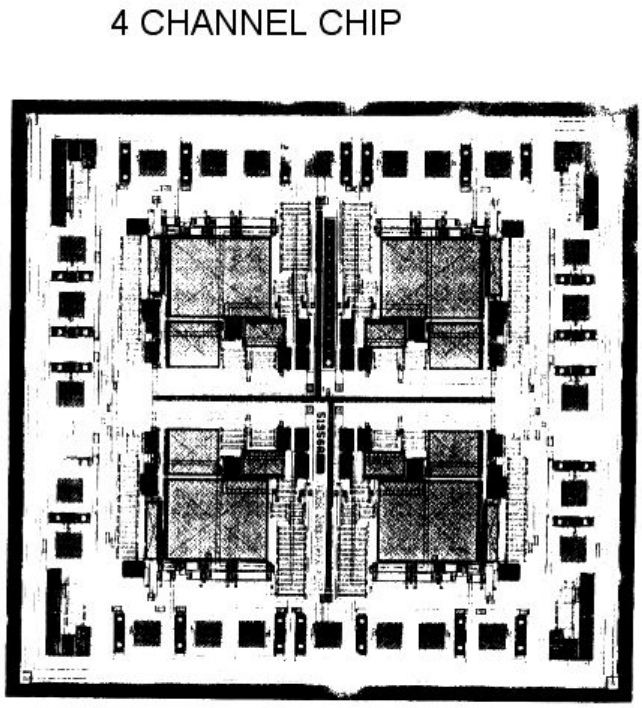


Figure 10: Photograph of the 4-channel PASA chip (die size 2.6 mm×2.7 mm).

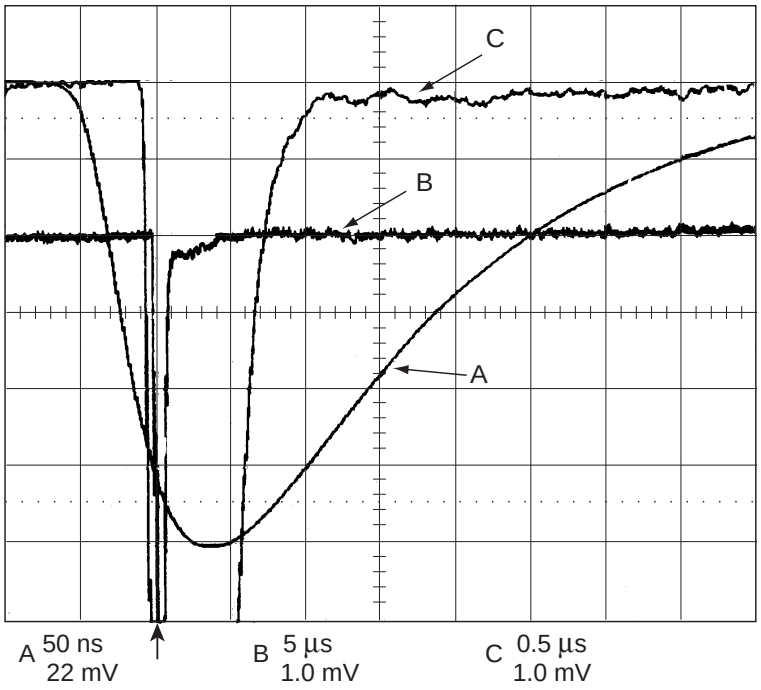


Figure 11: Signal from preamp/shaper connected to a small prototype RCC.

After production a batch of PASA dice was tested by Dassault Electronics. Based on these tests a subset of dice was selected for the mounting on the prototype readout boards. The test procedure and its application is desribed in [3] th test results and the selection procedure can be found in [4].

5 Connectic

The development of the ALICE TPC prototype was strongly influenced by constraints on manpower availability foreseen for the final construction phase of ALICE. Therefore a realistic scheme of readout production including the front-end electronics could only be achieved with industrial cooperation and the use of process like TAB that allows testability and handling of large volume production. These boundary conditions influenced finally the connectivity in general of all the other components.

The RCC prototype module was composed of the following components which are electrically coupled together to transfer the signal from the PAD directly to the ADC:
a) C-shaped pad elements
b) Multilayer board
c) PASA which are TAB-bonded directly to the backside of the Multilayer board
d) Buffer amplifier connected with FLEX TAB
e) ADC's connected via Pico-coax cables to the buffer amplifier

In Fig 12 the multilayer board with the daughter cards is shown. The ADC's are housed in VME crates located at a distance of approx. 2. m from the readout boards. It should be pointed out that in the ALICE TPC the buffer amplifier would be obsolete since the ADCs are mounted directly on the detector.

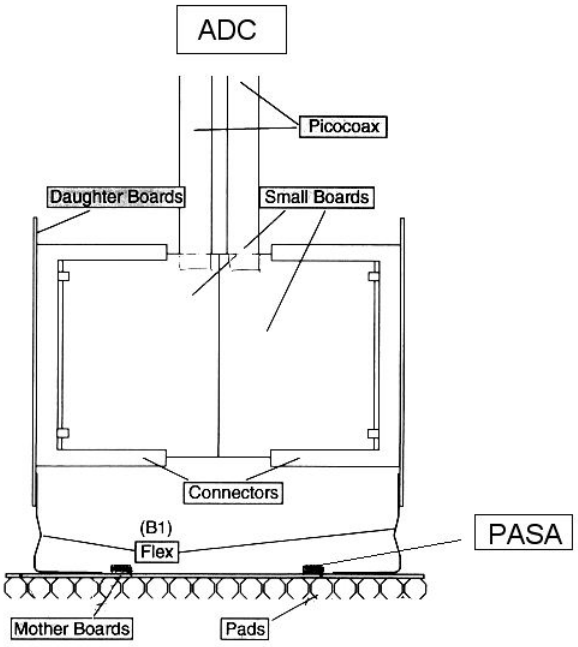


Figure 12: Schematic cross section of the motherboard with the small cards and pico-coax connectors

5.1 The Multilayer Board (Motherboard) Connectivity

The surface of the Motherboard on the pad side has specific Cu pattern, that centers the pad mechanically in the correct position and couples automatically 4 C-shaped elements

together to form one single pad. Each pad is then connected by a metallised hole through (via) the multilayer board to the input of the PASA.

The multilayer board consists of 7 layers. In Fig. 13 the layout of the MB is shown. The functions of the different layers are:
Layer 1 : component layer
Layer 2 : power for PASA (Ve)
Layer 3 : out1 and out2 of PASA and GND1
Layer 4 : power for PASA (Vc)
Layer 5 : out3 and out4 of PASA and GND2
Layer 6 : ground layer
Layer 7 : PAD (Cu foot print to connect the pad elements)

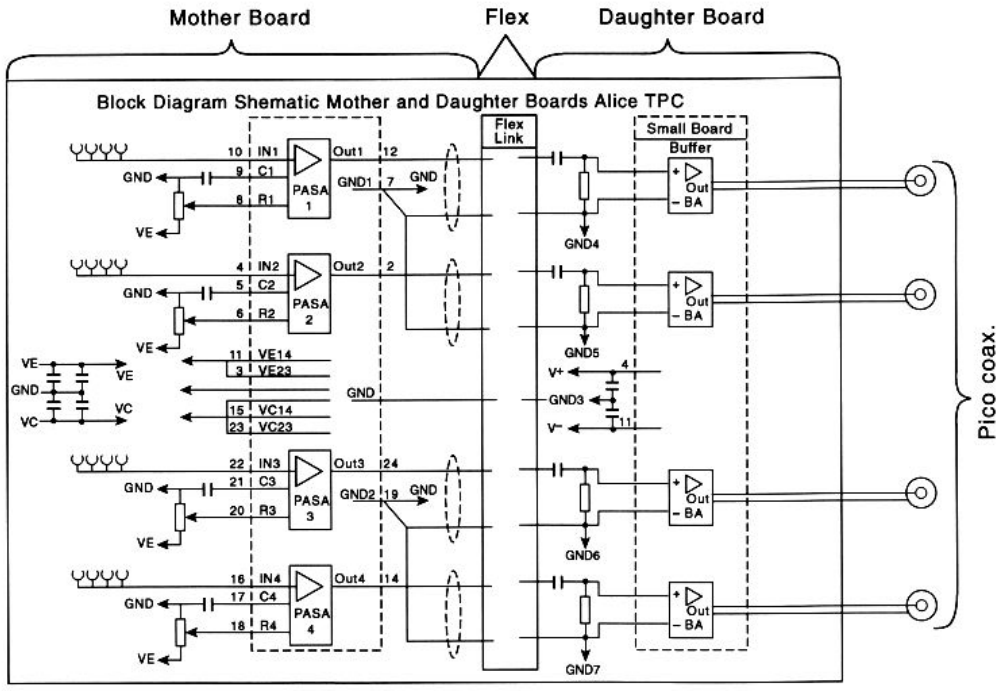


Figure 13: Circuit Diagram of the multi layer board

This architecture has the following advantages :
a) Each critical signal trace is surrounded by a ground trace to avoid cross talk (GND1)
b) Each signal layer is separated by a ground plane to avoid crosstalk
c) The GND layer is close to the pad
d) The back side of the PASA die is connected electrically to the GND reference plane.

In addition the different ground layers are interconnected by two blind conductive wires which are implemented into the MB to avoid feedback into the input of the PASA caused by voltage differences between the ground layers.

5.2 The Tape Automated Bonding (TAB) Process

The TAB [5] is a technology usually applied for production of big series where high reliability is required. In principle the TAB process in our application can be divided in the following steps :
a) Delivery of dies from the producer to the company providing TAB

b) ILB (inner lead bonding i.e. mounting of dice on tape) which allows to perform a full performance test (AC + DC)
c) Selection of dies which perform within certain quality limits (possibility to select different classes)
d) Transfer of selected dies from ILB tape to the substrate (detector back plane or PCB)

Step a) to d) would be done by the same company which delivers finally a fully functional and guaranteed device according to specifications.

5.3 Application of TAB for the Production of the RCC Prototype

For the RCC prototype we decided to bond the chip directly on the backside of the readout plane of the RCC with the advantage of fully tested readout segments which were delivered from the company. Furthermore the electrical connection from the PASA to the buffer amplifier was done with FLEX TAB connectors. The different steps of the TAB process is shown in Fig 14. The footprint of the TAB for the 4-channel chip is shown in Fig 15.

5.4 Pico-Coax Connection

To transfer the analog signals from the buffer amplifier to the ADCs we used coaxial cables (dia.: 0.5 mm) from AXON [6](type PCX 38 K10, see fig. 16). .

These cables were soldered to PCB boards (buffer amplifier cards). For the connection to the VME system (ADC's) 24-pin connector was used (see fig. 17).

6 Readout

In this chapter the digitization of the analog signals and the transfer of the data via an optical link into the NA49 data stream is described.

The data acquisition system can be operated in a standalone mode for development and test purposes or together with the NA49 DAQ system in order to participate in the NA49 data taking and to write to tape. Online event viewing is done with the standard NA49 online monitoring program which was expanded to accommodate the new detector.

In fig. 18 the readout system is shown in an overview.

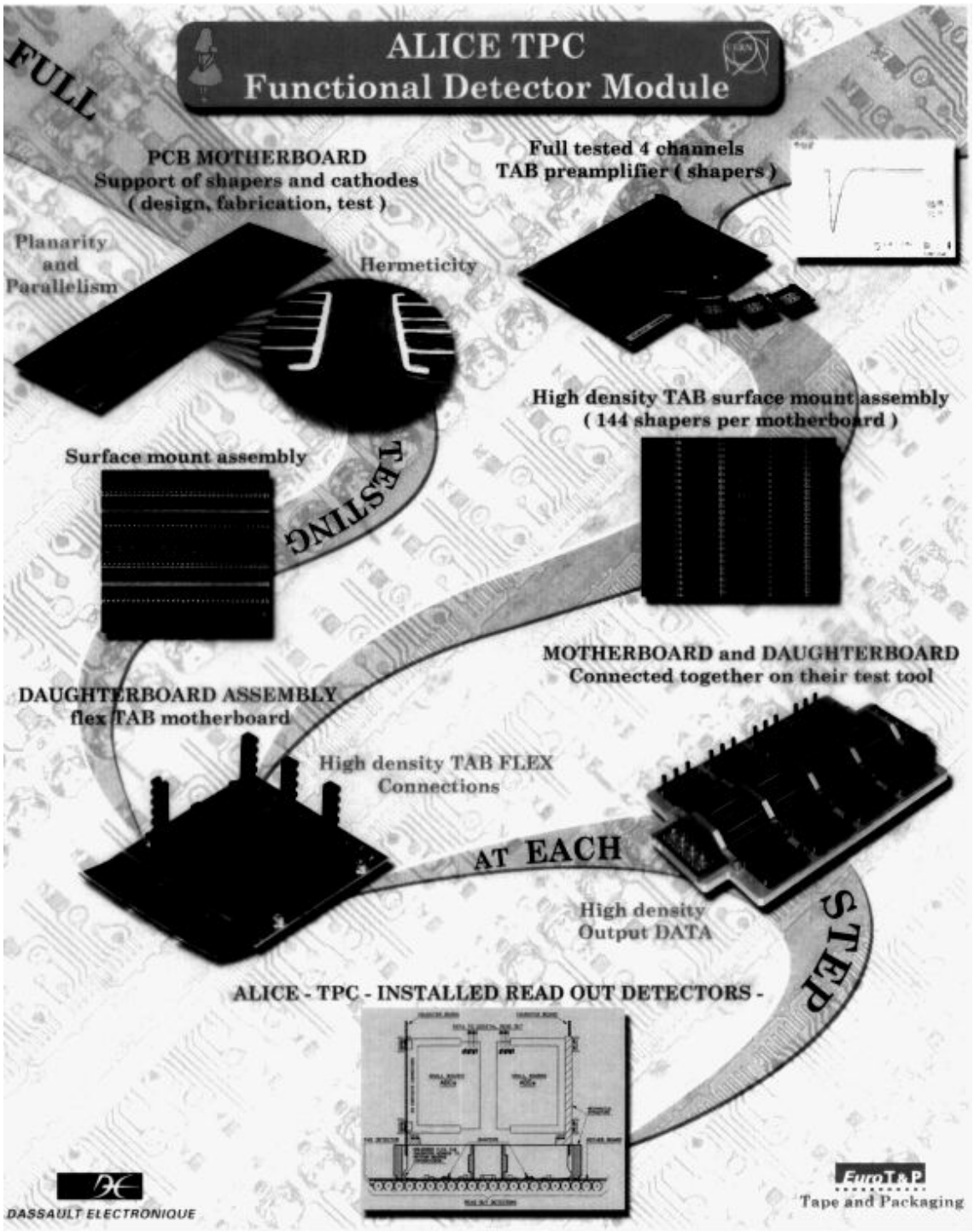


Figure 14: TAB production chain for the prototype TPC

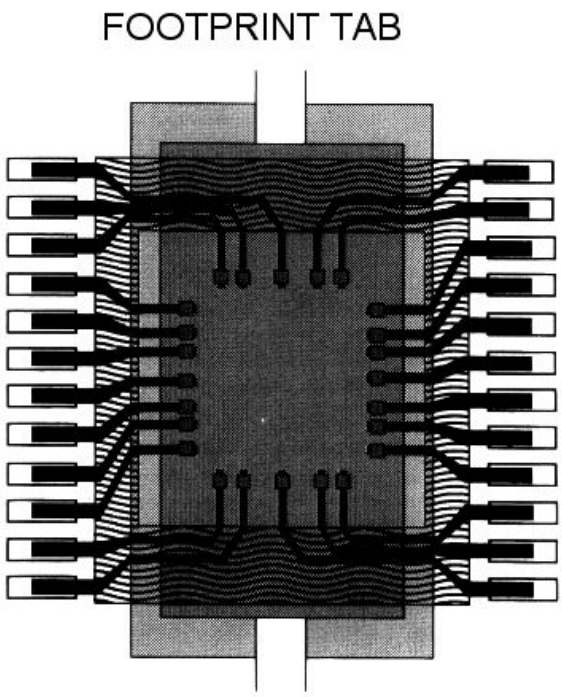
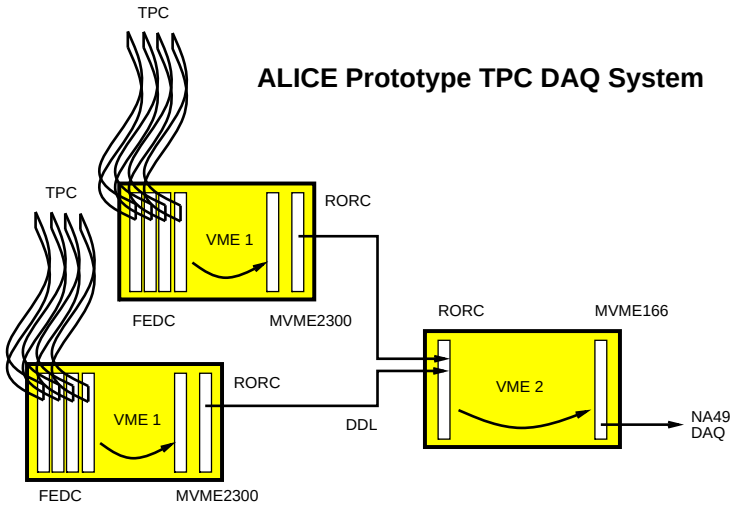


Figure 15: Footprint for TAB mounting of the 4-channel chip



FEDC	Front End Digital Card carries ADCs
RORC	Read Out Receiver Card Interface for DDL
MVME2300	CPU operating system LYNX−OS readout of ADCs
MVME166	CPU operating system OS−9 eventbuilding and data transfer to NA49 DAQ
DDL	Digital Data Link bandwidth <100 MB/s
VME 1	VME block data transfer initiated by LYNX−OS DMA 32bit
VME 2	VME block data transfer initiated by OS−9 DMA 64bit

Figure 18: Overview of the readout system

EINZELNES PICO-COAX®

PCX 38 K 10

Leiter
Versilberte
Kupferlegierung

Dielektrikum
FEP

Spiralförmige
Abschirmung
Verzinntes Kupfer

Außenmantel
Polyester (*)

(*) 8 Farben : schwarz / rot / orange / gelb / grün / blau / weiß / violett oder braun

ABMESSUNGEN

LEITER			DIELEKTRIKUM	SPIRALFÖRMIGE ABSCHIRMUNG	AUSSEN-DURCHMESSER
AWG	AUFBAU	Ø (mm)	Ø (mm)	Ø (mm)	Ø (mm)
38	7 x 0,04	0,120	0,35	0,45	0,51

ELEKTRISCHE EIGENSCHAFTEN

. Nomin. linearer Widerstand des Leiters (Ω/m) : 2,40
. Nomin. linearer Widerstand Leiter/ Abschirmung (Ω/m) : 2,75
. Kapazität (pF/m) : 100
. Wellenwiderstand (Ω) : 50

DÄMPFUNG dB/m

FREQUENZ MHz

BESTELLBEZEICHNUNG

PCX 38 K 10

Kapazität / 10
Dielektrikum K = FEP
Leiter AWG
PICO-COAX®

AXON' behält sich das Recht vor, den Aufbau dieses Standardkabels unter Beibehaltung der Haupteigenschaften zu ändern.

Kabel und Verbindungssysteme für fortschrittliche Technologien

AXON HIRBEL GmbH - POSTFACH 1131 - 71201 LEONBERG / HERTICHSTR 10 - 71229 LEONBERG - TEL. 07152/43028 - FAX 07152/46907

PICO-COAX®, Eingetragenes Warenzeichen von AXON' CABLE
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Figure 16: Data sheet of pico-coax cable

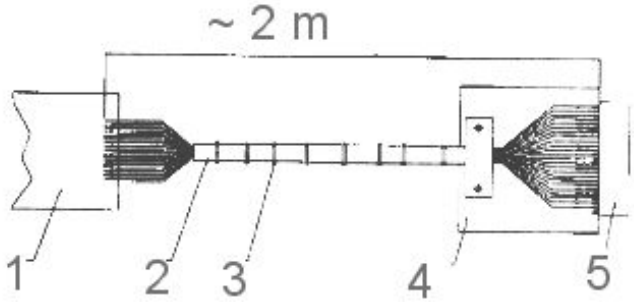


Figure 17: Connection of pico-coax cable. 1=PCB for buffer amplifier, 2=pico-coax cables, 3=protection, 4= PCB, 5= 24 channel connector (ADC side)

6.1 The Front-End Digitizer Card (FDC)

The readout of the prototype TPC is performed using a general purpose module, the "front-end digitizer card" (FDC). The module provides, for 48 channels, the following basic functions:

- 10 megasamples per second digitization of the input waveform;
- storage of the digitized data, over a programmable time interval (up to $50\mu s$), with optional baseline subtraction and zero suppression;
- transfer of trigger associated data from the front-end data memory to a multi-event asynchronous output buffer to give negligible dead times for data throughput of the order of 20 MB/s.

6.1.1 System Components and Interconnections

A schematic diagram of the system components and their interconnection is shown in fig. 19.

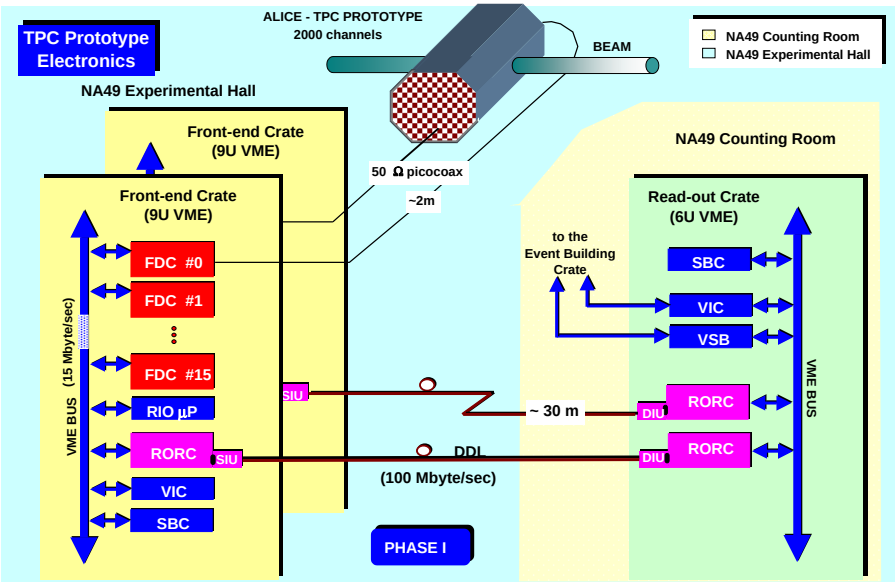


Figure 19: System components and interconnections

The front-end digitizer cards are housed in a large size (VME 9U 400 mm deep) crate, controlled by a "single board computer" (SBC), which initializes the system and steers the readout procedure. Data is moved by the SBC, via VME bus, from the FDC's to the RORC driver of the optical link, which finally sends the data to the RORC receiver, housed in the DAQ system. The system is completed by a "trigger and timing board" (TTB) which broadcasts, to the individual FDCs, the trigger and clock signals.

The readout of an event is performed in several phases, which are consecutive for a given event, but can otherwise be active concurrently. In a first phase the trigger information is received by the the TTB and broadcast to all modules in the system; it causes, in each channel, the storage of a programmable number of words (≤ 512) into the data memories. Data is then moved from all the 48 channel front-end memories into the multi-event output

buffer. This phase has strict time limits and is performed promptly. In the second phase, information is moved from the output buffers to the SBC memory. The FDC's inform the SBC that an event is ready by the generation of a VME interrupt, which starts the second readout phase. The time needed to complete the second phase depends on the size of the event, but other triggers can be processed during the readout of previous event, as long as the output buffers in the FDC's are not full. Finally in the third phase data is moved from the SBC memory into the RORC driver of the optical link which transmits data to the RORC receiver at a speed of 100 MB/s. As already mentioned all the system components are accessed by the SBC to allow software driven initialization and test procedures.

6.1.2 The FDC Board

The FDC contains 48 readout channels.

A single readout channel is comprised of three basic units: an input amplifier; a 10 bit 10 MSPS low-power ADC; a digital circuit (ALTRO), implemented in a FPGA, which contains the baseline subtraction, the zero suppression and the data memory.

:cted in fig. 20.

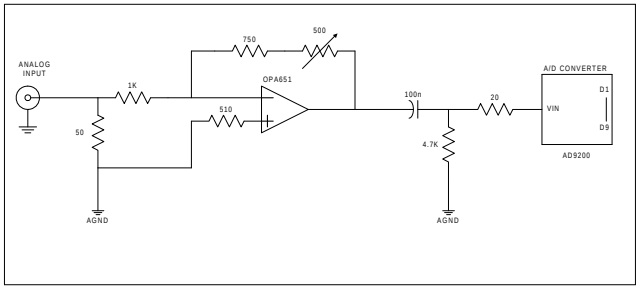


Figure 20: Cicuit diagram of the input stage of the daughter cards of the FDC board.

The board receives the analog input signals through two 24x2 (rows x column) connectors on the front panel. These signals, single-ended with a 50 Ω termination, enter the readout chain through a DC connection.

The amplifier provides the possibility of inverting the polarity of the input signal and matching the dynamic range of the input signal to the ADC's dynamic range. To this purpose, the operational amplifier OPA2651 (Burr-Brown) has been used in a configuration which allows a gain adjustment of $1 \pm 25\%$. The amplifier is connected to the ADC through a $0.1 \mu F$ capacitor. The interconnection line is terminated to ground by a 4.7 kΩ resistor; the resistor value has been chosen as a compromise between a large time constant ($470 \mu s$), needed to minimize the baseline shift, and a small offset (about 50 mV) created at the ADC input by its leakage current .

The ADC is the AD9200 (Analog Devices). Its main characteristics are listed below:

RESOLUTION	10 bits
CONVERSION RATE	< 20 MSPS
DC ACCURACY	
Differential nonlinearity	±0.5 LSB
Integral non-linearity	±0.75 LSB
Differential Reference Voltage	2 V (external or internal)
Gain Error	2% FSR

POWER	
Power-down (Sleep) Mode	< 5 mW
Power consumption	< 40 mW
DYNAMIC PERFORMANCE	
Effective Bits	
f = 3 MHz	> 9
f = 5 MHz	> 8

This ADC has been selected from a range of commercially available products based on detailed performance tests. Details of the tests can be found in [7] and in ref. [8].

This ADC is used in the FDC at a conversion rate of 10 MSPS. Under the control of the ALTRO circuit, the ADC can be put in "sleep mode" to be activated only during the detector drift time.

The ALTRO contains the digital circuitry to perform pedestal subtraction, zero suppression, formatting and buffering. In the block diagram of the ALTRO, shown in Fig. 21, the main logical units can be distiguished.

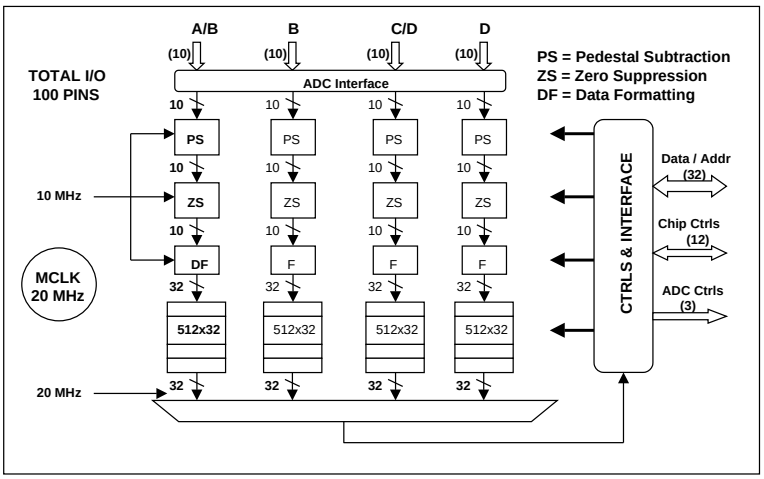


Figure 21: Block diagram of the ALTRO circuit.

In the Pedestal Subtraction Unit (PSU), the lookup table (LUT) corrects any possible systematic instability of the baseline allowing the subtraction of time dependent pedestal values from the ADC samples values. Alternatively this LUT, addressed by the ADC data, can be used to perform the corrections for a non linearity of the input signal during the pedestal subtraction. Finally the same LUT can be used to generate a test pattern. That is an important feature allowing complete tests of the overall digital readout chain.

In the Zero Suppression Unit (ZSU) the basic pulse detection scheme implemented is based on a fixed threshold, where samples of a value smaller than some constant decision level (threshold) are rejected. To reduce the noise sensitivity, a glitch filter checks for a consecutive programmable number of samples above the threshold (normally set to 2). In order to keep enough information for further feature extraction, a programmable sequence

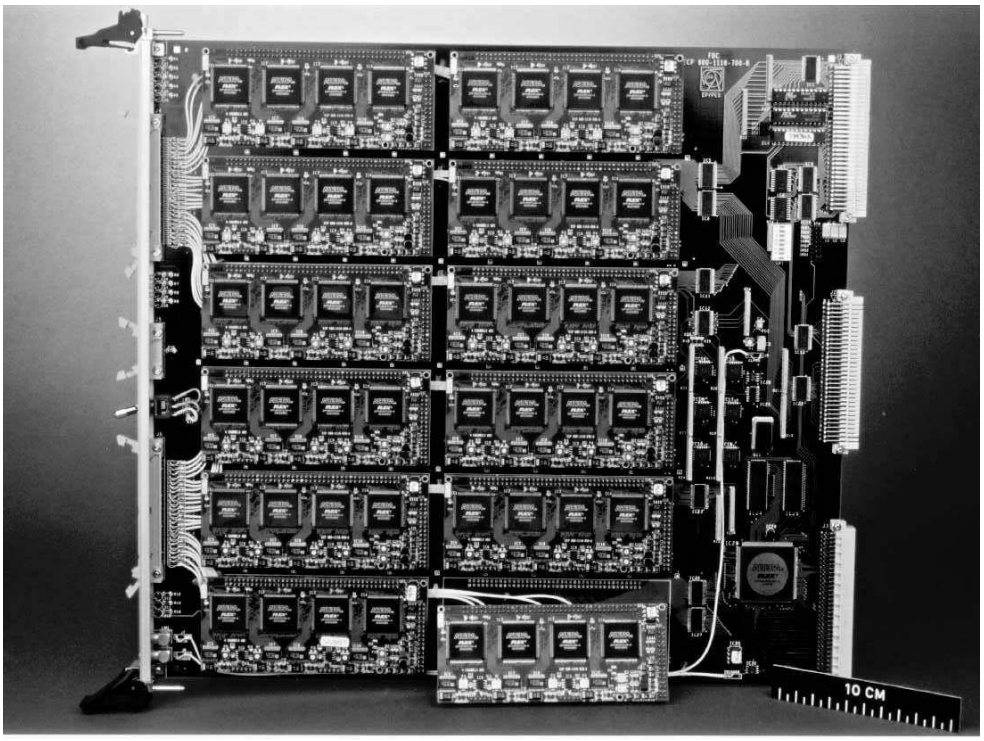


Figure 22: Photograph of the 9U FDC board with its 12 daughter cards.

of pre-samples and post-samples are also recorded. Finally, the merging of two subsequent sets, closer than 3 samples, is foreseen. The implementation of this zero suppression scheme requires 16 pipeline stages. With this pipeline a programmable number (up to 16) of samples before the trigger (pretrigger samples) can be stored. This feature allows the compensantion of the trigger latency. Trigger related data is stored in the event buffer with a depth of 512 words covering a maximum drift time of 51 us. The ALTRO circuits interfaces to the external world through a 10 bit port, for the data coming from the ADC, and a 40 bit control bus based on an asynchronous handshake protocol which can support a data transfer of 40 MB/s. This circuit is implemented in the FPGA EPF10K20-TC144 (ALTERA).

Each FDC consists of a 9U VME board (mother board) and 12 daughter cards, which plug into appropriate connectors of the mother board, each containing 4 readout channels (Fig 22). Besides the 12 daughter cards, the mother board contains the circuitry to implement the board control logic, the VME interface, the multi-event output buffer and the interface to the external clock and trigger signals. An on-board 40 MHz clock can be used to run the board as a standalone unit for test purposes.

6.1.3 The Trigger and Timing Board (TTB)

The TTB is a 6U VME board. It has 2 NIM inputs: one input receives an external clock signal to which the trigger signal from the second input is synchronized. Each of them is fanned out into 18 NIM signals, which are output from the module through 36 LEMO connectors. Alternatively an on-board 10 MHz quartz oscillator can be used as clock source.

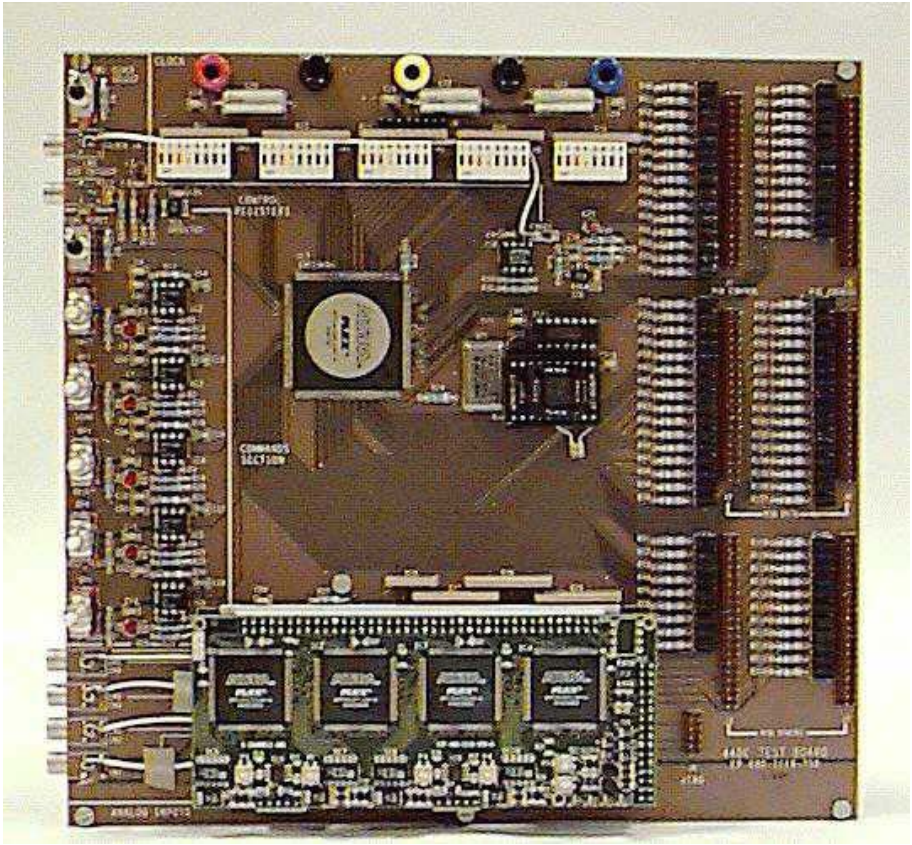


Figure 23: Photograph of the testbox with one daughter card plugged in.

6.1.4 Production and Tests

The prototypes for all the custom components of the system have been designed, manufactured and tested at CERN. For the series production, the Printed Circuit Board (PCB) and the assembly of 40 9U VME cards and 500 daughter cards have been done by industry, under the supervision of the Frankfurt University's group. For the connection from the front panel connector of the 9U FDC board to the input sockets of the daughter card thin coaxial cables have been chosen in order to guarantee a minimum of pickup from digital lines into the ADC input (see fig 22). This turned out to be big handicap for mass production since it requires expensive manual labour. For further applications the use of differential lines is therefore strongly recommended.

A dedicated system to run an automated test of the daughter cards has been developed. The test system is based on a custom "test box" (fig 23), where the daughter card is plugged in, and is completed by a standard Waveform Generator and a Logic State Analyzer. The operation of the test system and the evaluation of the results do not require a specific knowledge of the 4ADC daughter card. The full test of a single daughter card requires about 1 minute. The test system can be improved to allow the test of more daughter cards concurrently.

The FDC equipped with its 12 daughter cards is then tested in the VME environment, for which a set of test programs has been developed.

6.2 The Detector Data Link (DDL)

The Detector Data Link has been developed to constitute a standard interface between the ALICE sub-detectors and the DAQ system. It will interface the front-end-electronics (FEE) of all the sub-detectors to the read-out receiver cards (RORC) of the DAQ [9].

In the standard configuration the DDL consists of a source interface unit (SIU), connected to the FEEs and placed inside the ALICE detector, a destination interface units (DIU) connected to the RORCs and located in the counting room about 200 meters from the detector. The two DDL interface units are connected through two multi-mode optical fibres.

Each DDL transmits event data at a rate of 100 MB/s with a detected bit error rate of $< 10^{-15}$. As the zero suppression algorithm requires downloading blocks of data into the FEE, a throughput of 10 MB/s is also needed in the opposite direction.

The RORC interfaces the DDL to the VME bus. Up to 2 DDL channels can be connected to the prototype RORC. For each DDL channel, the RORC provides a 1MB output buffer for the outgoing data blocks and a 2MB dual-port input buffer for the event data. The RORC buffers can be read and written through VME bus with a maximum speed of 40 MB/s, using the Multiplexed Block Transfer Mode (MBLT) mode.

The performance, the protocol and the bit error rate of the complete read-out chain (processor → RORC → DIU → DIU → RORC → processor) has been tested.

6.2.1 DDL Configuration

In the prototype TPC readout system, the DDL is used in a DIU-DIU configuration [10] [11]. It means that data are transmitted through the DDL between two VME crates. A read-out Crate is located in the NA49 counting room, containing the Master RORC with two DIUs. The two Front-end Crates are installed close to the TPC detector. Each of them contains a slave RORC with a single DIU. For requesting an event transfer, a command is sent from the read-out crate to the front-end crate. This transaction is followed by the transmission of an event form the front-end crate to the read-out crate. Figure 24 shows the DDL configuration, used in the ALICE-TPC test system.

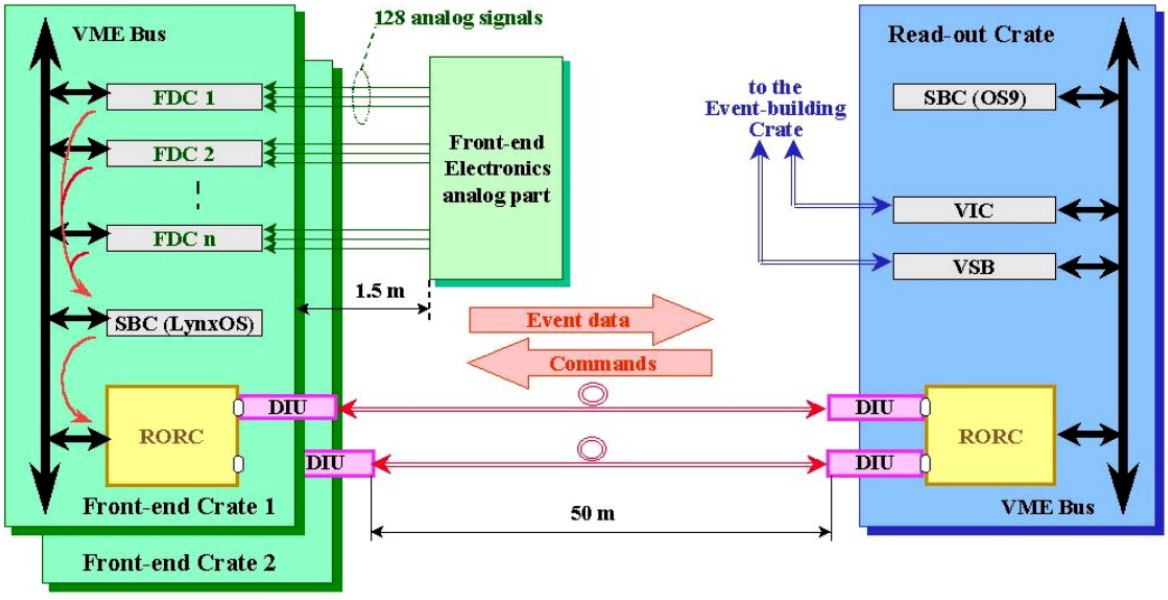


Figure 24: The DDL configuration, used in the ALICE-TPC test system.

6.2.2 DIU Configuration Problem and Possible Solution

During the installation of the DDL in NA49, DIU configuration problems were observed. The configuration files of the DIU protocol chips are stored in two on-board PROMs. These files are automatically downloaded from the PROMs to the protocol chips after

each power-on. Sometimes, however, several power-on/power-off cycles were required for the execution of a proper configuration procedure.

The core logic of the protocol chips are supplied from +3.3 V, while the I/O pins of these chips and the configuration PROMs from +5 V. Configuration problems have only been observed in those cases, when the power-on rise time of the +3.3 V and the +5 V power supplies was very different. This timing value strongly depends on the load of the power supplies. Thus the application of the automatic power-on configuration scheme is not a reliable solution a in multi-voltage environment. In the next generation RORC and DIU, we propose therefore to use a different configuration scheme, where the configuration files to each PLD will be downloaded via a single JTAG chain, controlled by the VME processor through the backplane.

6.2.3 RORC DMA Problems and Possible Solutions

The RORC integration in NA49 has pointed out two RORC hardware problems appearing mainly in heavily loaded VMEbuses used by several devices.

The first was the phenomena that the last "x" words - reading one of the Input Buffer of the RORC in the MBLT mode - was false, in spite of the fact that the data in the buffer was good. The explanation of this reside in the MBLT transfer of the RORC, which depends on the following things:
The RORC VME controller (CYPRESS CY7C961)
The Processor-board VME controller (UNIVERSE II)
The VMEbus traffic (jammed or silent)
The programming of the UNIVERSE II.

Here we deal with the RORC-side only, as the other participants are given, and we have to adapt to them.

The second is the block-braking, which could have occurred , causing operation fault, as the software is not prepared to manage this situation. We hope that the latest RORC hardware modifications answer these problems.

A. The Multiplexed Block Transfer Mode (MBLT) transfer of the CYPRESS-CY7C961 controller chipset

A very important feature of the (M)BLT transfer mode is the pre-read capability of the chipset, which means that the data from the RORC input buffer bank is read ahead, stored temporarily in the VME controller buffer, and when the read request arrives from the bus, will be immediately put onto the VMEbus. Without pre-read the (M)BLT transfer would be as slow as the single-cycle transfer, so the pre-read capability is an integral part of the (M)BLT transfer.

The problem arises at the end of the MBLT read, because - if there is a pre-read, - these words are not transferred to the VMEbus from the temporary buffer, but are overwritten with the words read from the same address at the beginning of the next MBLT block. As a result: some addresses of the input buffer banks are read twice.

The input buffer of the RORC operates the same way as if it were a FIFO, i.e. one has to read exactly the same number of words from it as were previously written into it. The RORC control logic contains two counters, a write and a read counter. If the read counter reaches the value of the write counter, then the input buffer bank is closed for reading and opened for writing. The read counter is incremented by every read cycle independently of the read address. If some addresses are read twice, than the read counter reaches the value of the write counter before all data words are read from the bank. The words which are read after the bank is closed are not originating from the memory bank but the Local

Bus, so they are false.

One can avoid this problem only by applying the MBLT reading-roles shown in Fig. 24, or making the UNIVERSE II chip close the (M)BLT transfer in such a way, that the pre-read appearance at the end of the (M)BLT block is prohibited.

The experience is: in NA49 the MBLT burst, instead of 256-bytes, was only 32-64 bytes long, so every MBLT read caused extra pre-read of two 32-bit words, and this prohibits the appropriate reading of the end-of-data in the input banks.

For example: if the processor reads the N word-long-block in 8 double-word-long MBLT blocks from the input buffer, and n = N/16, ie. the N-word-block is read by "n" pieces of MBLT blocks of 8-dword, then every small block (except the ones which ends at xxxxxx00 address boundary) will cause an extra pre-read at the block end, so the last "2n" words can not be read well from the bank.

Another fault was that at NA49 the single-cycle read was not used:
to avoid the extra pre-read at the block end,
to ensure the starting address alignment at the beginning of the MBLT block read.

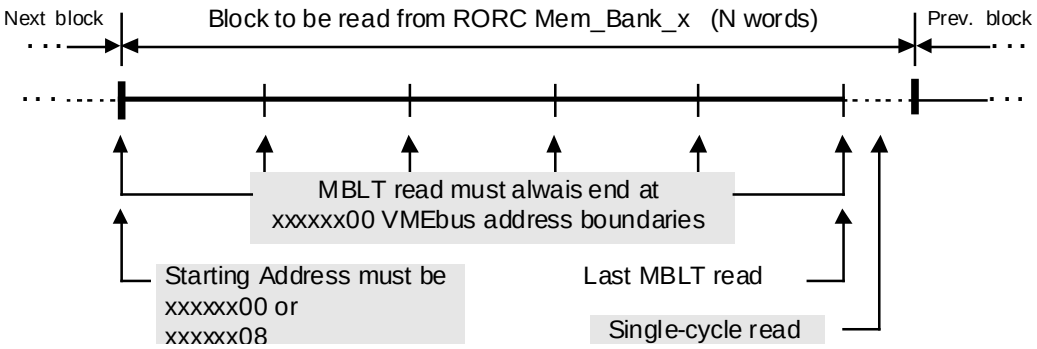


Figure 25: The necessary reading-roles to avoid extra pre-read in MBLT mode.

The lesson is that: the roles in Figure 25 are not realizable in a multi-device, multi-task environment with jammed bus traffic; so the RORC has to be modified.

(This is accomplished and tested already, now the RORC operates well in MBLT mode - independently of the block-size used in read the input bank or write the output bank. The solution is that the incrementing pulses of the read-counters are originated directly from the VMEbus control signals - instead of using the RORC local bus signals.)

B. The block-braking event caused by bank-writing overflow.

Figure 26 shows two bank writes: the first is a normal one, the second happens, when the incoming last block-size is too big to fill in the remaining place of bank 1. In this case the last block is broken into two parts, and the second part will be written into the freed bank 0. The software does not process this case, so it could cause operation failure when occurring.

The solution for this problem is that the near-full threshold can be programmed now by the software, so the last block-size never exceeds the space available to write over the threshold.

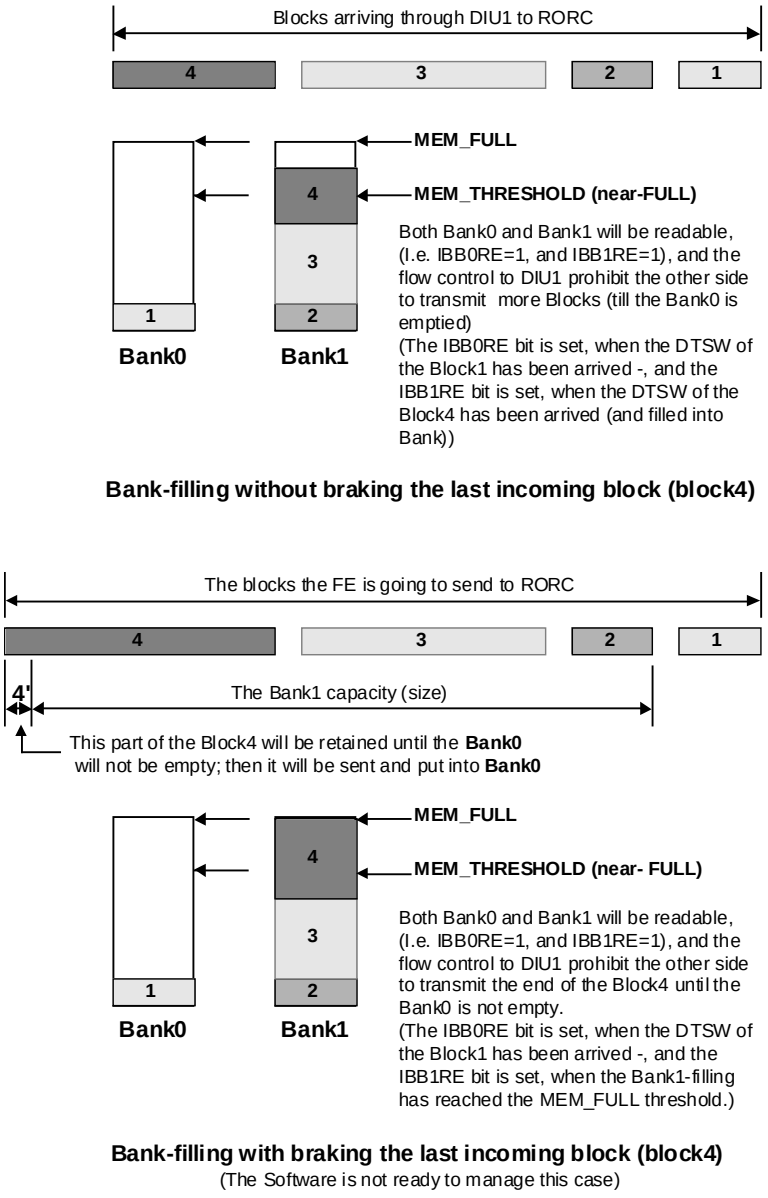


Figure 26: Bank-filling without - and with bank-overflow.

6.3 DAQ

For the readout of the two 9U VME crates housing the front-end digitizer cards (FDC) two Motorola MVME2300 processors were used. Originally it was foreseen to use MVME2604 processors but due to better availability from the electronics pool and easier mounting in the crate (the MVME2604 uses a 6U rear plane card for terminal and network I/O) and higher speed we later switched. Since both processors are binary compatible this switch did not require extra software effort. The processor is booted via the network from a boot server provided by CERN and runs under the operating system LynxOs. The NA49 DAQ uses OS9, the ALICE DAQ prototype presently uses AIX. Since there is no direct connection to the NA49 DAQ (only via the detector data link (DDL)) it was decided to use the more modern real time system LynxOs in the two front end VME crates.

The following performance was measured with the LynxOS system:
interrupt latency when triggered by the FDC or RORC: 40 μs
DMA setup time (to read FDC): 10 μs (single-user-DMA), 100 μs (multi-user-DMA)
Transfer rate in DMA mode: 8 - 10 MB/s

(A24/D32 between FDC and MVME and A32/D64 between MVME and RORC)

Therefore the DMA was used in a single process managing the FDC readout and the communication with the DDL. The advantage: no shareable memory is needed and no overhead for control of the DMA. Since the MVME2300 can access ′only′ 1/4 of the full VME address range the readout used the A24/D32 window.

The VME crate housing the receiver units for the DDL is controlled by a MVME-166 processor running under OS9. The data are transported via a VSB connection to the NA49 event builder crate whereas the control of the readout is performed via a VIC-bus connection. The new detector is an extension of the NA49 readout scheme [12]. The crate also accomodates a trigger module for standalone operation and 64 MB memory module which was partly used for system purposes. To allow fast DMA transfer of the data from the RORC module only on-board RAM was used for event buffering purposes. For booting and event storage a UNIX workstation connected via ethernet was used.

The readout software is divided into several processes in a modular way to accomodate switching from standalone operation to joint NA49 operation with only limited software overhead. The communication between processes is done via shared memory.

In case of the standalone system the following processes are used:
1. readout of the DDL and data store in a local buffer
2. check for available memory and waiting for next trigger
3. transfer of data to disk
4. eventserver to allow access to the eventbuffer for online display purposes

When the system is joined to the NA49 DAQ system the last 3 processes are residing in the NA49 eventbuilder.

A rate of about 10 events/spill could be achieved. The limitation was due to the limited available on-board memory size of 8 MB in the OS9 processor.

7 Electric Connections

The electric connections of the prototype TPC can be grouped in three parts: electronics low voltage supplies; readout connectivity; chamber voltage supplies and detector control. The low voltage system has been described above. The readout connectivity consists out of 2 x 576 pico-coaxial cables in groups of 24 between the two readout modules and two digitalization crates. These crates are otherwise supplied with ethernet, external clock and trigger signals (3 BNC cables), a CAN-bus loop (two Dsub9 cables) and terminal lines (2 x Dsub25). Two optical fibre connections are used for the digital data links.

The chamber voltage supplies and detector control connections are shown in Fig. 27. Three high-voltage connections supply drift and sense voltage, whereas three BNC cables connect to gating grid and skirts. The detector control system described in Section 9 uses one multi-twisted-pair cable for temperature control and two simple twisted pair cables for drift field monitoring.

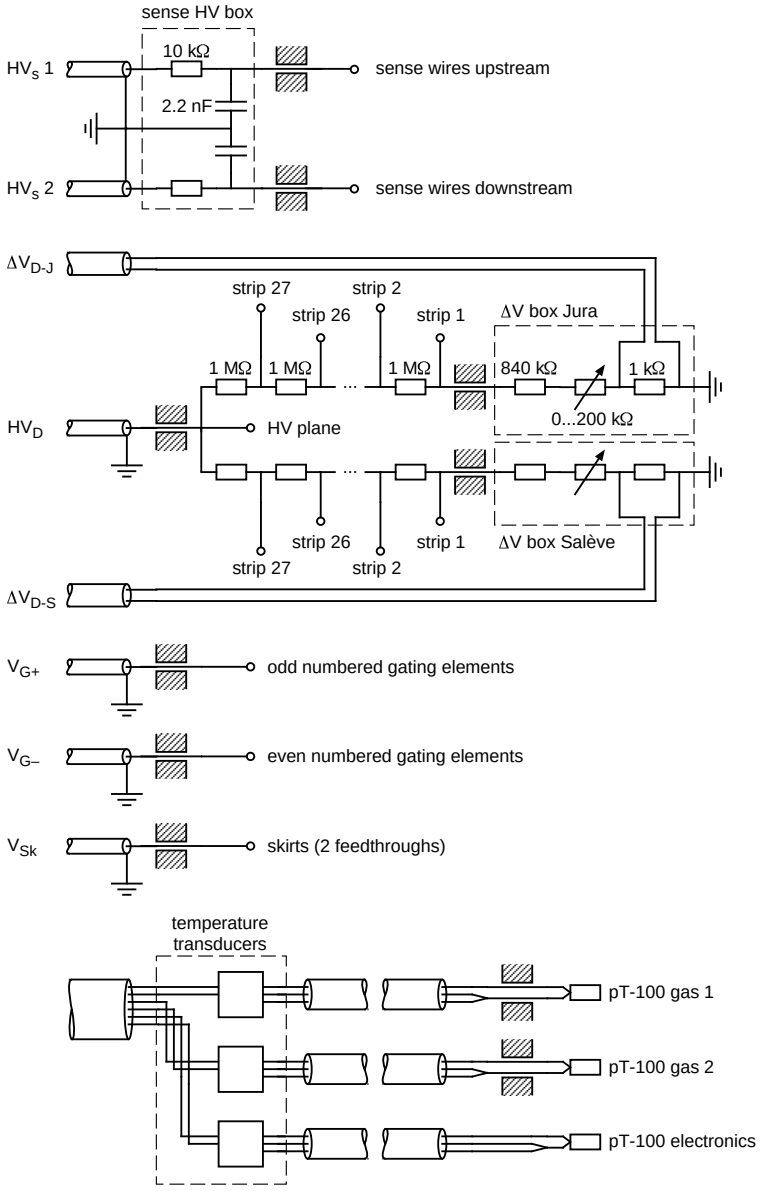


Figure 27: Electrical connections to the prototype TPC.

All grounds of incoming supply cables as well as the readout module ground on the chamber side and on the electronics side are connected to the detector base plate.

8 Low Voltage

Each readout module (or motherboard, MB) contains 4 x 144 = 576 electronics channels. The 4-channel preamplifier-shaper chips (PASA) dissipate 5 mW/ch at +-2.5 V (1 mA/ch) and the buffer amplifiers on separate daughter boards (DB) consume 50 mW/ch at +-4 V (6 mA/ch). Hence the total current requirements for the operation of one readout module are $\tilde{0}$.6 A for the PASAs and $\tilde{3}$.5 A for the daughter boards.

While the buffer amplifiers (gain 1) are relatively insensitive to noise from and voltage drift of the low voltage supply, the PASA chips require a low noise voltage supply with a stability of better than 5 mV for stable gain. To avoid electrical coupling of the readout modules via the PASA supplies, each module is served by a completely separate chain of a

linear power supply (Gossen 33K7 5/2, slightly modified for finer voltage adjustment), low impedance twisted pair supply and return lines and twisted pair remote voltage sensing lines. The buffer amplifiers on the daughter boards are all served by one pair of high-current power supplies (Delta Elektro SM 6020) and common twisted pair supply, return and remote sensing lines.

The power supply units are placed at several meters distance from the detector. For easy access during operation a dedicated low voltage distribution box close to the prototype fans out the 20 m long large-cross section supply lines into short, flexible section leads supplying the four individual PASA low voltage connectors and eight daughter boards per motherboard (Fig. 28).

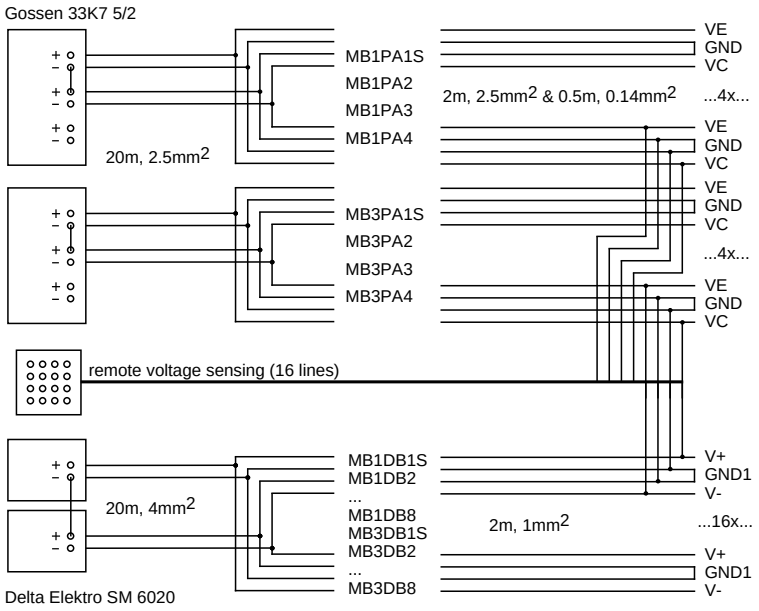


Figure 28: Low voltage connections.

A total supply line resistance of 180 mΩ for the PASA lines and 95 mΩ for the daughter board cables, together with total currents of $\tilde{0}$.6 A and $\tilde{7}$ A (all daughter cards are supplied over one common line) respectively results in a total voltage drop between power supply and electronics of $\tilde{1}$10 mV for the PASAs and $\tilde{6}$50 mV for the buffer amplifiers. Hence, the total power requirement including a 30% safety margin is 2 x 1 A at +- 2.6 V for the PASAs and 10 A at +-4.7 V for the daughter boards.

9 Slow Control

9.0.1 User Interface

Temperature control and drift field monitoring were incorporated into the existing NA49 slow control system as detector control of the prototype TPC (FTPC). The monitoring channels for the FTPC (five temperatures and two drift field monitors) are defined within the NA49 slow control user interface as the two items "FTPC Temperatures" and "FTPC Resistor Chains" in the menus "Temperatures" and "E&B Field" respectively (Menu definition is done in the routine SC_Menu_Globals.vi). The corresponding readout channel definitions are summarized in Table 1. The two drift field monitoring channels 803 and 804 are redefinitions of existing but unused channels originally foreseen for alternative

magnetic field readings of the NA49 main magnets. Five channels for temperature control and the corresponding ADC IDs have been newly created.

9.0.2 Drift Field Monitor

The drift field is measured via the voltage drop across a 1 kΩ precision resistor between the end of the field degrader resistor chain and ground. The field degrader has a total resistance of 27 MΩ , hence the field monitor reads 37 mV per 1 kV of drift voltage.

9.0.3 Temperature Readout

Temperatures are measured with 0.1(tm)C-calibrated pT-100 sensors, which are connected with 2 m long three wire cables (The blue, red and black wires are assigned to contacts 1,2 and 3 respectively on the Burndy connectors. Contact 1 corresponds to one end of a pT-100, contacts 2 & 3 to the other end) to precision temperature transducers (Phoenix Contact MCR-PT100/U/DC) converting the sensor resistance into a 0-10 V signal. The voltage signals of several transducers are transmitted to the NA49 counting house via a 27 m long multi-twisted-pair cable (see Table 2) and fed into a 32-channel CAMAC differential ADC (LeCroy 2232/A).

The calibration of the temperature transducers is performed with a temperature calibration box that contains adjustable precision resistors. In a first step, separate sockets allowing a precise four-wire measurement of the resistor values are used to set these to 100.39 Ω and 107.79 Ω , which corresponds to the values of a pT-100 at 1^0C and 20^0C respectively. Then, two connectors compatible to the temperature readout cables are used to connect each temperature transducer to the calibration box and adjust the zero-point and slope of the unit.

10 Ring-Cathodes: Mass Production Issues

For the ALICE TPC about 1.5×10^6 of cathode pads will be needed. The production of a large quantity of cathode pads has to fulfill the following conditions:

- precision of all dimensions of the pad better then $\pm 0.02mm$
- low Z material
- material with minimum ageing
- minimum thickness of the pad walls
- pad production speed: $1pad \leq 5s$
- high precision and fast positioning of pads on the motherboard
- low cost

To fulfill the above mentioned conditions for a large quantity pad production several methods were considered:

- High pressure injection of the plastic material to the form with subsequent metalic coating. Material: polycarbonate, polystyren etc.
- Pressing of ceramics to the form with subsequent metalic coating. Material: ceramics.
- Extrusion of aluminium profile with the necessary shape and cutting it to pads. Material: aluminum.

- High precision cold forging in one step. Material: aluminum.

- High precision cold forging in several steps. Material: aluminum.

We discarted plastic materials, because of the risk of outgasing and problems with the quality of metallic coating. Ceramics we discarted because of price and problems with shinking after production.

Extrusion methods may lead to complications because of large deformations and sharp edges created during the cutting process.

On the basis of discussion above we found the method of aluminum pad production by high precision cold forging the most suitable.

10.1 High Precision Cold Forging.

10.1.1 One Step Forging.

The dimensions of a C–shaped pad fulfilling the requirements of the pad response function in the ALICE TPC is shown in figure 29. Signal fluctuations along the anode wire should not exceed about 2.5% requiring a precision of $\pm 0.02mm$. Tiny "legs" in the bottom of C–pad are for the positioning of the pad to the corresponding holes on the motherboard.

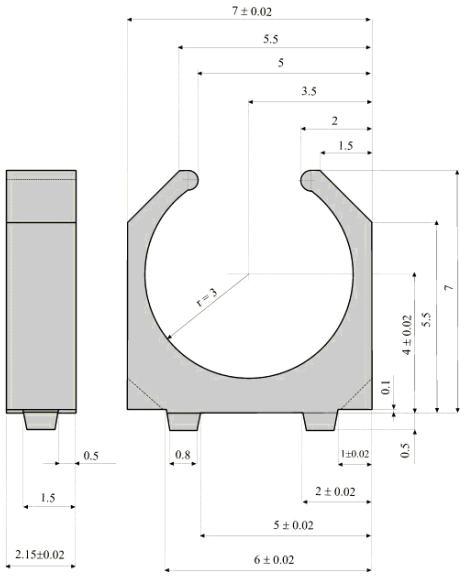


Figure 29: Pad geometry.

The cold forging is made in a form shown in figure 30 in a one step process. The form (fig. 30a) is placed inside the supporting apparatus, which is inserted into the excentric press with the maximum force of $3000kp$. The press provides not only the stroke with necessary force and speed, but also the movement of all parts of the apparatus.

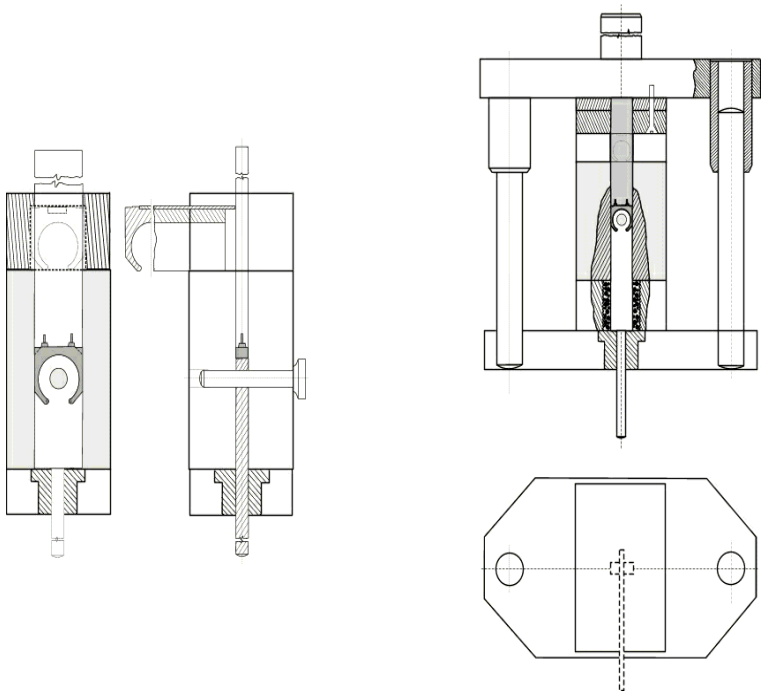


Figure 30: Form for the cold forging.

For the pad production we used aluminum formed to a rectangular rod with precise dimensions, which was inserted into the rectangular hole. The cutter cuts a well defined piece of aluminum, which is then formed to a C–pad by the same stroke.

Several hundreds of C–pads were produced by the one step forging method. Measurements on the product show, that it is practically impossible to forge C–pads of the necessary precision from the technically pure annealed $Al(99.6\%)$ with a hardness of $26HB$ (in Brinell scale).

We used also soft annealed high–purity $Al(99.999\%)$ with $6HB$ hardness, which gives much better results, but even in this case the edges are rounded in the far corners of the pad. The main problem of the one step forging are the very high stress forces in some parts of the moving and shape–forming cutters. Also the simulation of the stress forces in the apparatus showed, that there is a high probability of breaking the cutters after several forging procedures.

10.1.2 Three-step Method.

In this case, the production of aluminum C–pads is divided into three steps (fig. 31). In the initial step, a well defined piece of aluminum is cut and by the same stroke is forged to a U–shape, with the arms longer then in the final pad. Th advantage of this method is, that we are not filling a closed form, but the aluminum is released to the open space, considerably lowering the stress forces and improving the quality of the pad.

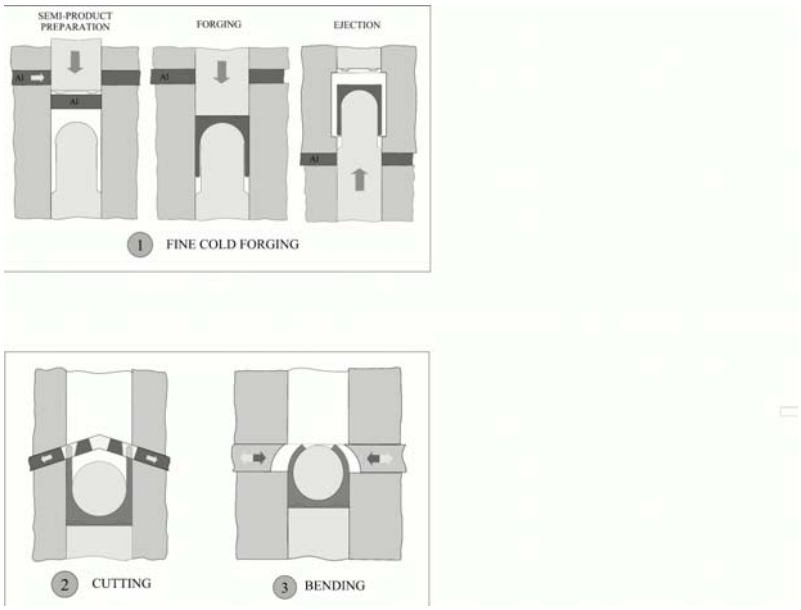


Figure 31: Three-step method.

The first step consists of three phases. In the first one a piece of aluminum with the dimensions of $1.8 \times 2.4 \times 5.75mm^3$ is cut. In the second phase the forging to the U–shape is performed. In the third step the U–pad is taken off the form and then cut by a special tool.

The second step is the cutting of the arms to the necessary length. Cutting is performed in a special tool at an angle of $10°$ from the inside of the U–pad. No sharp edges are created by this method on the inner part of the pad.

In the last step the pad arms are bent in a special tool, connected with the cutters for the second step.

Each of the three steps does not take more then $5s$. A pad produced by this technology is shown in Fig. 32.

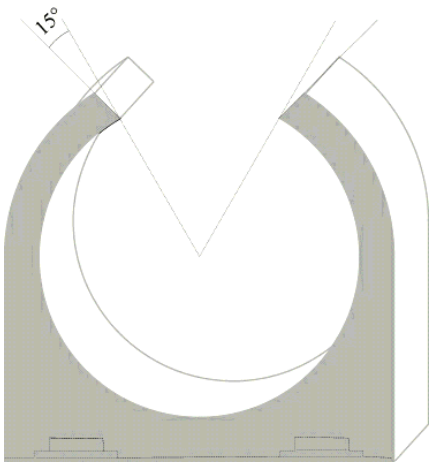


Figure 32: Pad produced by the three-step forging technology.

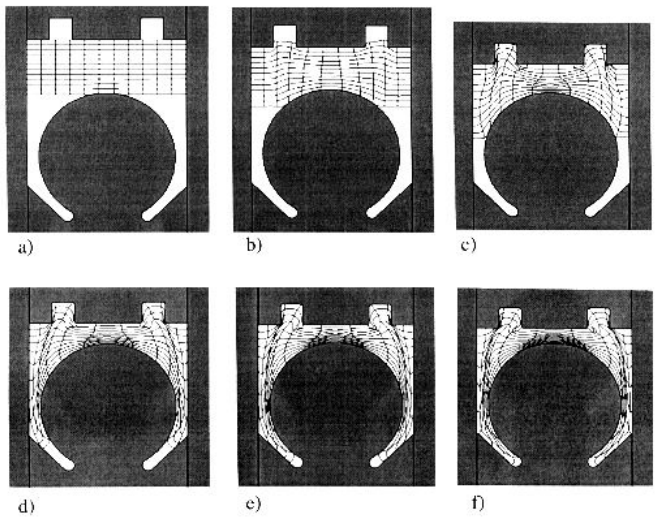


Figure 33: Simulation of the forging process of the "old" C-pad.

10.2 Simulation of the Forging Processes.

10.2.1 Forging Process of the "old" C-pad.

Plastic flow of the material (Al) to a form during the forging is shown in Fig 33. The filling of the form during the forging is shown from a. to f.. The flow of material and the stress is visualised by the deformation net. In Fig 33a there is aluminum in the rectangular form. Fig 33a-c shows the filling of the upper part of the form. In the Fig 33d-e the lower part of the form is filled. The edges are filled only in the last (f) phase of the processes. The large stress on the top of lower shaping tool is visible.

10.2.2 Forging Process of the "new" C-pad.

In Fig 34 a plastic flow of aluminum for the "new" shape of the C-pad is shown. In the new shape the arms of the C-pad have the same cross section. This is advantageous for the regular flow of material to the arms. The phases a-c are similar to the Fig 33. The lower part of the form is filled more smoothly (d-f) and the filling of far edges of the form is better.

10.2.3 Forging Process of the "U"-shape Semiproduct.

In Fig 35 there is shown a material flow of aluminum formed to the U-shape. In this case it is possible to further decrease necessary stress (material does not need to fill in thin sides of the pad) and to improve form design.

10.2.4 Comparison of mean Stress in the Forms.

In Fig 36 the mean stress in forged material is shown. The new shape of the form considerably decreased the maximum stress from 1166 MPa to 684 MPa, which is more then 40% difference. One should keep in mind, that stress over 1000 MPa often causes break-down of the tool.

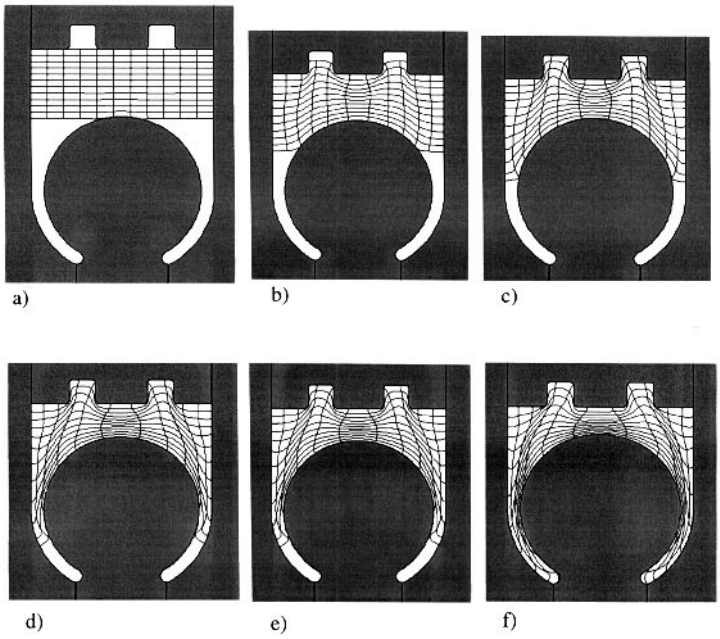


Figure 34: Simulation of the forging process of the "new" C-pad.

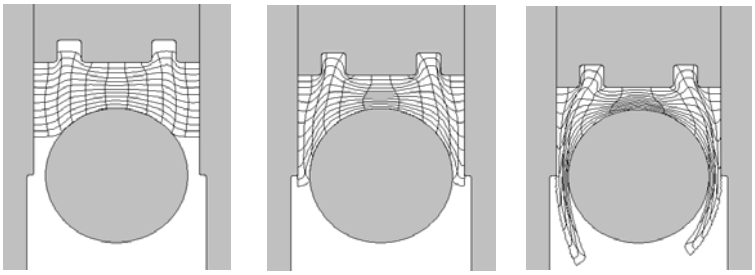
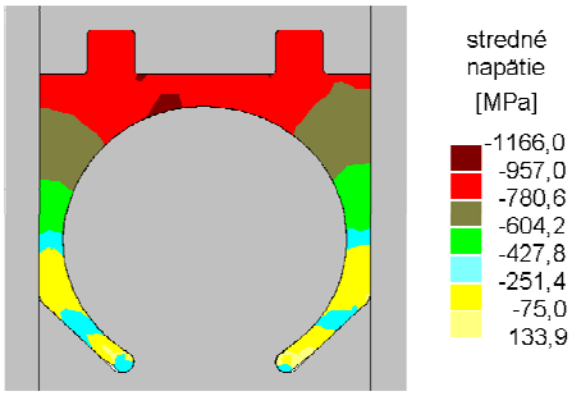
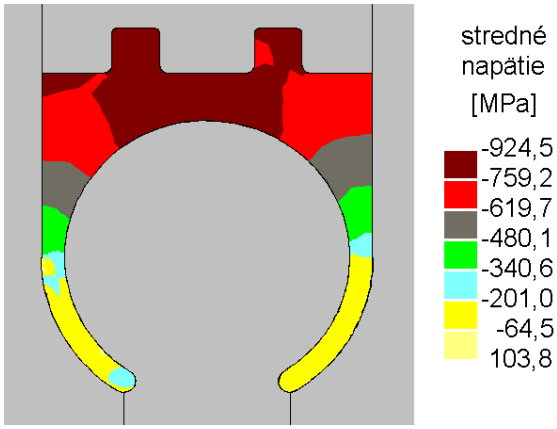


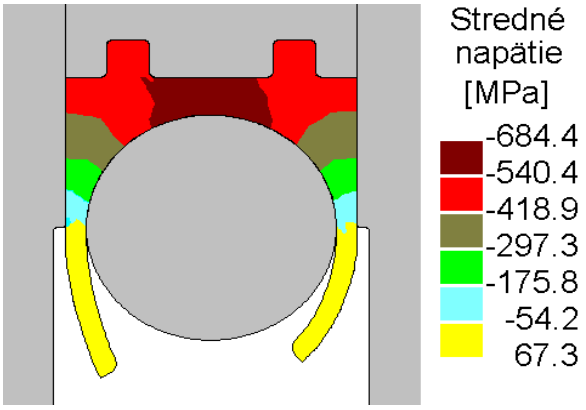
Figure 35: Simulation of the forging process of the "U"-shape semiproduct.



a) old shape C-pad



b) new shape C-pad



c) U shape semiproduct

Figure 36: Comparison of the mean stress in the forged material using the different forging processes.

10.3 Pad Precision

On about 100 C–pads all dimensions $A - E$ (see Fig 37) were measured.

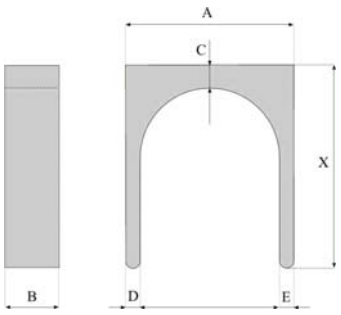


Figure 37: Dimensions measured for comparison.

It was found, that all dimensions are within the tolerance of $\pm 0.02mm$. The most critical dimension is the thickness of the pad base C, which depends on the damping of the cutter. The result is shown in Fig. 38. Of 110 measured pads 85% have dimension C within $\pm 0.02mm$.

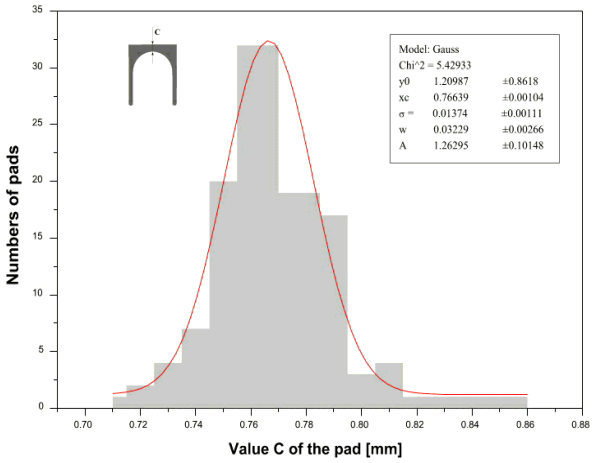


Figure 38: Precision of pad production.

The second step – cutting – and third step – bending – are performed with a precision better then $0.02mm$.

10.4 Positioning and Fixing of the Pads to the Motherboard.

Several methods of pad positioning and fixing to the motherboard have been discussed.

10.4.1 Leg–to–hole Method.

On the bottom side of the pad there are two tiny legs ($0.5mm$ long). The legs are fixed to holes in the motherboard. The precision of hole position is $\pm 0.02mm$, which results in the positioning of the pads with the same precision. The free volume between the square legs and the round holes is filled by a conductive glue.

The following problems are expected:

- the conductive glue is too rigid
- to ensure the same amount of glue for each fixing is not simple
- if there is too much glue, neighbouring pads may have an electrical connection

10.4.2 Glueing

It is assumed that the pads are glued to the motherboard using a positioning tool (Fig. 39), which enables high precision positioning. A positioning tool for 6×16 pads ($80 \times 60mm$) has been produced. The motherboard is fixed to the base of the tool via 4 positioning holes in the motherboard. The tool has 6 high precision segment pegs, to which C–pads are wired–up. The segment pegs can be moved in the movable prism, which can be positioned with the necessary precision ($\pm 0.02mm$) relative to the motherboard. Both fast and conductive glues are given to different parts of the pad bottom. Then the movable prism with 6 pads is lowered and the pads are glued to the motherboard. The distance from the previous row of pads is ensured by the $0.5mm$ thick spacer, which is taken off after fixing . The positioning precision is of the order of $0.02mm$. There is a possibility of using this method also for larger motherboards e.g. to glue a row with 18 pads at once.

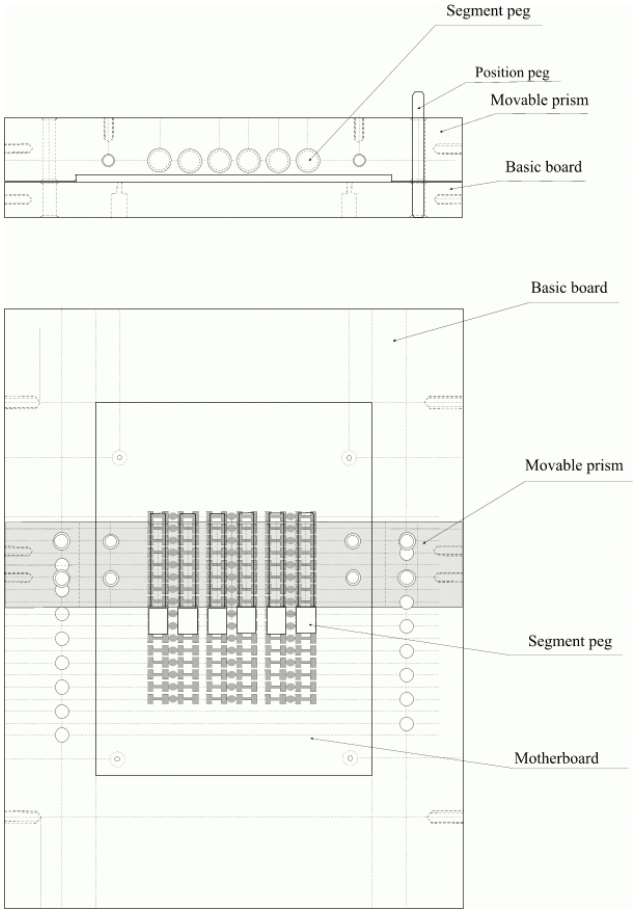


Figure 39: Positioning tool.

10.4.3 Soldering (Bonding)

To the bottom of the pad a thin layer of gold can be sputtered. Then it is possible to solder the pad to the motherboard using the positioning tool. The SMD technology of soldering

may be used. Another possibility of pad positioning is to produce two small holes in the bottom of the pad. Small $Ga - In$ spheres could then be put on the motherboard and then fixing is provided by a bump–bonding method (see Fig. 40).

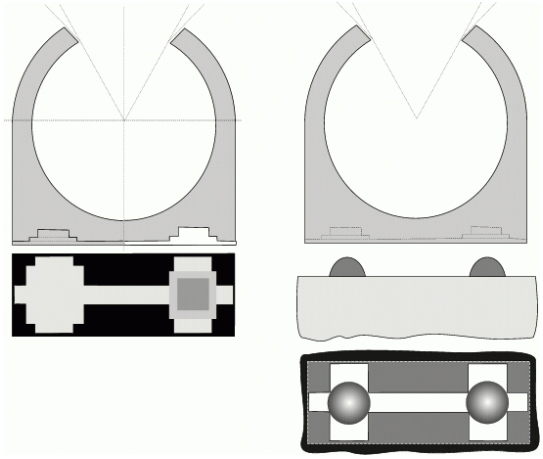


Figure 40: Soldering and bonding methods.

10.5 Gating Strips

Between two lines of C–pads gating strips are positioned. The shape of these strips fits the outer shape of the C–pads (Fig 41). Such a structure is self–supporting and the gating strips are positioned with high precision.

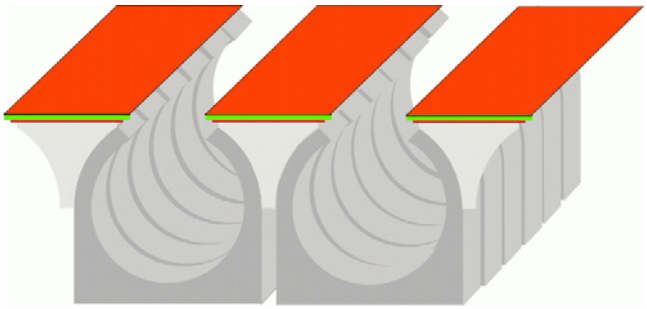


Figure 41: Gating strips.

The gating strips are produced by pouring epoxy resin into the form shown in Figure (42). The radius of the rods is equal to the outer radius of the C–pads. A copper strip is placed on top.

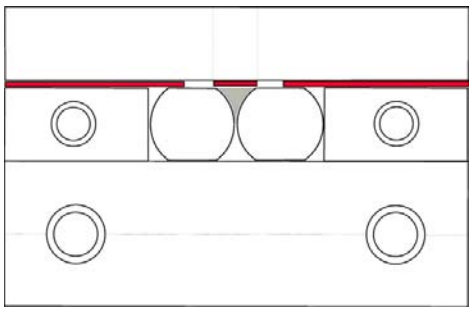


Figure 42: Form for the production of gating strips.

There is a possibility to produce a two level self–supporting structure with the gating grid on top and a grounded strip underneath. A scheme of the full structure is shown in Figure 43.

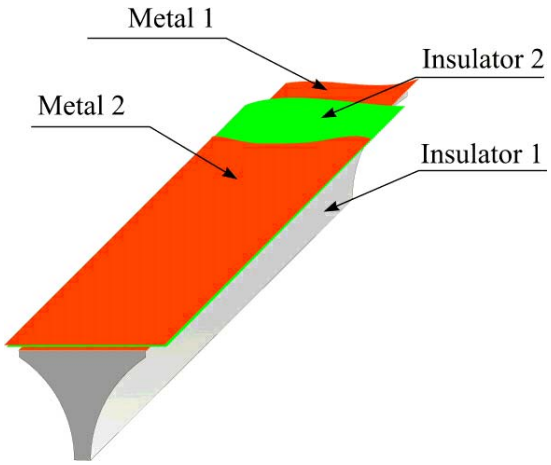


Figure 43: Two-layer gating strip.

10.6 Conclusions

The method for C–pad production from Aluminum with a precision better then $0.02mm$ and production speed suitable for a large–scale production has been developed. There is still room for further optimisation of the method for the ALICE TPC.

11 Bench Tests CERN

11.1 Pad Response Function (PRF)

In preparation of the RCC prototype several high precision measurements have been performed to determine the width of the PRF for the specific wire pad geometry of the RCC. It has to be mentioned that the natural PRF is only determined by the charge coupling of the electrons/ion to the pads while the reconstructed PRF is dependent also on the sampling i.e. the chosen pad width. The pad width in our test measurements however was small compared to the width of the natural PRF and therefore the intrinsic error of measurement due to undersampling can be neglected. Furthermore an alpha source was used which ensures a repetitive homogenious high ionization deposit with a minimum of

fluctuations. Angular wire/pad effects were minimized by using a trigger counter to select particles that were emitted from the source parallel to the readout plane. Figure 44 shows the fit of the PRF with the Gatti, Endo and Gauss - function. Applying a Gaussian fit to the data measured with the RCC structure (ring-radius of 3 mm) a sigma (PRF) of 2.0 mm was obtained.

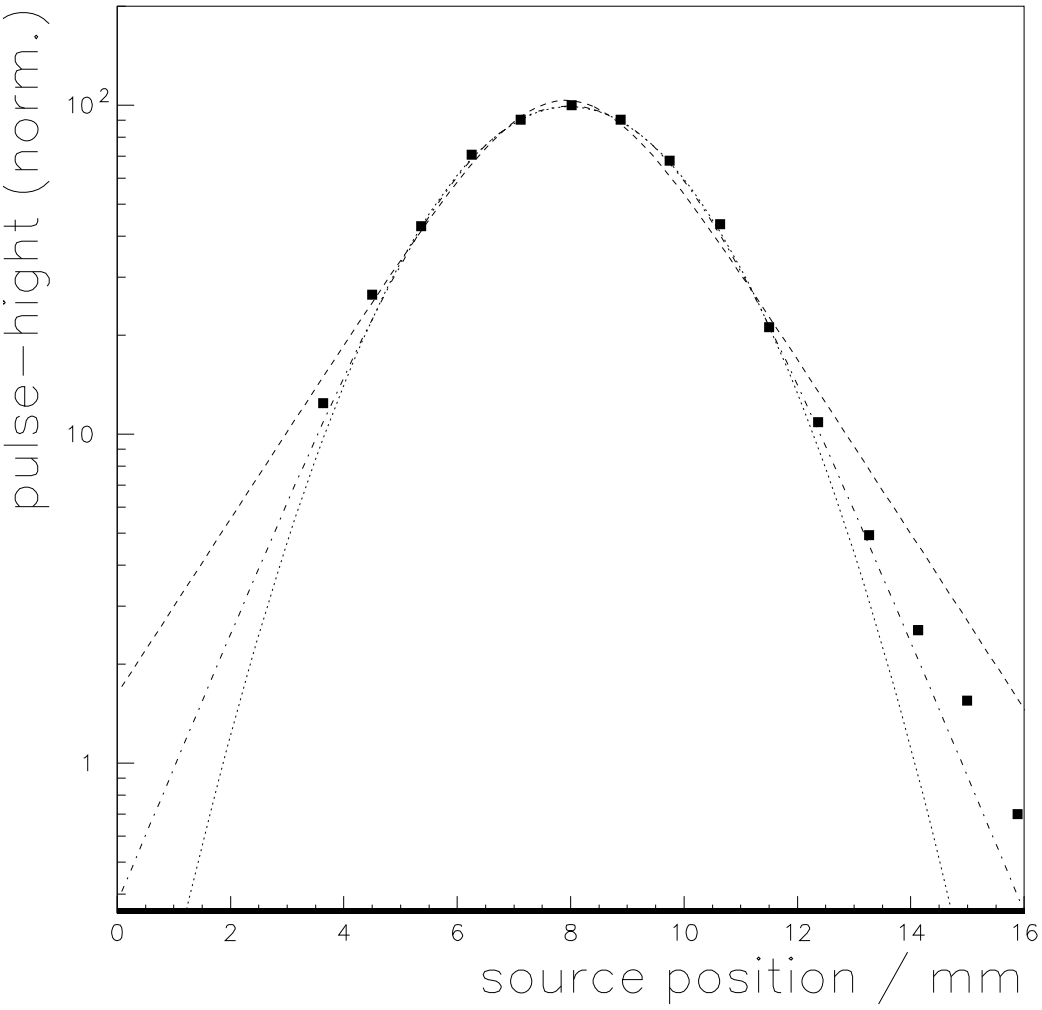


Figure 44: Pad response function of the ring-cathode chamber.

The smallest residuals were obtained with the Gatti function which might be explained by the larger number of degrees of freedom compared to Gauss and Endo. As a result of different measurements the width of the measured PRF in case of the RCC is approx. 75 % of the radius of the cathode ring.

More details about the measurement with the small prototype TPC can be found in ref. [13].

11.2 Gating

11.2.1 Transmission for Electrons

The transmission for electrons of the gate structure depends on the offset voltage that is applied to the gating strips. The voltage setting for a given transparency which is defined

as the fraction of electrons that arrive on the amplification wires depends on the drift field strength. The higher the drift field the higher the offset voltage has to be chosen.

For the gate transmission measurements of the RCC (fig. 45) a β-source was glued to the mylar window of the field cage. The current in the sense wire circuit was measured as function of the gate-offset voltage for different drift field strength. It has to be mentioned that the drift field strength was kept for safety reasons far below the 400 V/cm which are necessary for the operation of the ALICE TPC.

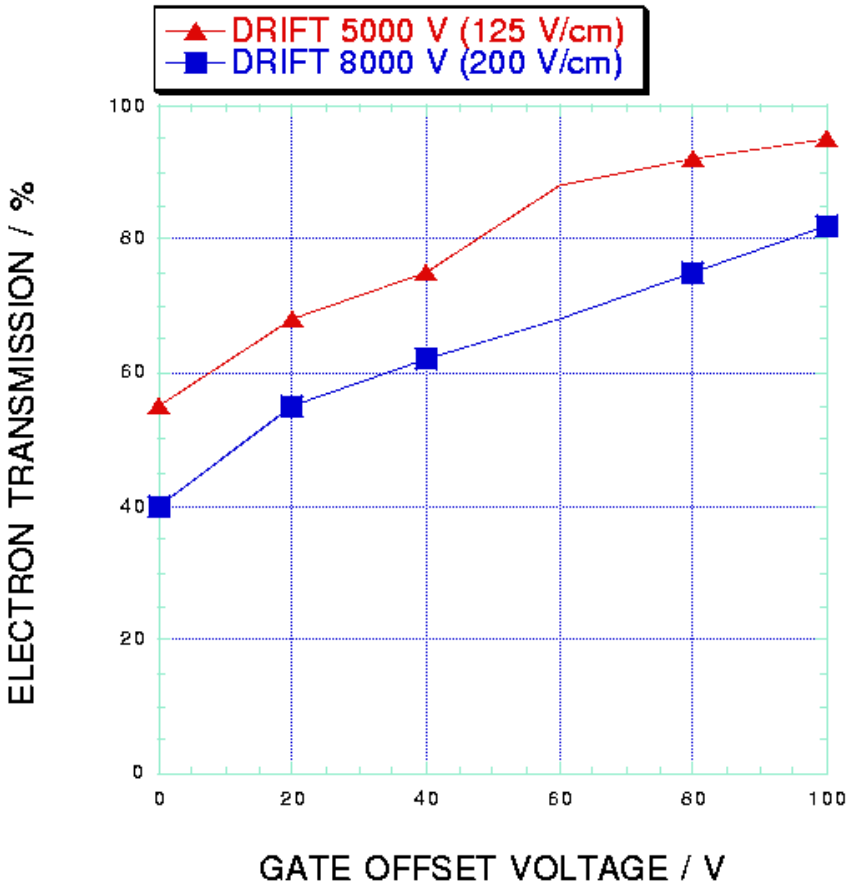


Figure 45: Measurements of gate transmission as function of offset voltage for two different drift field settings.

11.2.2 Closing Characteristics for Electrons

The closing characteristic of the gating structure for electrons was measured experimentally with a β source and with the Lead beam. As in the previous chapter the current in the sense wire circuit was measured as function of δ V (bias voltage) for different offset voltages and drift fields (fig. 46).

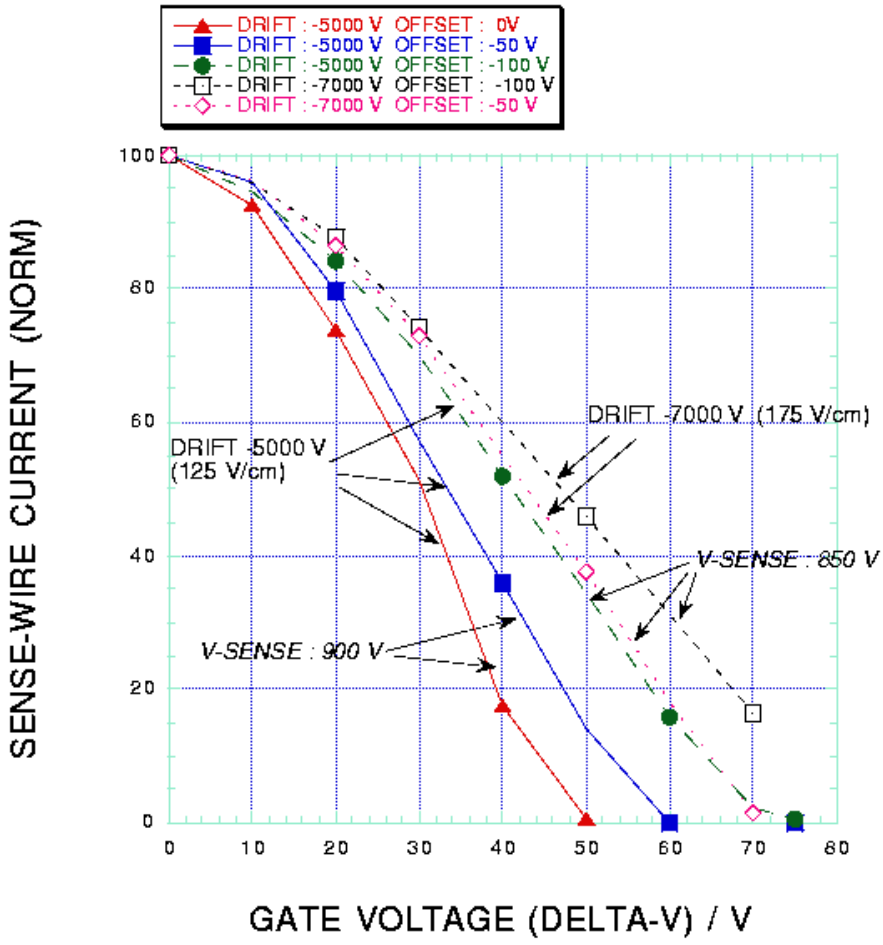


Figure 46: Closing characteristics for electrons as function of δ V (bias voltage) for different drift fields and sense wires voltages.

11.2.3 Dynamic Test of the Gating Structure

In the normal operation of a TPC the gate is switched by a pulser between the open and close states. This switching is done in a time interval of 1 to 2 μs and induces signals on the pads/preamps. To minimize the amplitude and duration of the induced signals, the capacitive coupling of the gate strips to the pads has to be kept as small as possible. Furthermore the tuning of the pulser by exact synchronization of the positive and negative slopes of the respective pulses is mandatory.

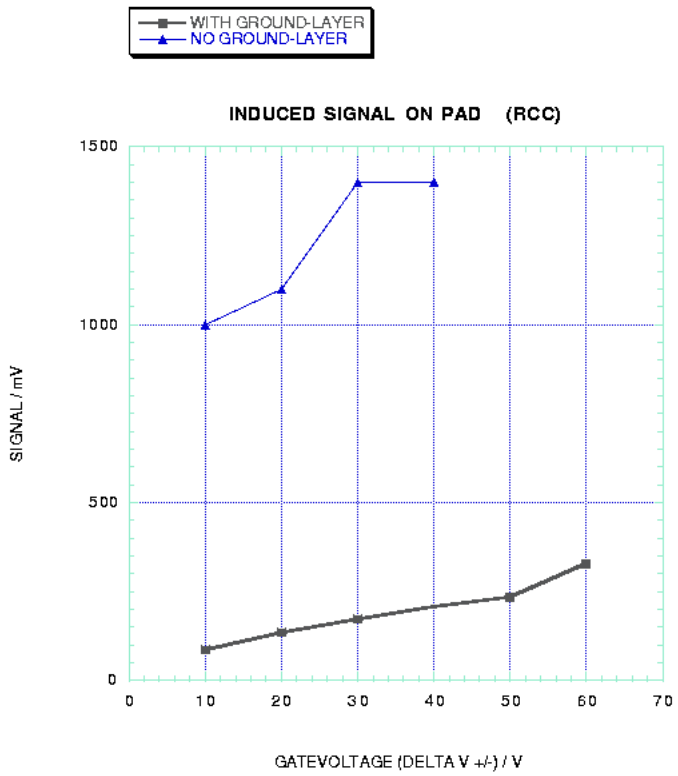


Figure 47: Induced signal on the pads of asmall RCC prototype as function of δ V (bias voltage) for a single gating strip and with the additional ground strip.

From fig. 47 it can be concluded that the induced signal can be reduced by more than a factor of 10 by introducing an additional ground layer isolated from the gate strip by a layer of Vetronite. The gate element that was used for the RCC has a total capacity of 0.5 nF/m. The total capacity is then about 6 nF, roughly the same as the classical wire chambers of NA49. In principle the thickness of the insulator can be increased to several 100 μ to achieve a further reduction of the capacity and thus the induced signal.

12 Bench Tests Bratislava

12.1 Chamber design

For detailed studies and further development of the RCC readout a small test chamber has been built . It allows to study a variety of both static and dynamic properties of the readout.

The chamber design is shown in figures 48 and 49. It consists of the drift space and the readout part.

The drift space is made from two printed circuit boards ($3 \times 5cm$) with metallic strips (thickness of a strip $1.5mm$, spacing $2mm$). The strips (6) are connected to the resistor chain ($10M\Omega$ between strips) and a high voltage supply. As a result a homogeneous

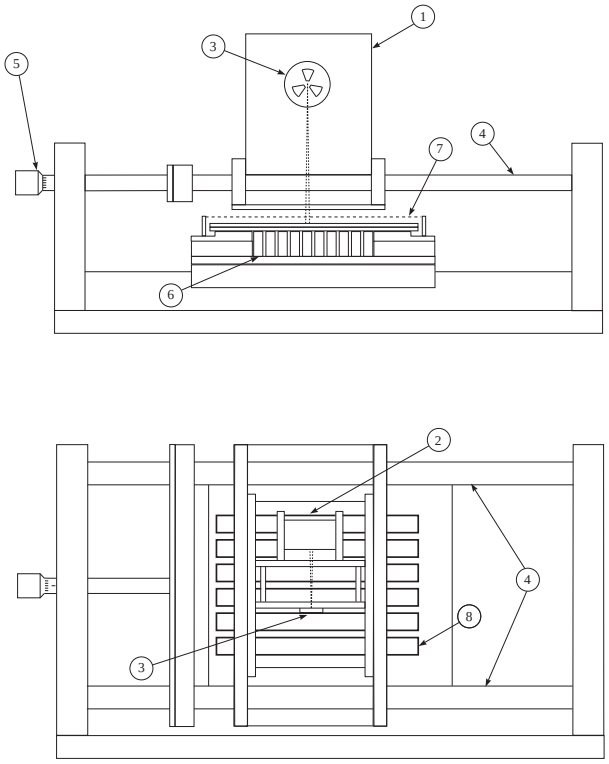


Figure 48: Vertical and horizontal cross section of the test chamber.

electric drift field is created. Ionization is induced by a collimated α source placed in the upper part of the drift space (3). An ^{241}Am source with $E_\alpha = 5.5MeV$ (effective range in Ar about $2.5cm$) has been used. To be able to trigger on α tracks perpendicular to the electric field, a small proportional counter has been placed at the wall of the drift space, opposite to the α source (2). To allow movements of the drift space along the anode wires, it is put on a carrier, moving on thin ceramic rods (4). It is possible to use also a ^{55}Fe source.

The readout part of the chamber is situated in its lower part. There are two rows, each consisting of 12 pads (here one pad means three C – shaped elements connected electrically together). The elements are connected to the printed circuit board using conductive epoxy glue. The thickness of a pad (=element) is $3mm$, its inner radius $6mm$, the opening angle of each element is $45°$, the length of a pad (three elements) is $21mm$. Each pad is connected to a separate preamplifier.

The anode wires are made of $20\mu m$ diameter Gold–covered Tungsten. Each anode wire is connected to a separate preamplifier.

The gating strips have been made from Kapton with a $80\mu m$ copper layer. The strip width is $4.75mm$. In order to allow a study of the gating properties, neighbouring strips are connected to two independent HV supplies.

The readout is electrically shielded from the drift space using a shielding mesh (7). The aim of the mesh is to simulate an electric field in an (almost) infinite structure (see figure 48).

For comparison a test chamber with a classical pad geometry has been built. Standard rectangular pads have been etched on a printed circuit board (pad size $6 \times 42mm$ and a pad pitch $6.5mm$). The sense-field wire grid is placed $3mm$ from the pad plane (the anode wires have $20\mu m$ diameter and are made from gold covered Tungsten, the cathode wires have $100\mu m$ diameter and are made from Beryllium bronze). The classical pad readout can be mounted inside the same drift space and gas box as the RCC readout (see figure 48).

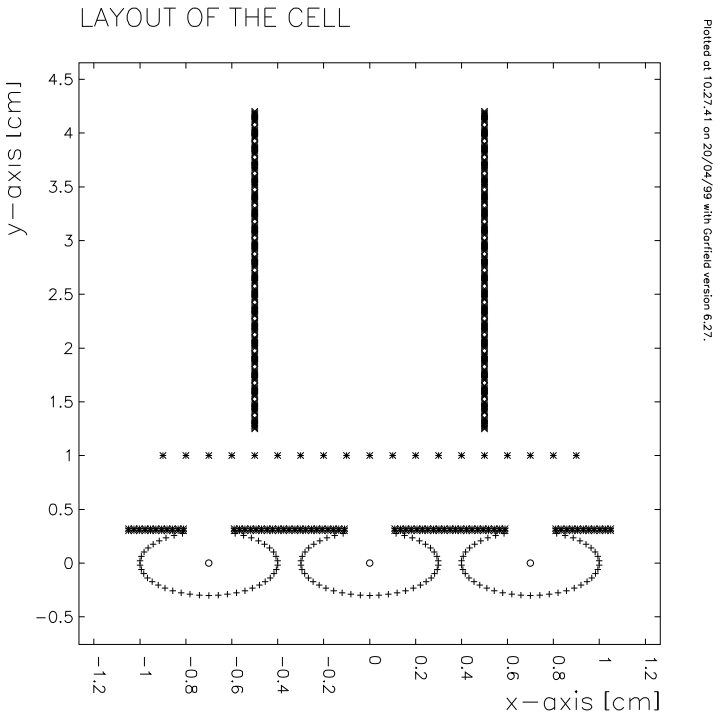


Figure 49: Test chamber geometry.

For all measurements standard $Ar + CH_4$ mixture $(90 : 10)$ was used.

12.2 Electronics

There are 6 independent HV supplies connected to the chamber using gas-tight BNC connectors. (One each for drift space, decoupling mesh, anode wires of the readout, anode wire of triggering chamber, two for gating strips.) Both anodes and pads are connected to charge-sensitive preamplifiers (input impedance 1000Ω, anode preamplifier gain $0.55mV/pC$, pad preamplifier with positive input signal and gain $0.65mV/pC$). The preamplifiers are inside the gas box, connected to fast linear amplifiers via gas–tight BNC connectors. The signals form the amplifiers are analysed using a 12 channel ADC LeCroy $2249A$ connected to a computer. For precise measurements, the ADC was replaced by a fast digital $500MHz$ oscilloscope $HP54616B$ with a sampling frequency of $2GHz$.

12.3 Static Characteristics

12.3.1 Charge Collection in RCC

When the RCC is in the open state, part of charge is collected on the sense wires, part on the gating strips. To achieve a reasonable transparency of the structure, it is necessary to put the gating strips to negative potential with respect to the pads (see figure 50).

This leads to a "repulsion" of the electron drift lines from the strips and to their focusing towards the sense wires. This effect is visible in figure 50. By changing the voltage of the gating strips it is possible to increase the amount of collected charge.

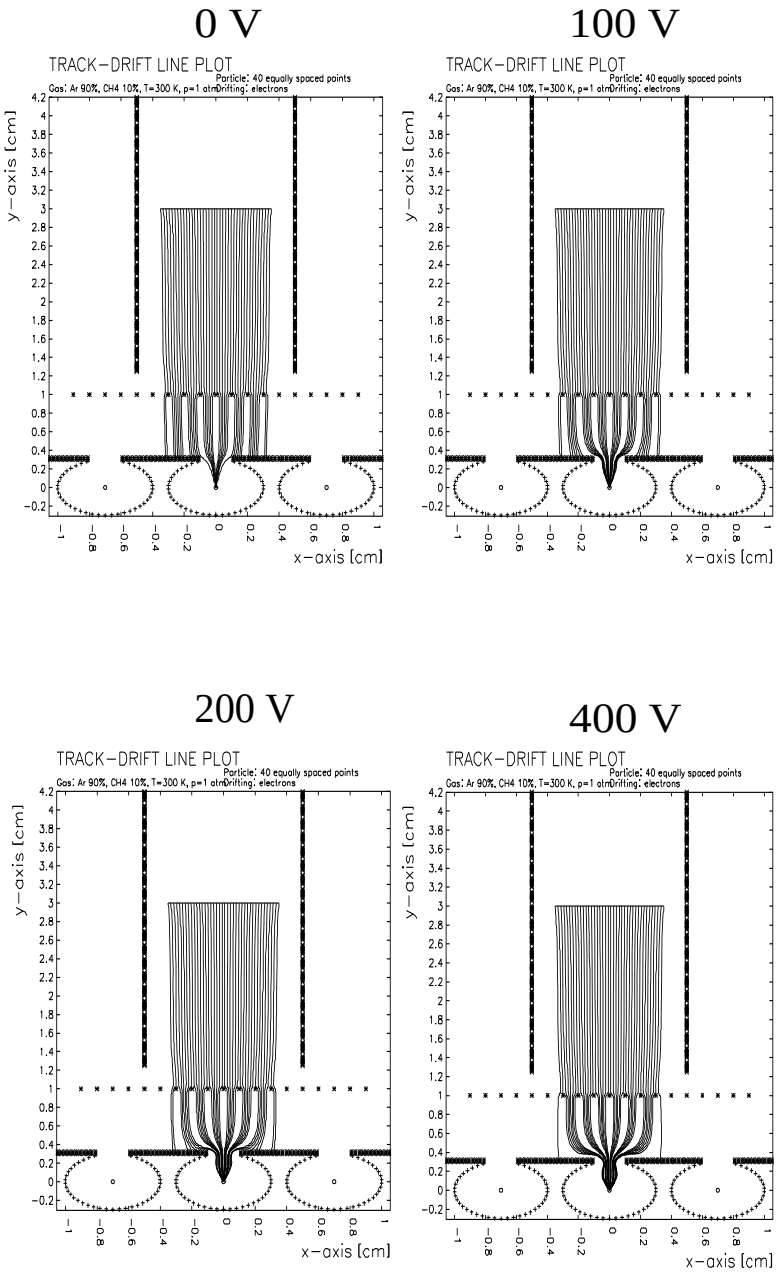


Figure 50: Focusing of the electron drift lines as a function of the offset voltage on the gating strips.

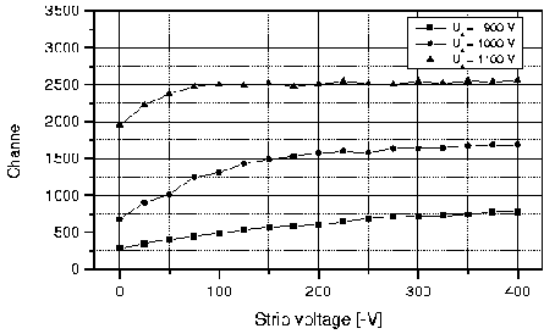


Figure 51: Signal amplitude as function of strip voltage for three different anode voltage settings.

The charge collection in the RCC depends on the geometry and the working potential. An important geometrical parameter is the C-pad opening (the bigger the opening, the easier it is to focus the field lines) and the gating strip distance. For a fixed geometry the fraction of charge collected by the anode depends on anode voltage, strip voltage and drift field.

In figure 51 one can see the result of the optimisation of the focusing voltage for our geometry (45° opening, $4.75mm$ strip width). During the measurement, a constant drift field of $200V/cm$ was kept between shielding mesh and gating strips. It is visible that for $U_A = 1000V$ in order to achieve 80% collection efficiency (which is the estimated efficiency of the Frisch grid in a standard TPC), the focusing voltage should be about $-100V$ or below.

12.3.2 Gating Properties for RCC

It is possible to close the proportional chamber of the TPC by applying different voltages to neighbouring strips . This has two purposes firstly electrons from the primary ionization are collected on the strips and not on the anodes thus decreasing discharge probability and ageing. Secondly positive ions created during gas amplification do not enter the drift space, thus diminishing problems caused by positive charge built up.

In this paragraph the data on closing properties for electrons are presented. All measurements have been done in a static regime.

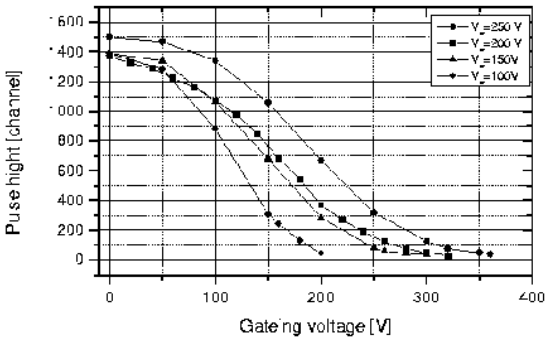


Figure 52: Signal amplitude on the anode wires as function of the gating voltage for four different focusing voltages.

In figure 52 one can see the results of such a measurement done for $V_A = 1000V$ with a drift voltage (just below the shielding mesh) of about $200V/cm$ for various focusing voltages. Assuming a focusing voltage $V_{G0} = 100V$ the necessary gating voltage is approximately $200V$. (That means $\pm 100V$ with respect to the focusing voltage.)

We think it is necessary to study the gating properties of this structure in more detail. It would be interesting to measure the gating efficiency for positive ions, a parameter crucial for the ALICE TPC. Assuming a gas gain of the order of 10^4, the gating efficiency for positive ions should be better than 10^{-4}. To study the gating efficiency with such an accuracy would require a very good precision of the measurement.

The gas gain for anode voltages around $1000V$ has been estimated to be around 100 (in $ArCH_4$). The necessity to work with moderate gas gains is caused by the use of an α source with its big specific ionization. In Alice the gas gain will be about two orders of magnitude larger.

12.4 Dynamic Characteristics

12.4.1 Pad–to–wire Signal Coupling.

An important parameter in favour of the RCC readout in comparison with a standard readout is the good signal–to–pad coupling. While in planar geometry only part of charge is induced on the pads, C–pads surround anodes almost completely, thus collecting a bigger part of the induced signal.

The amplitudes of anode and cathode signals have been compared in our geometry. There were two methods of measurement used.

- Seven pads were connected together. An α source was collimated to irradiate the pad in the middle. In this case the ratio of pad to anode signal is 89% with an estimated error of $\pm 5\%$.

- One pad was connected to a preamplifier and a collimated source was moved in steps of $0.5mm$. The results (after correction for different preamplifier gains) are shown on figure 53. After summing–up all measurements and division by the pad pitch one obtains a pad to anode ratio of $85 \pm 5\%$.

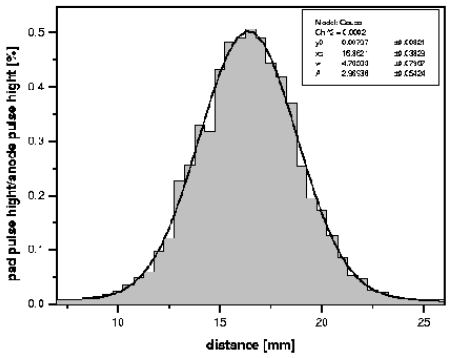


Figure 53: Fraction of signal on one pad as a function of the position of the α source.

The results of measurements have been compared with GARFIELD simulations. In order to eliminate possible sources of error during signal evaluation in GARFIELD [1], a simple electrostatic approach using the weighting field method has been used.

The current induced on a conductor (kept at constant potential) by the movement of free charge can be expressed using Gauss law of reciprocity in the form

$$I_{ind}(t) = -q\overrightarrow{v}.\overrightarrow{E_W} \tag{1}$$

Here $\overrightarrow{v}$ is the ion drift velocity and $\overrightarrow{E_W}$ the weighting field intensity. In the case of a signal induced on the anode, the weighting field is the field in the detector without free charges but with potential $U = 1V$ at the anode and $U = 0V$ at all other electrodes (pads, Frisch grid, ...). In the case of a signal induced on a pad, the weighting field is defined by the potential $U = 1V$ on the pad and $U = 0V$ on all other electrodes. As $\overrightarrow{v}$ is the real ion drift velocity, not depending on where the signal is taken from, it is possible to express the ratio between anode and cathode signals in the form:

$$\frac{I_C}{I_A} = \frac{E_{WC}}{E_{WA}} \tag{2}$$

as the ratio of weighting field magnitudes.

To evaluate the weighting fields, GARFIELD has been used. Anode and cathode weighting fields have been calculated in the C-pad geometry and classical geometry. To evaluate the ratio in equation (2), the intensities of the weighting fields in close proximity to the anode have been used. [2]

In the case of the RCC, the ratios of cathode signal to anode signal height have been estimated to around 92%, whereas in standard chambers with pad readout [3] it is around 30%. This number corresponds to the signal induced on the whole pad plane, the signal induced on a padrow is obviously smaller.

These estimates are in good agreement with the measurements (taking into account the precision of both measurement and simulation).

In a standard pad readout TPC geometry, a large fraction of the signal is induced on the field wires which interleave the anode wires. It is possible to increase the fraction of charge induced on the pad plane by using only sense wires. In that case the simulation predicts the signal on the pad plane to be around 50% of the anode signal.(The induced signal is equally shared between pad plane and Frisch grid.) However one should be careful, omitting field wires may lead to a nonuniform electric field below the Frisch grid which

[1] The signal shape is a rather complex function of the electric field, gas properties (ion drift velocities, in complex mixtures ion recharging) and electronics parameters.

[2] $20\mu m$ above anode surface

[3] In calculations, the Na49 VTPC1 chamber geometry has been used.

may lead to a decrease of the Frisch grid transparency in comparison with the standard TPC geometry. Clearly, these effects should be studied in more detail.

13 Lead Beam Tests

For the Lead beam test the prototype TPC was mounted downstream of the Vertex II magnet of NA49 directly in front of the MTPCR (fig. 54). It was mounted on rails such that it could be moved in and out of the beam.

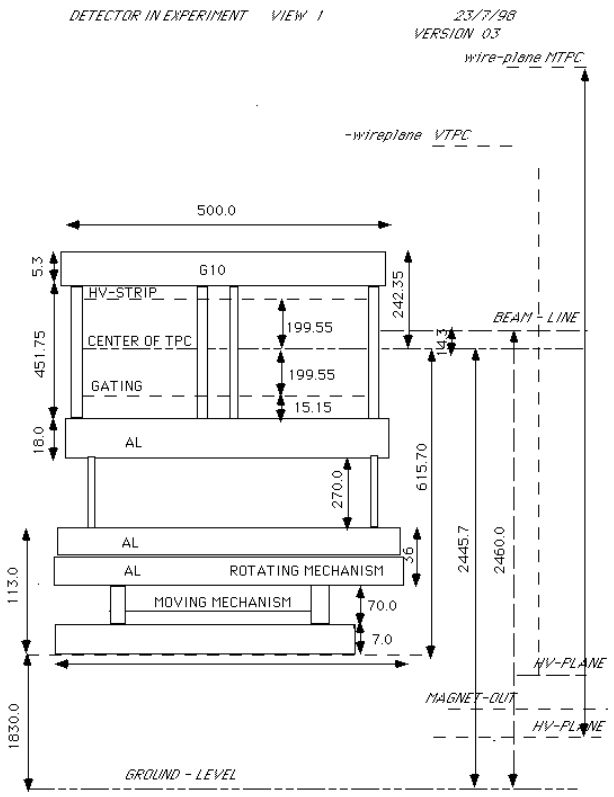


Figure 54: Position of the prototype TPC in the plane perpendicular to the beam axis.

13.1 Gating

For the gating of the new chamber a standard NA49 gate pulser was used [14]. All voltages could be regulated independently by external power supplies. The effect of the gating pulser on the readout is shown in fig. 55. It shows the averaged signal from 90 pads of padrow 11. A relatively large signal is induced on the rings with an amplitude of about half of the dynamic range available (peak value). After about 1 μs the signal is down to about 20 ADC counts above the pedestal level. Keeping in mind that the gate signal is subtracted as part of the pedestal subtraction procedure one looses less than 1 μs (10 time bins) in total. After about 4 μs the baseline is fully stabilized again.

No attempts have been made to fine tune the gate pulser. It is expected that this would lead to a significant improvement.

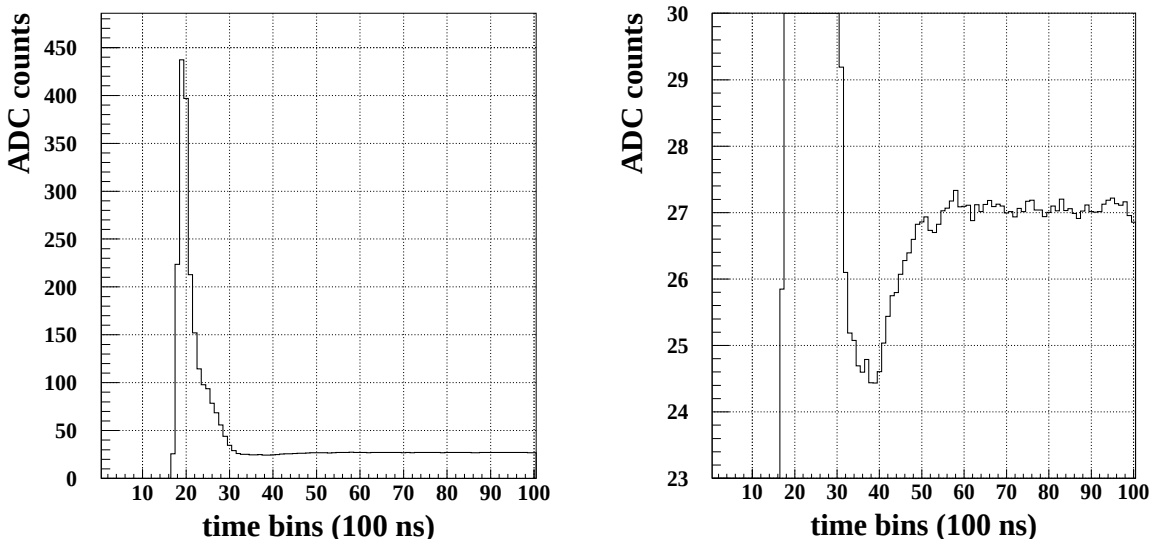


Figure 55: Signal induced by the gate pulser. Left side: full scale, right side: expanded scale. No pedestal subtraction has been applied.

13.2 Gas Gain

The gas gain was measured by injection of radioactive ^{83}Kr gas. By counting the events above threshold and measuring the current in the sense wire circuit the gas gain can be computed [12]. The sense wire voltage was set to 1100 V in order to produce sufficiently large amplitudes for minimum ionizing particles (see fig. 57). The assumed gate transmission is estimated to 60%. A gas gain of $\tilde{5}{\cdot}10^4$ is estimated. This is roughly expected given the rather low sensitivity of 4 mV/fC of the PASA chip.

13.3 Pedestals

After complete installation of the system in the experimental area and connection to the DAQ system pedestal data (empty events, gating pulser on) were taken. The result is shown in fig. 56. The noise behaved as expected and was measured to be around 1.2 ADC counts. The baseline shows a very small systematic tendency to drop over the readout time by about 0.1 ADC counts.

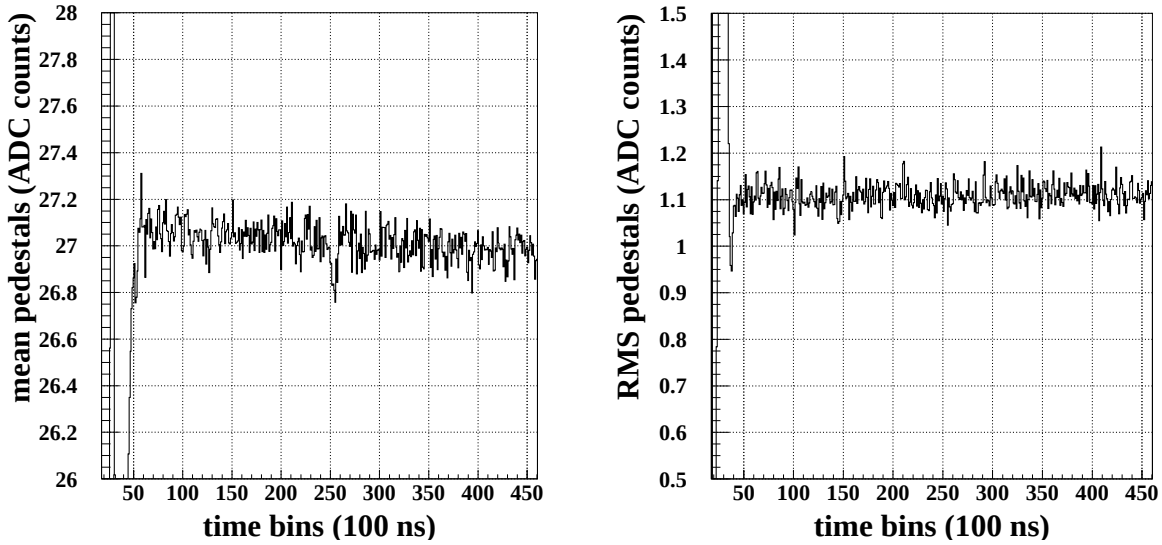


Figure 56: Mean value and RMS of pedestals as function of time bin. Average over pads from row 10.

13.4 Baseline Stability

A qualitative impression of the baseline stability can be obtained from inspection of the signals of a single pad with the online monitor. An example is shown in fig. 57.

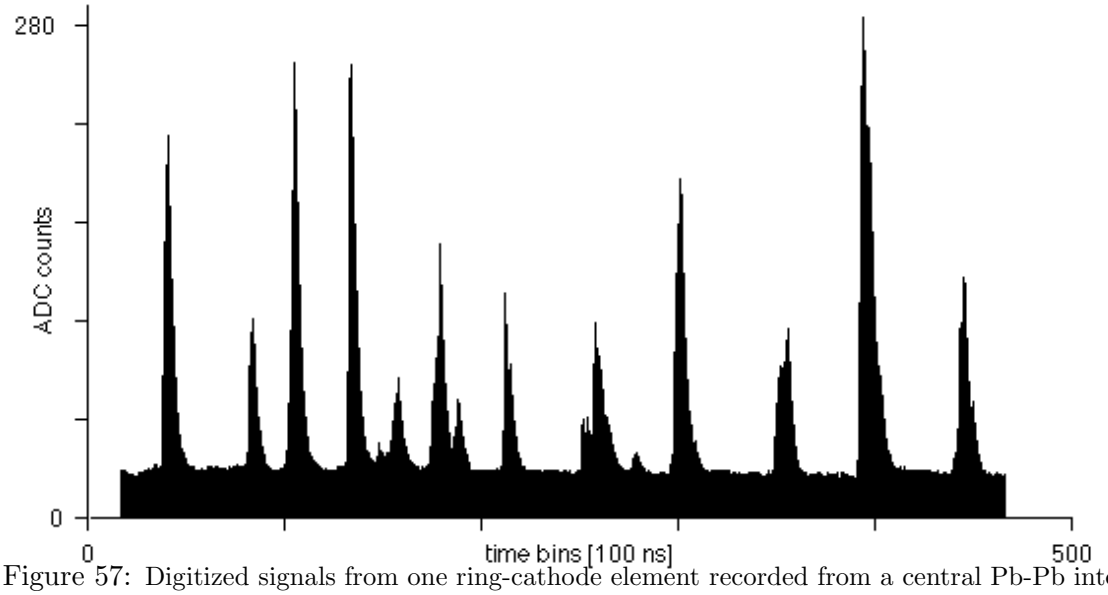


Figure 57: Digitized signals from one ring-cathode element recorded from a central Pb-Pb interaction (40 GeV/nucleon).

For a more quantitative evaluation of the baseline stability with sub-permille resolution the ^{83}Kr dataset was used. Pb-Pb interactions could not be used for this purpose due to the rather high occupancy and the tendency to have more than one hit during the readout time.

The following procedure was used: a peakfinder was run, marking the position and amplitude of all peaks (definition: local maximum over 3 time bins). In the next step it was checked that for 20 timebins before and 380 time bins after no other peak was found. For

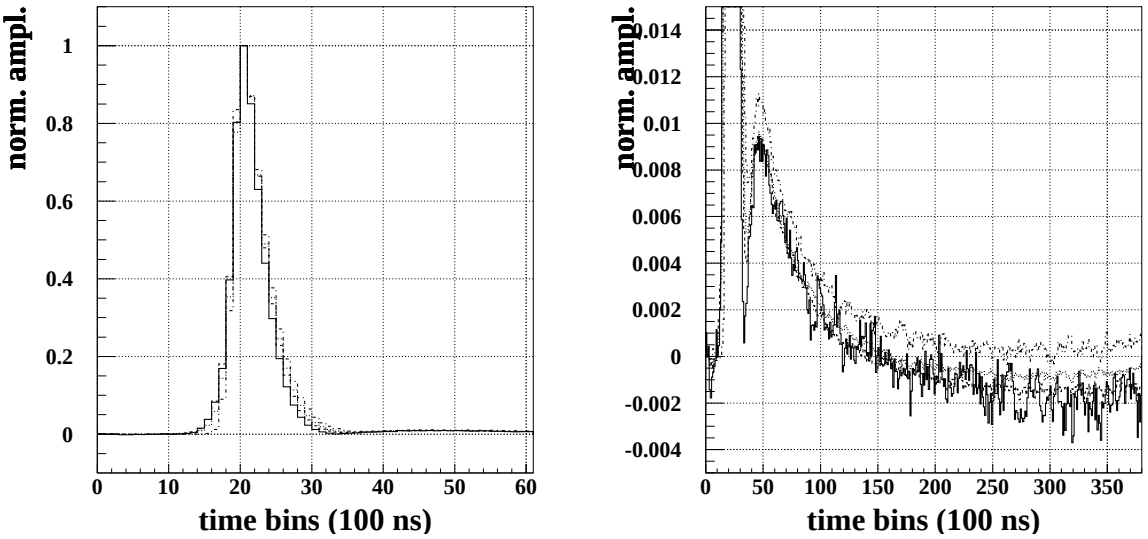


Figure 58: Average signal from ^{83}Kr normalized to the maximum. 4 different amplitude ranges are shown: 100 - 200, 200 - 400, 400 - 700, > 700 ADC counts. Left side: full scale, right side: expanded scale.

the peaks fulfilling this criterion the neighbouring pads where checked for matching signals i.e. clusters were identified. After alignment to the time bin with the maximum signal (time bin 20) the complete history i.e. all 400 time bins were filled into four histograms depending on the amplitude of the cluster maximum. Separate histograms were used depending whether the signal came from the pad containing the cluster maximum or its neighbours. Results are shown in figure 58 where the amplitudes are normalized to the maximum of the signal. No difference between cluster maximum and neighbouring pads could be observed.

A significant nonlinearity is observed for the overshoot following the signal as well as the long range undershoot. For large amplitudes the undershoot even vanishes.

There seems to be an indication that the baseline moves upward again after reaching a minimum. With the available statistics though it is not possible to see this unambigously.

For a more quantitative evaluation the relative amplitudes (normalized to the peak amplitude) in the region of the positive overshoot (around time bin 40) are plotted in fig. 59 as function of the mean peak amplitude in the four amplitude intervals analyzed. The same is done for the region between time bin 300 to 350. A possible explanation of the nonlinear behaviour could be the increasing spread of the ion cloud around the sense wire depending on the primary ionization. This is suggested by a comparison to the results of the simulation in fig. 72. The question whether the ion cloud really develops differently for different primary charges cannot be answered by the simulation at present. It should be pointed out that in classical TPCs this effect is basically not visible due to the limited dynamic range of the readout electronics (8 bits).

Another way of looking at baseline stability and cross talk effects was tried by looking at pads in the neighbourhood of the ones with the actual signal. Since the position of the Lead beam is fixed within a σ of 0.3 mm it is possible to average over many events to increase the sensitivity. In fig. 60 the baseline is shown for padrows 9 to 10 during the relevant time interval. One observes some cross talk producing negative and positive signals. The peak amplitude is always around 600 ADC counts. It should be noted that due to the fact that the Lead beam passes across all rows cross talk effects between rows cannot be observed this way.

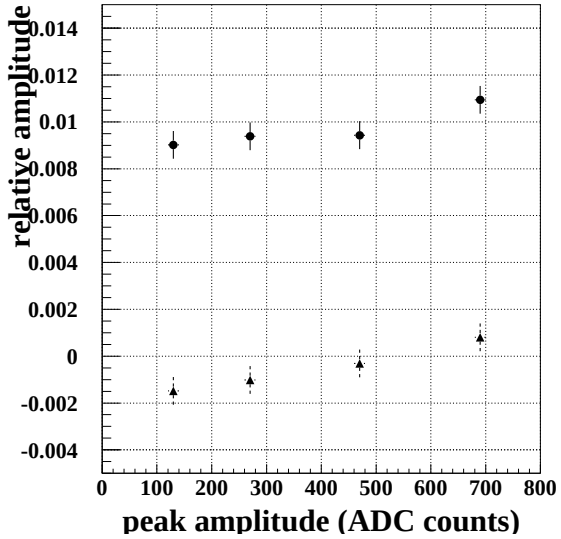


Figure 59: Relative baselineshift taken from two regions of fig. 58: around time bin 40 (dots) and around time bin 340 (triangles).

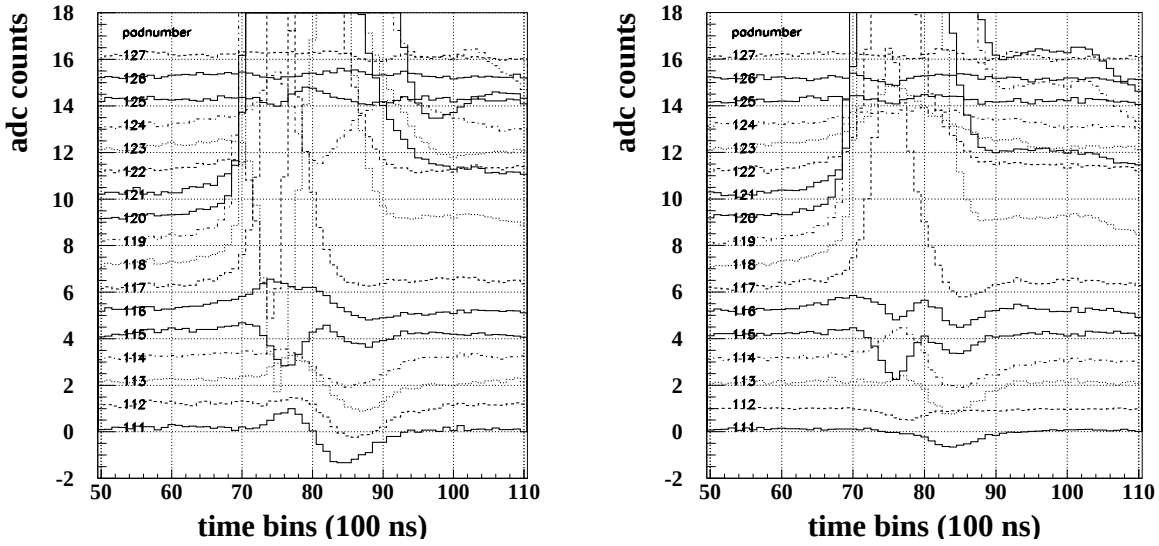


Figure 60: Baselines for pads of row 9 (left side) and row 10 (right side) from the region where the Lead beam crosses the chamber

For this purpose a look at the ^{83}Kr data showed for small amplitudes a significant negative undershoot (fig. 61). This effect is visible in padrows 9 and 12 only, not in rows 10 and 11. Further analysis showed that this is due to a coupling effect inside the 4-channel chip which connects 2 pads each from adjacent padrows to the same chip. Small amplitudes in a given padrow are mostly due to the fact that the ionizing electron is located close to the edge of a padrow and thus most of the signal is in padrows 10 and 11 but the adjacent padrow shows the strong negative cross talk. Since in the analysis procedure the peaks are aligned (see above) the relative position in time does not show the true situation.

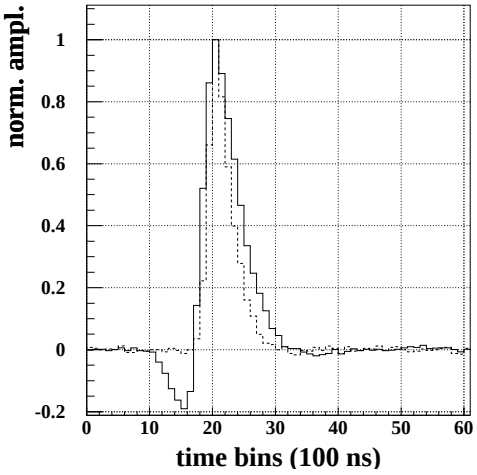


Figure 61: Comparison of signals from ^{83}Kr from row 9/12 (solid line) to rows 10/11 (dashed line) for small amplitudes (< 100 ADC counts).

13.5 Pad Response Function

For the determination of the pad response function (PRF) the dataset with the Lead beam passing through the chamber and operating at a reduced voltage of 600V at the sense wires was used. The width of the Pb beam was found to be σ=0.3 mm in x (pad) direction. In addition an offline cut on the position of 0.5 mm width was applied. In fig. 62 the result is shown. The width of a Gaussioan fit yields σ = 2.28 mm. The reason for the slight asymmetry on the right side is not clear. A possible explanation could be cross talk effects as observed in fig. 60.

The width corresponds to the bench measurement using an Alpha source (see chapter 11).

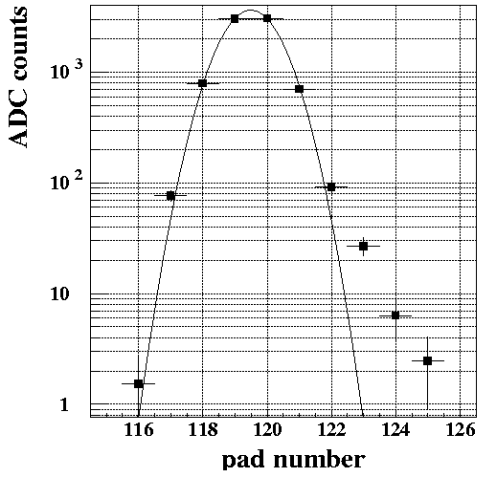


Figure 62: Pad response function of the ring-cathode chamber (σ = 2.28 mm).

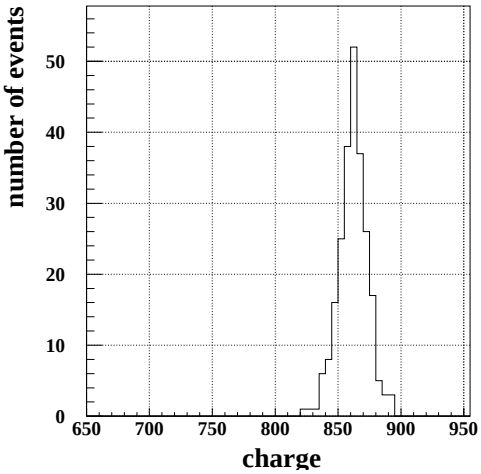


Figure 63: Charge resolution for Lead ions (σ = 1.4 %).

13.6 dE/dx Resolution

The dataset taken with Lead beam passing directly through the chamber at reduced sense wire voltage (600 V) has also been used to test for amplitude stability. Due to the good definition of the Lead beam (σ = 0.3mm), only few pads contribute to the signal. The total charge was determined by adding up all time bins above threshold for all pads showing a signal. It was found that due to cooling problems the amplitude changed over the duration of this particular run by about 4%. For the final distribution of energy loss in one padrow (fig. 63) only the stable part of the run has been taken. The resolution obtained is δ(dE/dx)/dE/dx = 1.4%. Considering the huge primary electron statistics and the electronics noise one would expect about a factor 5 better resolution.

In order to investigate the limits of dE/dx resolution the correlation between rows was analyzed using pedestal data (no signal). The charge information is derived by summing up all time bins and pads normally containing a beam signal (8 pads, 19 time bins). A strong correlation is observed (64).

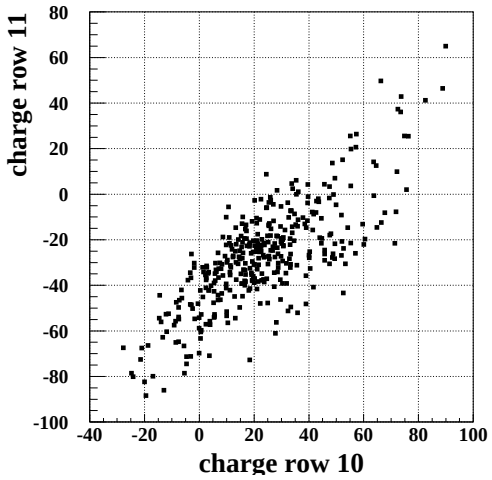


Figure 64: Correlation between pedestal charge (all amplitudes summed up over 4 pads with 7 time bins each) of 2 different pad rows.

The reason for this seems to be a correlated variation of the pedestal level across the detector. All channels seem to fluctuate synchronously i.e. the correlations between different rows or groups of pads within a row show the same pattern. From the width of the summed signal and its scaling with the number of bins summed the RMS of this fluctuation is estimated to 0.75 ADC counts whereas the random electronics noise is 0.97 ADC counts. Both add up quadratically to the observed 1.2 ADC counts per time bin.

14 Simulation of the RCC Response

A detailed simulation of the behaviour of the RCC has been performed using GARFIELD. The results together with a comparison to various other wire chamber geometries (NA49, CERES, STAR) can be found in ref. [15]. In the following the main results referring to the RCC are summarized.

For the simulation the RCC has been modelled as closely as possible to the actual design. Each sense wire is surrounded by an grounded octagonal cathode, called ring cathode, with an inner radius of 3 mm of which one panel is absent. Electrons approach the wire through the missing panel, ions can escape through this opening. The avalanche wires have a diameter of 20 μm and are at a potential of 1100 V. A Neon 90%, CO2 10% gas mixture is assumed.

14.1 Gate Transparency

A gating structure is located between the openings in the octagonal cathodes. The gating structure consists of an alternating sequence of strips at a potential of typically 0 V and at -200 V (-100 V offset). These strips are mounted on a 270 micron thick G10 layer, on the bottom side of which an earthed strip is glued, of the same dimensions as the gating strips. The assembly is held in place by a triangular G10 structure. The G10 components of the gating structure have been modelled using a material with a dielectric constant of 3.6 wrt vacuum. The triangular piece is not shown in the figures, but is present in the model. All conductors are assumed to be perfect. The field in the model has been computed assuming periodic boundary conditions on the "left" and "right", grounding on the "bottom" and a constant potential at 5 cm "above" the wire which ensures a drift field of 185 V/cm at 1 cm and more from the wire.

14.1.1 Transparency for Electrons

In fig. 65 the drift lines for electrons are shown for the open state (about 90% transmission) and the closed state.

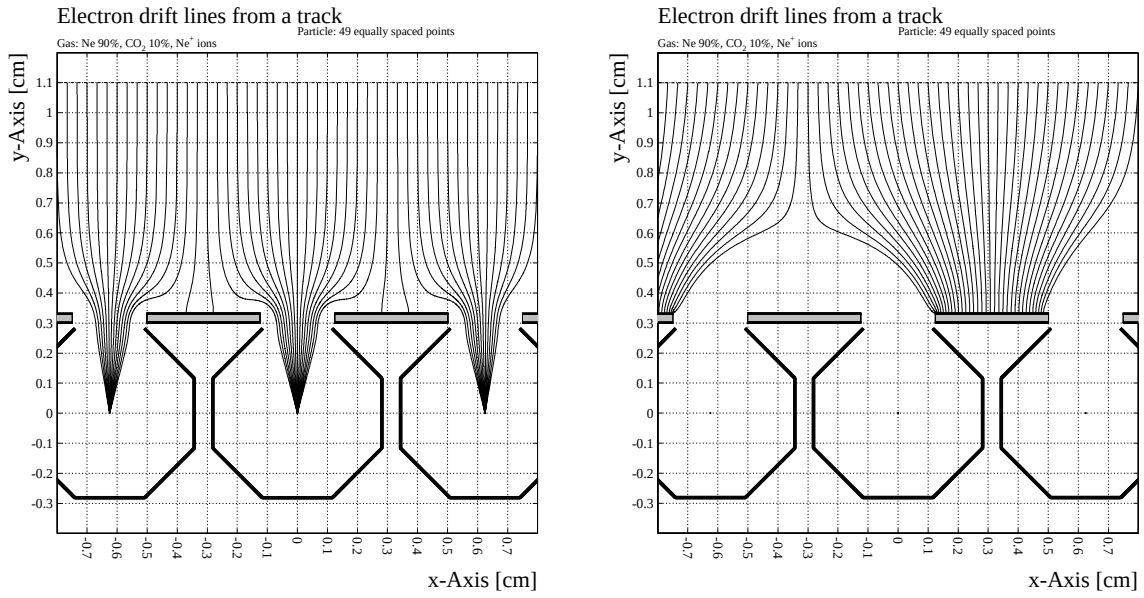


Figure 65: Garfield simulation of the RCC with gate open (left) and gate closed (right), offset voltage = -100 V, delta-V = 100V, drift filed = 185 V/cm.

Assuming a wire potential of 850 V and a drift field of 125 V/cm, the transparency in

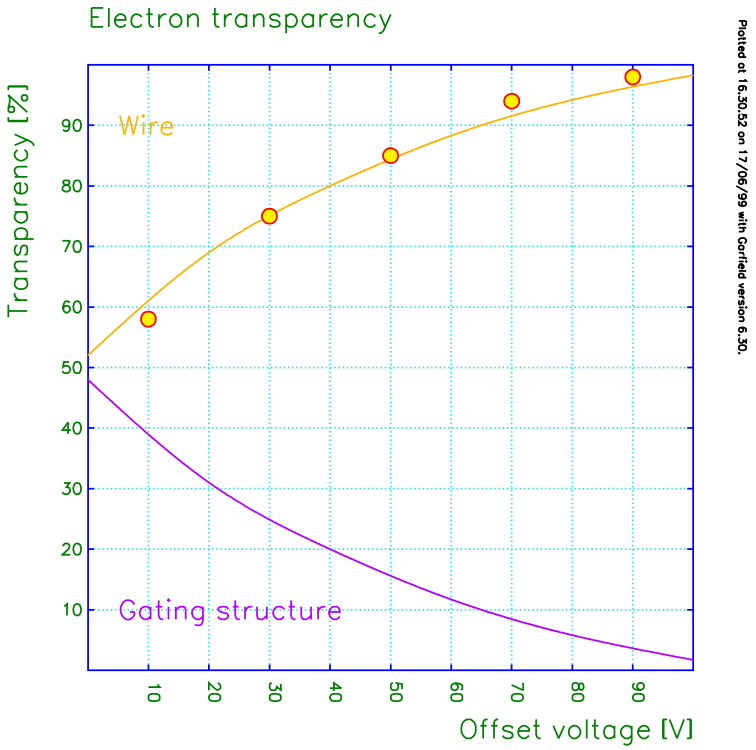


Figure 66: Transparency for electrons as function of the offset voltage compared to measurement (full dots).

the open gate state varies from 50 % at an offset potential of 0 V to nearly 100 % for an offset of -100 V. This agrees well with measurements of this quantity.

Measurements have been performed for a sense wire voltage of 900 V, a drift field of 125 V/cm and an offset of -50 V. Although the measured acceptance as function of the offset voltage agrees well with the calculations (fig. 66), the agreement for bias variations is poor (fig. 67 right side). The data do however agree reasonably well with calculations performed for an offset of -30 V (fig. 67 left side) .

14.1.2 Transparency for Ions

Ions go, under most angles, to the ring cathode. These are the ions produced under angles that do not face the ring cathode exit. Since the gating field barely penetrates into this part of the ring, the angular acceptance for the ring cathode is virtually constant.

When the gate is fully open, the ions produced in a 30^0 sector facing the ring cathode exit, will enter the drift zone. When the gate is fully closed, this sector vanishes. The gating structure is reached by some ions irrespective of the state of the gate - when the gate is open, slightly under 20^0 give access to the gating electrodes, and angular range that increases to nearly 45^0 when the gate is closed (fig. 68) .

Since the gating efficiency for ions depends strongly on the assumptions about the initial distributuion of the ion cloud around the sense wires no predictions on the permille level can be made. In addition diffusion effects start to play an important role, also hard to calculate with the required precision.

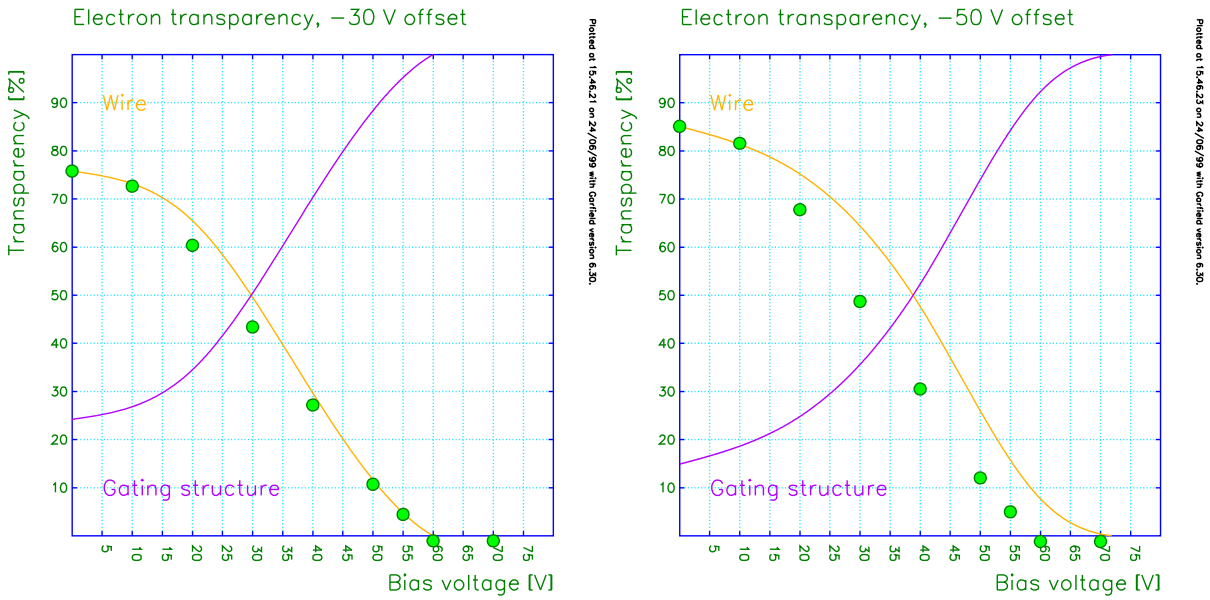


Figure 67: Transparency for electrons compared to measurement (full dots) as function of bias volage (δ V) for two settings of the offset voltage. Left side: -30V , right side: -50 V.

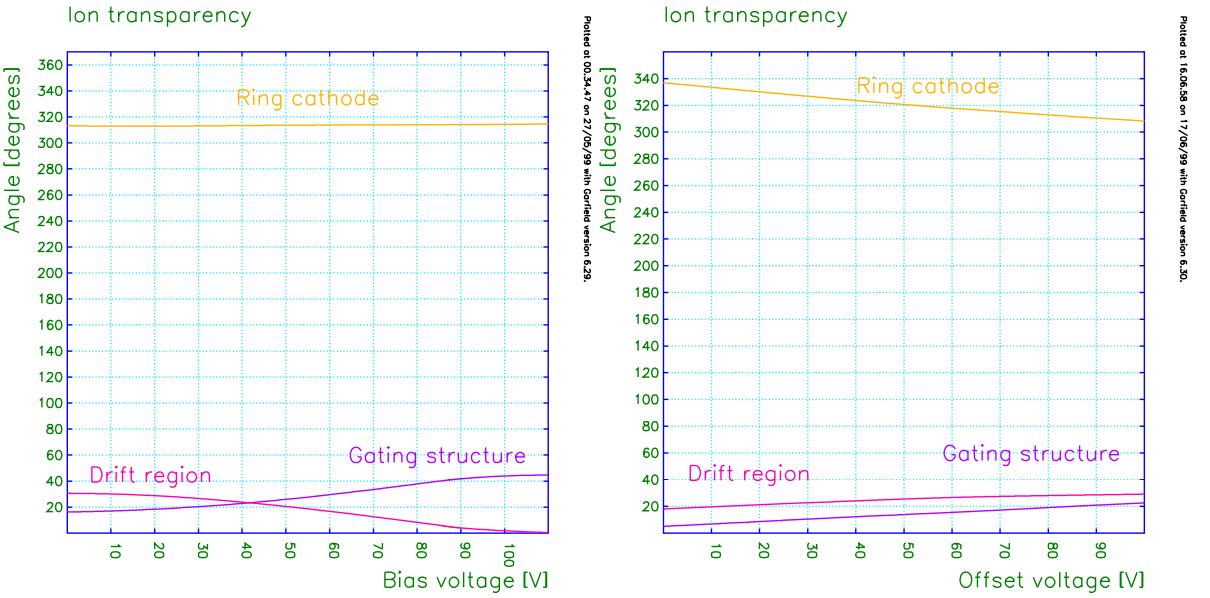


Figure 68: Angular region around the sense wire from where positive ions end up on the gating grid, the ring-cathode or the drift volume respectively as function of bias voltage (left side) and offset voltage (right side).

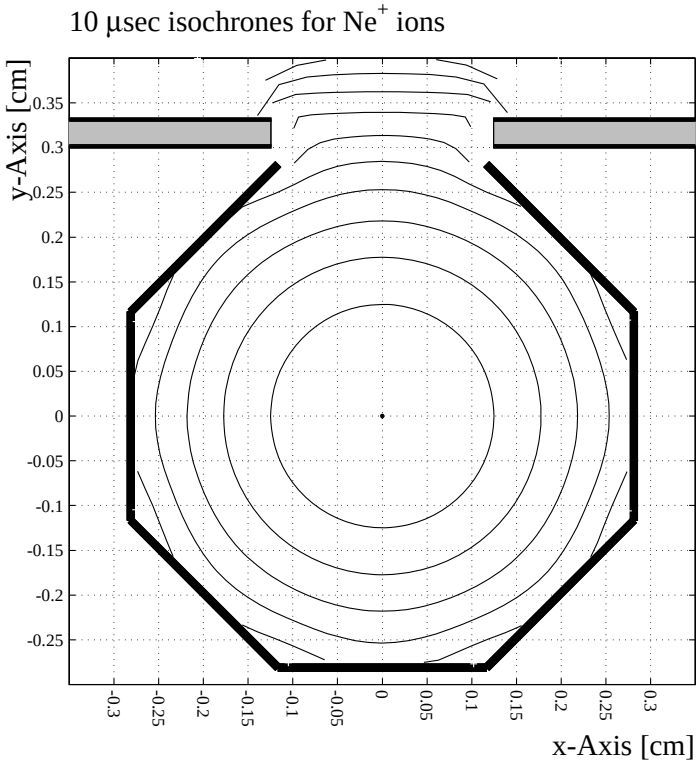


Figure 69: Isochrones (10 μs) for drift of positive ions away from the sense wire. (offset voltage = -100V, δ V = 0 V, drift field = 185 V/cm
).

14.2 Isochrony

Neon ions need 45-55 μs to reach the ring cathode, while carbon dioxide ions need 25-35 μs. Once past the gate, ions enter the drift region where the field is of the same order of 180 V/cm, with drift velocities of only 800 cm/sec. In fig. 69 lines of isochrony are shown for positive Ne ions.

The variation in drift path of electrons for the RCC is quite substantial. Some electrons enter the the cathode ring directly, others at first almost reach a gating electrode, drift back out, and finally enter the cathode. The isochrony is of order 250 ns when the gate is open. The gate setting has little influence on the drift time from a given point as can bee seen in fig. 70.

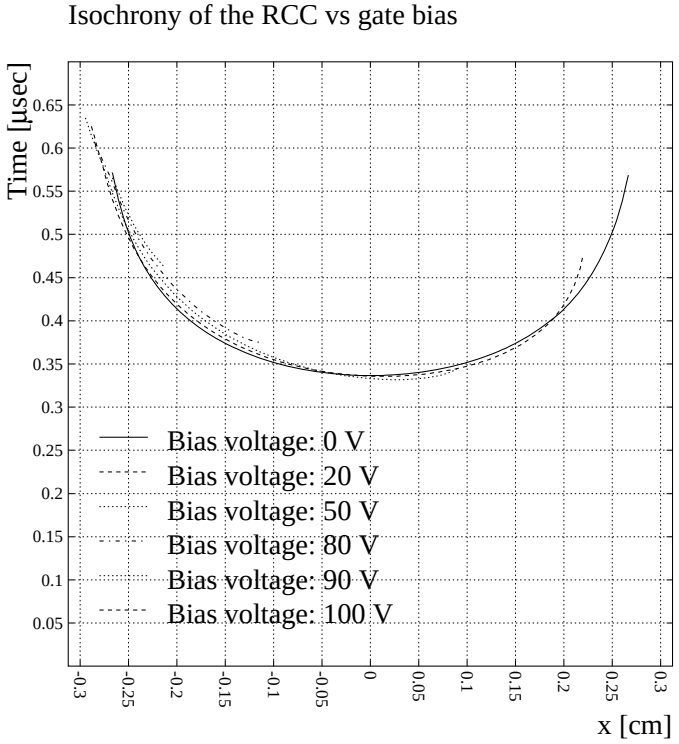


Figure 70: Arrival times of electrons at the sense wire for various gate bias voltages (δ V). The x-axis is perpendicular to the wire, see fig. 69)

For the solid line in figure 70 the transmission is about 90%. For other bias voltages part of the electrons go to the gating strip and never reach the wire. For this reason the curves are not symmetric any more.

14.3 Signal Shape

Signals induced in an electrode can be computed using the technique of the weighting field of the electrode. This field is multiplied with the velocity of the moving charge in order to obtain the current which is supplied by the HV supply in order to maintain a constant potential on the electrode. The weighting field therefore represents the effect on the electrode, that a charge moving in a certain direction has. Weighting fields are easy to compute: they are obtained by setting the voltage of the electrode that is read out to 1 V and all other electrodes to 0 V.

The weighting field for the ring cathode points away from the ring cathode and towards all other conductors (fig. 71). Ions that start from the wire and reach the ring cathode will, as a rule (there is a small region near the entrance) move in the direction of the weighting field, and hence induce unipolar signals on the ring cathode.

Since the ring cathode surrounds the avalanche almost entirely, the cathode collects the charge more efficiently than the classical TPC. In contrast, not all ionisation electrons reach the avalanche wire, some are lost on the gating structure.

In the absence of angular spread of the avalanche arond the sense wire , all ions return to the drift region. On the way out of the ring cathode, the weighting field changes orientation and the signal therefore changes sign. This happens after 17 μs. Approximately 65 μs after the ions have left the wire, they are at the exit of the ring cathode. There, they see a somewhat larger field and weighting field, hence induce a slightly larger current. When the ions are in the drift region, the weighting field from the ring cathode is largely shielded

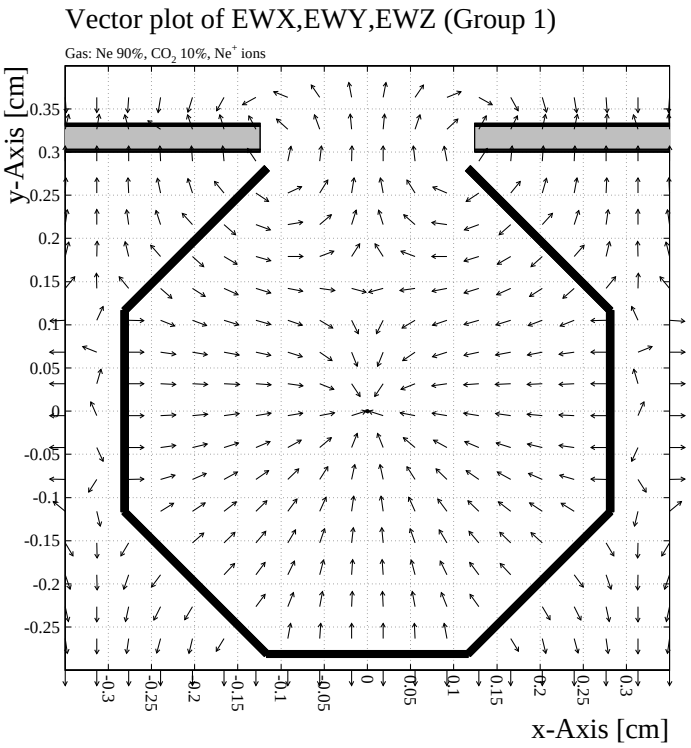


Figure 71: Weighting field of the RCC (Offset voltage = -100 V, δ V = 0 V, drift field = 185 V/cm).

by the gating structure, and also the ion velocity is small. Hence, the signal from ions in this region is very small:

Gradually increasing the angular spread, at first some ions will reach the gating structure, in the neighbourhood of which they accelerate, causing the appearance of a small negative spike. When the spread further increases, more and more ions will go to the ring cathode, inducing a unipolar signal. As a result, the undershoot diminishes. The result of these calculations are summarized in fig. 72.

14.4 Drift Field Variations

To ensure full transparency, the offset potential needs to be lowered when the drift field increases, so as to ensure that the entire gate electrode remains negatively charged. Gate transparency can be achieved up to drift fields comparable to the fields found near the entrance of the RCC, which are of the order of 2000-2500 V/cm for a sense wire voltage of 1100 V.

However, well before the gate can no longer be made transparent, the cathode rings start to become positively charged. For a sense wire potential of 1100 V, losses start to occur for drift fields from 550 V onwards and losses reach 20 % for a drift field of 900 V/cm (fig. 73).

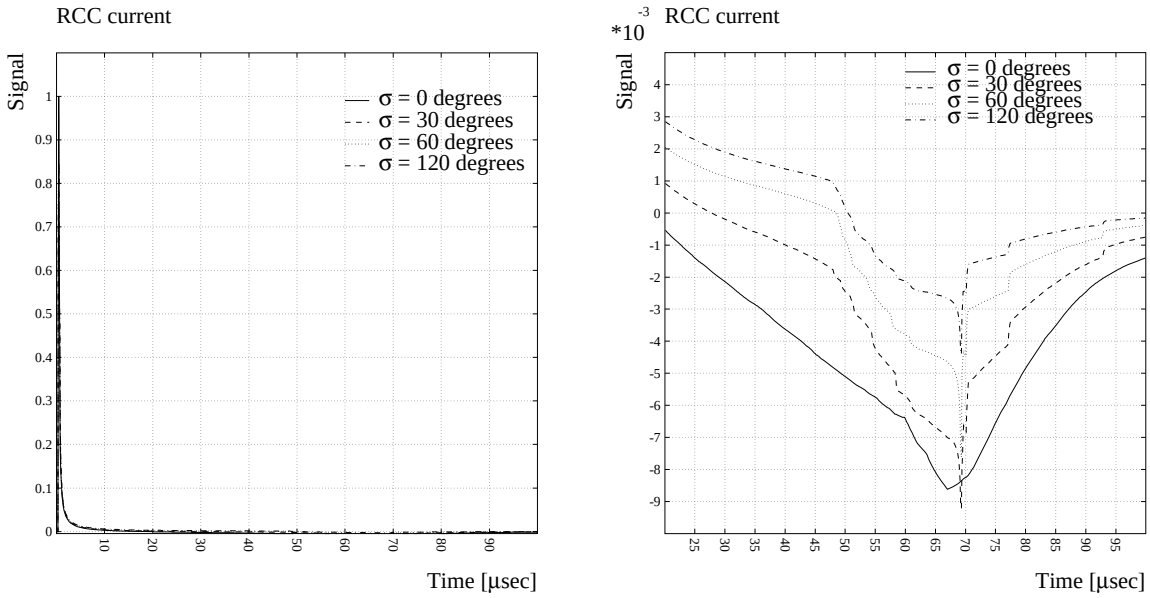


Figure 72: Normalized current signal induced on the ring-cathode for various assumptions about the spread of the avalanche around the sense wire. Left side: full scale, right side: expanded scale

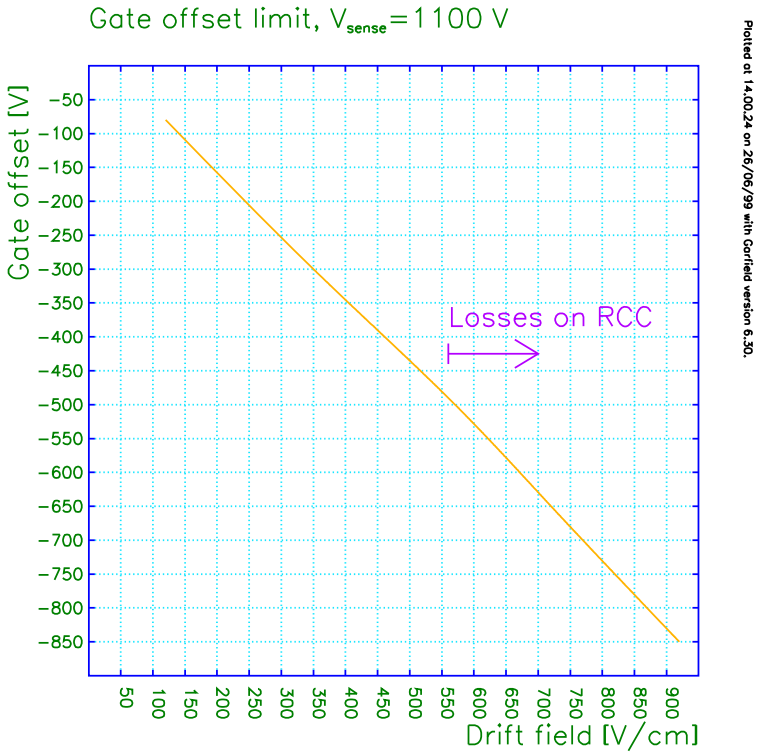


Figure 73: Dependence of gate voltage on drift field for a given sense wire voltage setting of 1100 V. The arrow indicates the regions where electrons are starting to be lost

15 Cost Estimates

In the following quotes for mass production of preamp/shaper chips and readout boards including the mounting of the dice and connection to ADC boards are listed.

15.1 Preamp/Shaper

Quote from ALCATEL for PASA chips produced by HARRIS and SdM from 1. 10. 1996:

It is based on 520 000 channels corresponding to 130 k PASA chips delivered over 2 years and packaged for surface mount assembly and tested (wafer tests and test of packaged product).

price/channel: 5,71 SFR

(not included: non-recurring engineering cost for design, prototyping, pre-production, external components (capacitors etc))

15.2 TAB

Quote from Dassault Electronique from 15. 12. 1997:

Is is based on 518 000 channels and on the design of the prototype (see fig. 4).

It comprises 900 motherboards (6 layer boards, size 11cm x 40cm) carrying 144 chips each and 8 daughterboards produced over a period of 2 years. The PASA chips are TAB mounted and the daughtercards connected by TAB Flex to motherboard (3 TAB Flex per daughterboard).

price/channel: 4,72 SFR

(not included in price: non-recurring engineering cost, PASA chips, capacitors, connectors on daughter cards, tests ILB and boards, mechanics, cooling)

16 Conclusions

The benchtests and in particular the Lead beam tests have shown that the system in general works quite well. In the following the weak and strong aspects of every component are briefly summarized.

- The **ring-cathodes** work according to expectation: the coupling of the signal is found to be around 90% i.e. about a factor 4 better than classical TPCs with field wires (NA49) and about a factor 2 better than TPCs without field wires (CERES, STAR).
  The **baseline shift** is smaller than in classical TPCs when operated with Ne/CO2 (NA49). Simulations suggest that a readout without field wires (CERES, STAR) though would be rather similar to the RCC. Unfortunately its baseline behaviour could not be measured over the full time range relevant for ALICE (100 μs) due to a limitation in the readout. From simulations a negative undershoot of around 5×10^{-3} is expected after 70 μs.
  The width of the **pad-response-function (PRF)** is as expected from the ring diameter and about appropriate for an application in ALICE. Ideally one would use a somewhat larger PRF of about 3 mm matching the expected clustersize given by diffusion.
  The position resolution could unfortunately not be determined in the tests.
  For the **mass production** of rings promising techniques have been developed. Clearly more studies are needed to evaluate the final production scheme.

- The new gating scheme using **gating strips** instead of a wire plane works in principle quite well. Its limits in terms of electron transmission could only be determined down to the percent level. The behaviour at the 10^{-4} level has to be known though for ALICE applications.
  The closing properties for positive ions have not been measured. From simulations it is concluded that for Ne/CO2 gas it is not possible to close the gate while the positive ions are still inside the ring cathode. Due to the high drift velocity the positive Neon ions pass the opening after around 70 μs. For Ar/CO2 gas the ion drift velocity is sufficiently small to allow closing the gate. A significant modification of the gating scheme would be required for the operation with Ne/CO2.

- The present iteration of the 4-channel **preamp/shaper** in bipolar technology worked to satisfaction. From the gas gain necessary to obtain reasonable signals it is clear though that its sensitivity is low (4mV/fC). Simply increasing the gain will not be of much help unless the noise can be kept at the same level as it is now. The present noise level matches ideally the sensitivity of the ADC. The observed rather asymmetric pulse shape with its long trailing slope can be a problem in a high track density environment.
  The **baseline stability** was found to be quite good. The positive overshoot peaking at about 2 μs after the signal can probabaly be improved by proper adjustment of the time constants to the actual operating conditions of the chamber. The nonlinearity of the overshoot and the subsequent slight undershoot as function of the amplitude is presently not completely understood but could be due to variations of the spread of the ion cloud around the sense wire.
  Same cross talk between the 4 channels has been observed which should be reduced in a next iteration.
  There seems to be a contribution to the noise coming from insufficient separation from the power supply line. The noise contribution from the buffer amplifiers is not

negligable but would not be present in a more realistic setup where all components of the electronics are mounted directly on the detector.
The question of **cooling** has not been tackled so far. It posed a serious problem for the tests. Blowing air against the multilayer board and the PASAs turned out not to be sufficient. A water cooling system either integrated into the multilayer board or attached directly to the PASA chips is clearly necessary.

- The **TAB** bonding of the PASA dice directly to the readout board could be demonstrated as a viable technology. It offers the possibility to do elaborate tests on the chip level and thus allows selection before installation.
  It is not clear on the other hand whether the price to be paid is justified. Standard technology using surface mount techniques should be compared in more detail.

- The **multilayer board** used to mount the cathode rings on the front side and the PASA dice on the backside was manufacutred with the required flatness and gas tightness. The question up to which dimensions this can be enlarged keeping the same tolerances has not been investigated.

- The **pico-coax** cables worked in the present configuration according to specification. For the future they are clearly not desirable. Due to the difficult mechanical handling their price is quite high. In addition the use of unipolar signals is problematic. For further development of a board carrying the ADC and the zero-suppression ASIC to be mounted directly on the detector it is desirable to use differential signals to connect to the PASA.

- The **direct digitization** using a commercial low power ADC showed no problems and can be regarded as a very attractive solution. If it is possible to use the power saving SLEEP mode of the ADC (which has not been tested so far) the power consumption is comparable to the readout scheme using analog storage before digitization (NA49).

- The **zero suppression** and **buffering** implemented in a FPGA has also proven to be a viable solution for ALICE. Further work will concentrate on the conversion into an ASIC.

- The **Digital Data Link (DDL)** in its basic functionality worked as advertised. In the VME environment unfortunately some problems showed up which could be clearly identified. It is therefore an attractive way for ALICE to transfer data from the detector front ends to the DAQ.

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