Off- and in-beam tests of Silicon-strip Detectors for the ALICE experiment at LHC

C. Suire, C. Kuhn, J. Baudot, J.P. Coffin, L. Arnold, D. Bonnet, M. Germain, G. Guillaume, F. Jundt, J.R. Lutz, A. Michalon, A. Tarchini.

Institut de Recherches Subatomiques-IReS - IN2P3/CNRS - ULP
BP28, F 67037 Strasbourg Cedex 02 - France

W. Dulinski

Laboratoire d'Electronique et de Physique des Systèmes Instrumentaux LEPSI -
IN2P3/CNRS - ULP
BP28, F 67037 Strasbourg Cedex 02 - France

Abstract

The ALICE detector at LHC consists, in its inner part, i.e the internal-tracking-system (ITS), of six concentrical barrels of silicon detectors. The outmost two layers are made of double-sided strip detectors. In the framework of an R&D, their characteristics and performances have been studied off- and in-beam at the PS and the SPS (CERN). Sensors, manufactured by two different companies, have been tested and their performances analysed. The results are presented and discussed.

1 Introduction :

<u>A</u> <u>L</u>arge <u>I</u>on <u>C</u>ollider <u>E</u>xperiment (ALICE) [1] is in preparation at LHC. It is a complex apparatus aimed at the detection of hadrons and leptons emitted in the Pb + Pb collisions at ultra-relativistic energies. Together with the TPC, the most inner part (ITS), covering the $|\eta| \leq 0.9$ pseudo-rapidity region, is devoted to the dE/dx measurement and the tracking of charged particles as well as the secondary-vertex reconstruction for the short-lived particles with a $c\tau$ ranging between a few millimeters and a few tens of centimeters. It allows also the detection of low transverse-momentum particles which do not reach the TPC. It consists, from inner to outer, of 3 pairs of concentrical cylinders of pixels, drift and strip silicon-detectors.

The outmost two layers of the ITS have 40 and 45 cm radius, for a length of 45.1 and 50.4 cm, including 770 and 936 double-sided strip detectors (SSD), respectively. These sensors have been designed [1] as 75×42 mm^2 overall area, for a maximum thickness of 300 μm. They have 768 strips, about 25-40 μm wide, with a pitch of 95 μm, on each side. The strips are oriented with an angle of ± 17.5 milliradians, depending on the side, with respect to the short side edge of the detector, i.e a stereoscopic angle of 35 milliradians.

In the framework of R&D's currently in progress, we have ordered from each manufacturer (Canberra and Eurisys Mesures) several SSD's with the general specifications reported above, and studied their characteristics and performances on a test-bench at IReS, as well as in-beam at the PS and SPS at CERN. Additionnal so-called test-structures, i.e replicas of the SSD's with only 128 strips, have also been used for complementary tests, see for example Ref. [2].

The results obtained for the two sets of detectors are presented and discussed in this note. Typical results are given without direct comparison due to the low number of tested detectors.

2 Specific Characteristics of the SSD's :

The four SSD's, prepared to the general specifications given in the introduction, have the following features. They are produced from a block of silicon of n-type and the implanted strips obtained by p$^+$ (junction side) and n$^+$ doping (ohmic side) on the p side and n side, respectively. An SiO$_2$ dielectric layer performs the insulation of the detector, i.e. the capacitive coupling between aluminium strips ($\geq 1 \mu$m thick) and implanted strips on which the created charges are collected. All strips extremities have two pads, thus offering spare-bonding or flexible connection during tests. Each detector side is electrically, mechanically and chemically protected by passivation.

There are no floating-strips and the insulation between strips on the ohmic side is achieved by p-spraying. The strips are polarised via punch-through technics with a bias ring which is surrounded by a guard ring ($\leq$ 1mm wide), defining an effective area of 73×42 mm^2 for the SSD. A layout of a part of the p-side is shown in Fig.1.

As the functioning and the performances of the SSD's depends substantially on the different capacitances characterising the detectors, values for these have been specified at the time of the order. However, they may vary with the resistivity of the silicon ($\geq 6 \, k\Omega.cm$), the design technics and the manufacturing process. Consequently, they have been measured, after delivery, with a probe-station [3] at IReS. The results are described in the next section.

2.1 Test-bench and Probe-Station Measurements

The geometrical characteristics of the SSD's have been measured by means of a probe-station and were found nominal. The coupling capacitor value (C$_{cpl}$) of the strips is typically
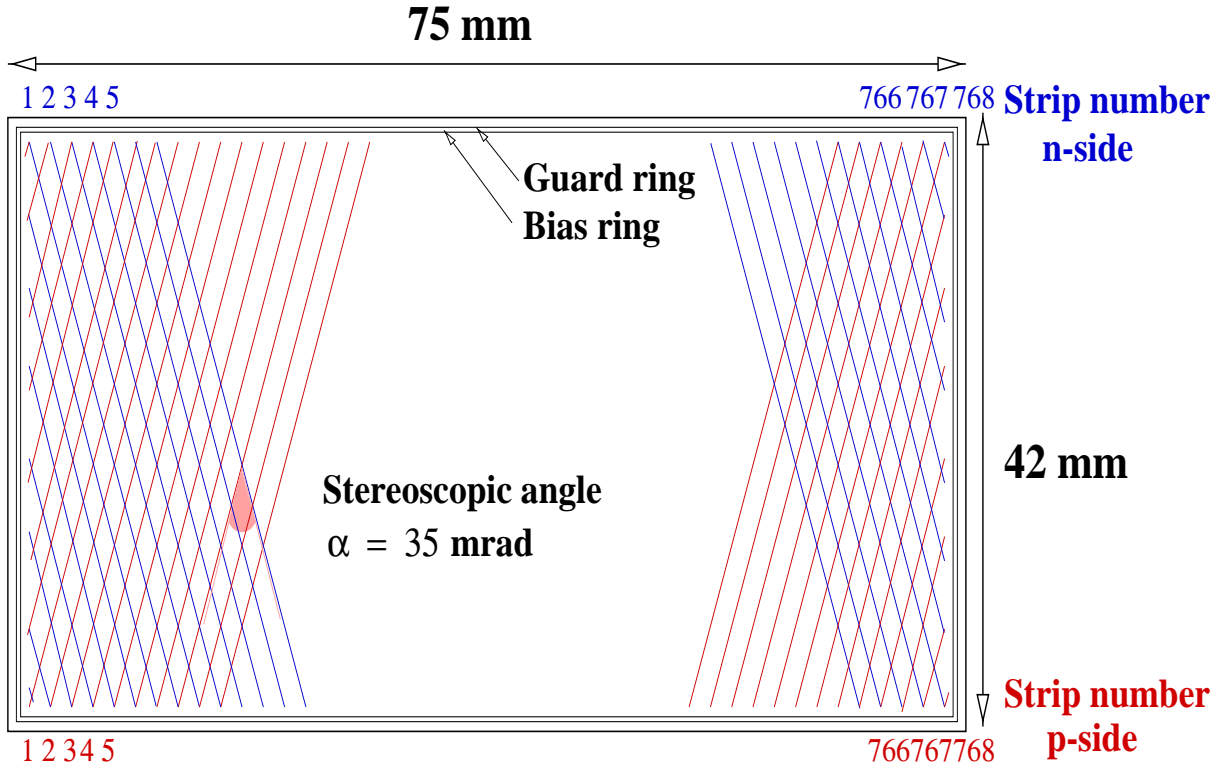
Figure 1: Scheme of a SSD, some of the characteristic dimensions are indicated

larger than 180 pF. An example is shown in Fig. 2 for all the strips on both sides of a SSD. The C_{cpl} values are close to 220 pF and 200pF for the p- and n-side, respectively, for most of the strips. One shortened capacitor is visible among the low-numbered strips, while the C_{cpl} decrease, for the high-numbered strips, is due to shorter-length strips, resulting from the stereoscopic angle.

The C_{cpl} over inter-strip capacitance (C_{is}) ratio has been imposed ≥ 20, it yields a C_{is} value ≤ 9 pF. Such a ratio minimises the crosstalk between the neighbouring strips which is strip-width and pitch dependent in a complicated manner. According to simulations giving C_{is} as a function of the width of the strips (for 95 μm pitch), it justifies a requested strip-width value of 25-40 μm.

The bulk capacitance (C_b) was measured versus the bias voltage (V_b) to examine the full depletion voltage of the SSD. As shown in Fig. 3 the complete depletion may be reliably obtained for $V_b \geq 40$V.

The bulk (i_b) and the guard ring (i_{gr}) leakage currents are shown in Fig. 4 versus V_b. Both increase rapidly up to $V_b \sim 25$V then level off somewhat around 1.5 and 1.8 μA between 30-60V. The strip leakage current (i_s) was measured to be ~ 1.9 nA, i.e $i_b/768$.

These figures are satisfactory but not absolutely representative of a large number of SSD's. Nevertheless, it may be considered that the SSD's could be effectively operated at $V_b \leq 55$V, thus limiting the risk of voltage break-down and SSD damage, and warranting a satisfactory detector operation with acceptable leakage currents $i_s \leq$5nA, $i_b \leq$5μA and $i_{gr} \leq$5μA.
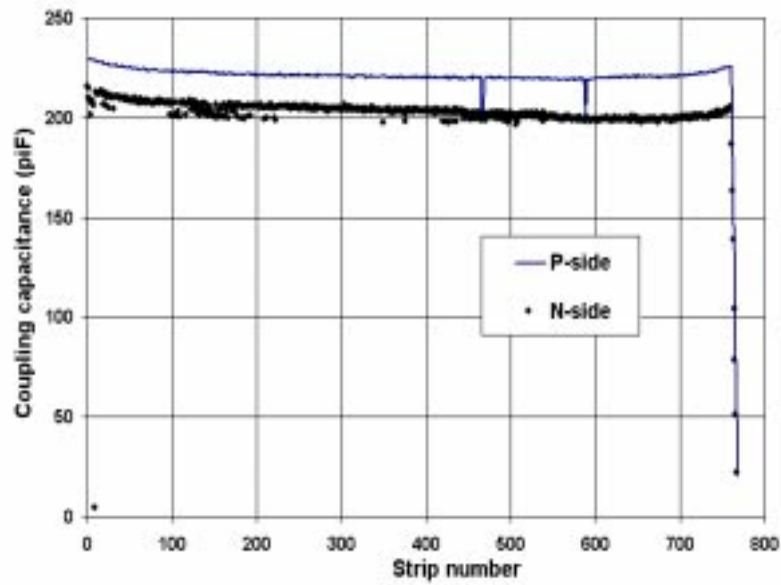
2

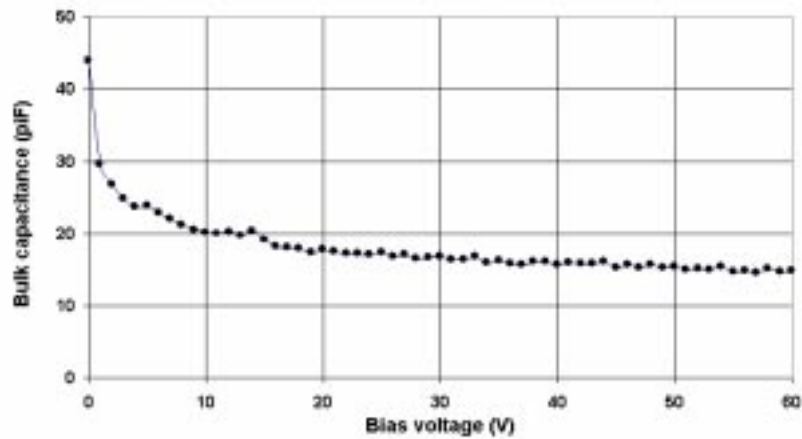Figure 2: Measured strip coupling capacitance of a SSD

Figure 3: Bulk capacitance versus bias voltage for a SSD

2.2 Definition of quality tests after mass production for SSD

Due to the low number of tested SSD's, only some limited information may be derived from the present analysis about the expectable quality of the mass production. However relevant specifications have been imposed to the potential manufacturers.
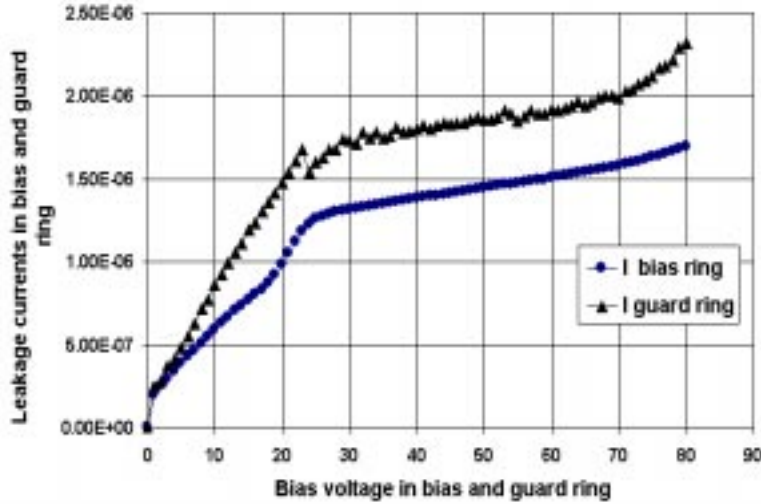
Figure 4: i_b and i_{gr} versus V_b

3 In-beam tests of SSD's

The four SSD's have been tested in-beam at the PS and the SPS with 6 GeV and 120 GeV pions, respectively. The detectors were bonded to twelve (6 for each SSD-side) 128C read-out chips designed and developed in collaboration by the LEPSI and the IReS. These chips, described in previous papers [4, 5], are essentially characterised by 128 analog channels allowing shaping and amplification. They incorporate JTAG digital control, a pulse generator for test purposes, and run at very low power consumption (≤ 340 μW/channel). In this way, the test campaign was also devoted to the study of the performances of the 128C chip and the results will be published separately [6]. The chips were mounted on a hybrid board, also IReS designed and developed. This structure was placed on a spectrometer connected to a Data Acquisition system previously described [7, 9].

The spectrometer consists of 4 planes of pairs of single-sided SSD's (each pair having a detector with strips x- and another y-oriented), with about 2 μm spatial resolution, thus allowing for accurate tracking of the pions, with a track interpolation error of less than 1 μm at the location of the tested SSD, i.e in between each couple of pairs of reference detectors. The four SSD's were successively tested in the spectrometer.

The DAQ, triggered by pulses from NE102 scintillator + photomultiplier assembly, incorporates a VME crate, Sirocco ADC boards, and an acquisition sequencer board. The system is run by the MicroDAS software using the OS9 operating system. The data are recorded on Exabyte cassettes.

The data analysis procedure, which makes use of a C++ computer code using the ROOT framework, originally developed by the RD42 collaboration, has also been described before in its principe [10]. Since a choise is left to the user about the input parameters, which, in turn, may influence the results, the present analysis deserves nevertheless, some comments about the procedure.

When a particle passes through a SSD , it activates a number of strips without, *a priori*, knowing how many of them participate to the collection of the created charges (incidence angle effect, interstrip capacitance, δ electrons ...). The analysis consists of measuring and

4

interpreting these charges via an electronic signal.

The readout strip-signals (rawdata in ADC counts) include different components : ADC (i,k) = P (i,k) + CMS (j,k) + S (i,k) where i, j, k are the strip, the chip and the event numbers respectively. The pedestal P(i,k) value, for each channel, is calculated by averaging the individual values over a certain number of events. Then, the noise n_i characterising each channel is calculated. It is assumed to be the variance of $A_i = (ADC(i,k) - P(i,k))$.

After common mode shift (CMS) and pedestal subtraction from the rawdata, one gets the signal S(i,k) for each strip and each event.

This physics signal should exceed substantially the noise (n_i) for the activated strips. An example of data is presented in Fig.5, it shows the signals after pedestal subtraction for the both sides.
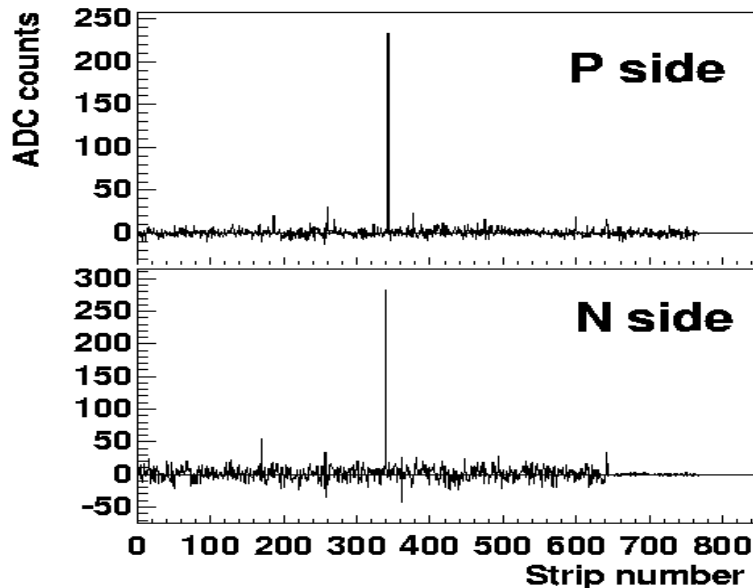

Figure 5: Signals on both sides of a SSD after the pedestal subtraction, one readout chip on the n-side (channels 640 to 768) was not operating properly. The physics signal corresponding to a pion detection is clearly visible and well correlated on the both sides.

Distributions of the noise measured on the two sides of a SSD are shown in Fig.6 for the Eurysis detector. They represent the noise of the SSD + chip ensemble for one channel taken at random among the 768. The noise on the n-side is larger than for the p-side , the σ of the distributions being equal to 371 e$^-$ and 780 e$^-$, respectivelly (one MIP has been taken equal to 25000 e$^-$ in 300 μm of Si). For the Canberra detector, the noise value is almost the same on each side and equal to 540 e$^-$.

Turning now to the data analysis itself, the first step, consists of searching the strips having a s_i/n_i ratio exceeding a threshold L_1 chosen by the user. L_1 is taken large in order to identify reliably the fired strip which is considered as the *seed* strip. In the present analysis, there should be only one strip found per event, but it turns out that some events ($\sim 3\%$) have more than one strip satisfying the requirement, even after elimination of possible defectives strips previously identified, i.e dead or noisy strips. The next step consists of repeating the operation for the neighgouring strips with another limit $L_2 \leq L_1$. These latter strips define, with the seed-strip, a cluster of n_s adjacents strips. Typically, $n_s \sim 1.5$ for L_1=10 and L_2=2, as illustrated in Fig. 7.
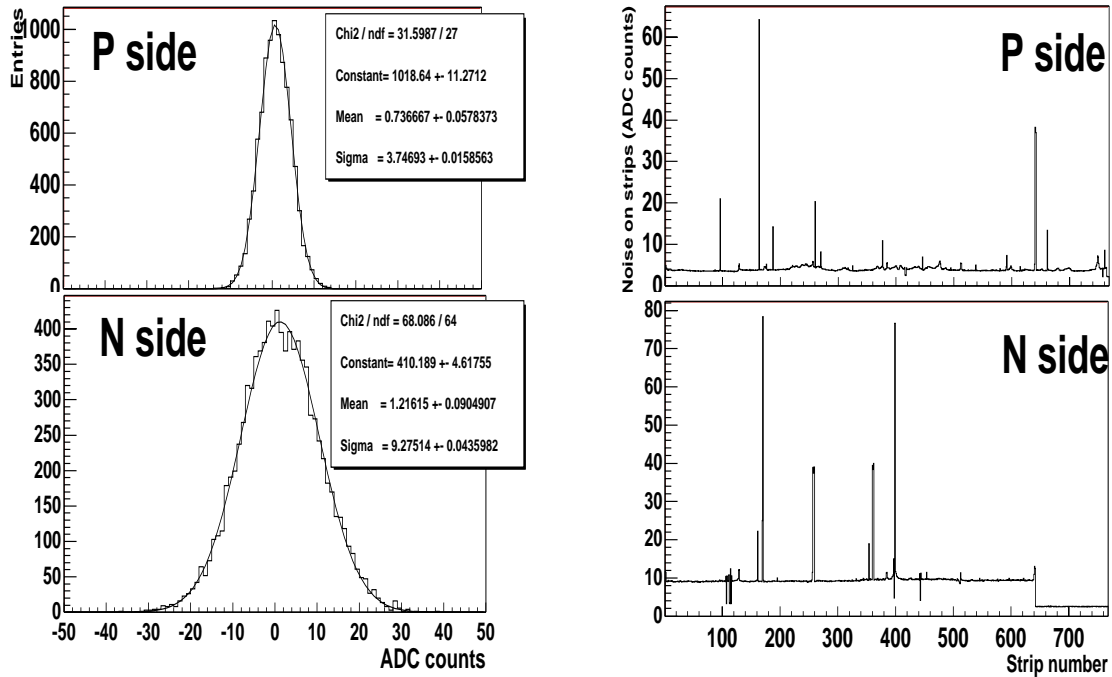
5

Figure 6: On the left part, signal (ADC - P - CMS) distributions for a p-side and a n-side strip randomly chosen. The noise is given by the sigma value of the fit. On the right part, the sigma value obtained from a gaussian fit for each strip is plotted for both sides of an SSD.
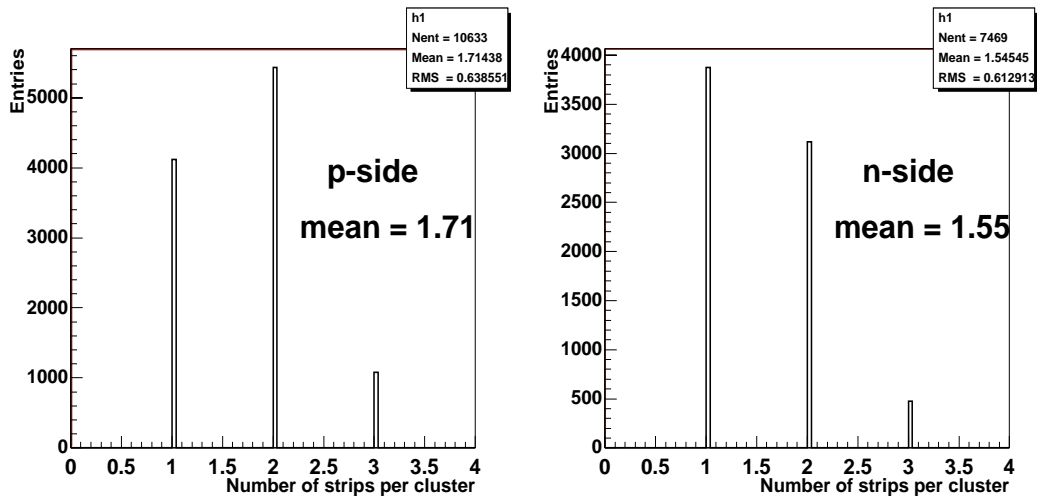

Figure 7: Number of strips per cluster for L_1=10 and L_2=2

These's L's values, used throughout the analysis, have been optimised from a recurrent analysis leading to a detection efficiency (number of hits measured with the SSD/number of

6

hits measured simultaneously with all the reference detectors) of 99%. It reflects the fact that the pulseheight distribution of the physics signals exceed by 3 σ (99% confidence probability) the noise distribution characterised by the standard deviation σ. More constraints are applied for the cluster determination but they are not discussed here as being of secondary importance.

Once a cluster of strips (of charges) has been determinate, a signal and a noise value are currently calculated as $S = \sum(s_i)$ and $N = \sum(n_i/n_s)$, respectively, for these clusters ; S/N turns out to be a relevant variable. An example of S/N, measured for the two sides of a SSD, is shown in Fig 8. The distributions are Landau shaped, and exhibit a maximum around S/N $\sim$ 45 for each side (upper frames). Departure from this case may be seen in the same figure (lower frames) where an asymetry is observable between the p- and n-side ($\sim$ 60 and $\sim$ 30 respectively) of another SSD.
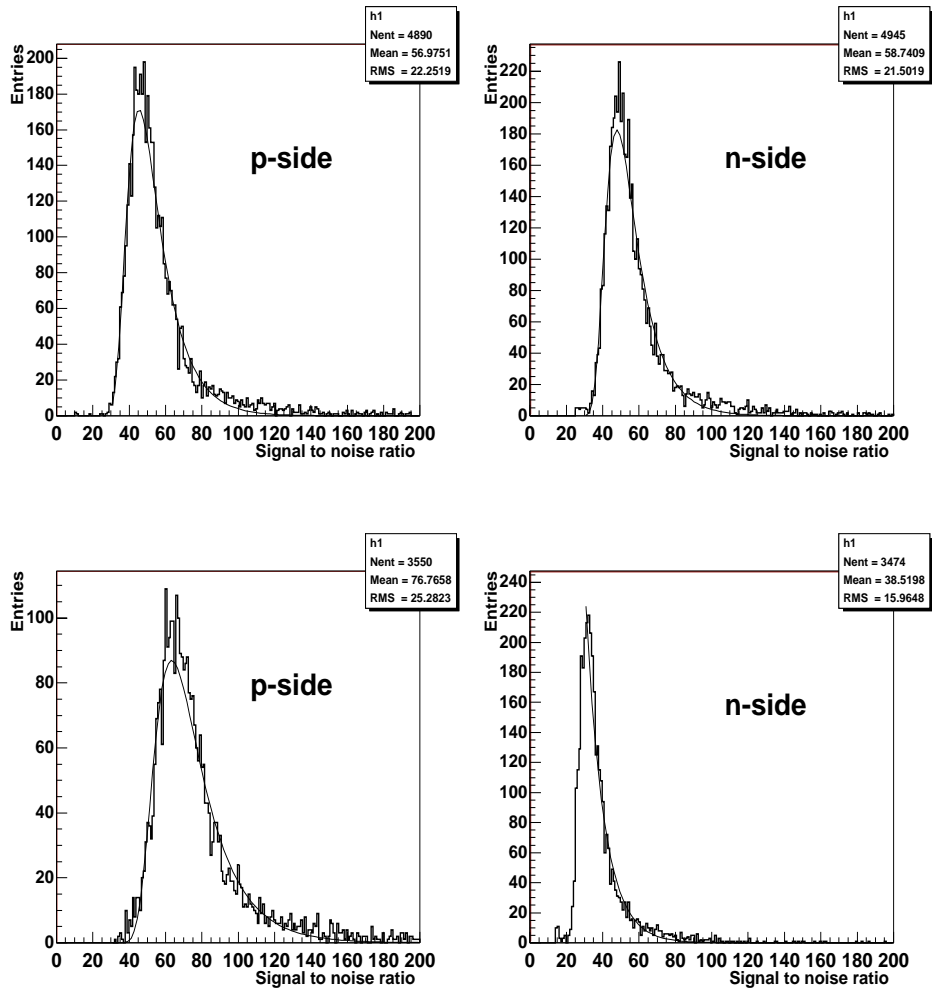

Figure 8: Signal to noise ratio for tested detectors (Canberra detector on higher part and Eurisys Mesures detector on lower part)

One virtue of a double-sided SSD is to allow the correlation of charges collected on the two sides [8], thus reducing multi-hit ambiguities. An example of this charge matching is presented in Fig 9, it corresponds precisely to the case of Fig 8 lower part . The pulseheight of the p-side is plotted versus that of the n-side The standard deviation σ measured for the distribution of the ratio (p-side pulseheight/n-side pulseheight) is between 5 and 6% which is typical of all tested SSD's.
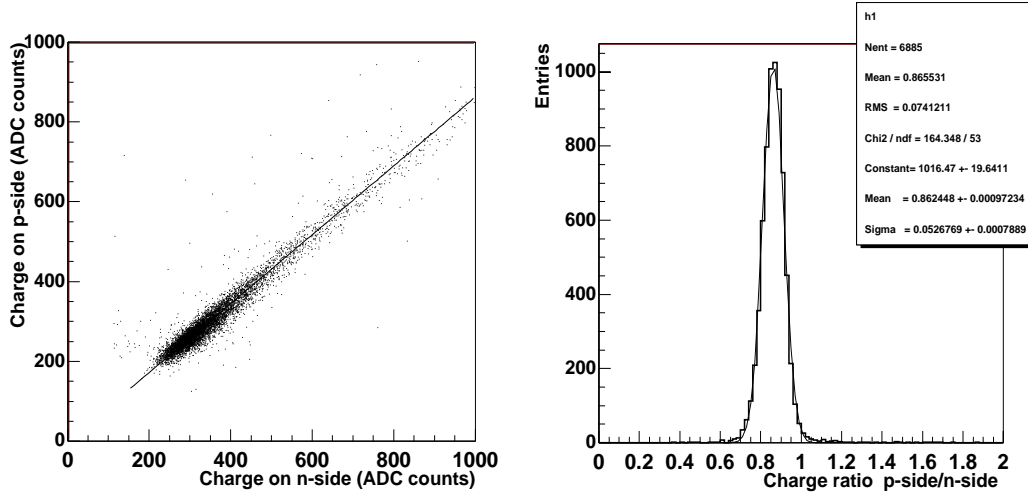

Figure 9: Charge matching between p-side and n-side of a double-sided detector

The spatial resolution of the detector is, of course, quite a relevant characteristic. The used method to determine it has been described earlier [9], [10]. The resolution may be calculated from the residual difference between the measured position of the hit on the SSD and that determined from the tracking. It should be kept in mind, that due to the stereoscopic angle, the hit position is initially determined in a (u,v) frame referential rotated by 17.5 milliradians with respect to (x,y) frame, see Fig. 10.
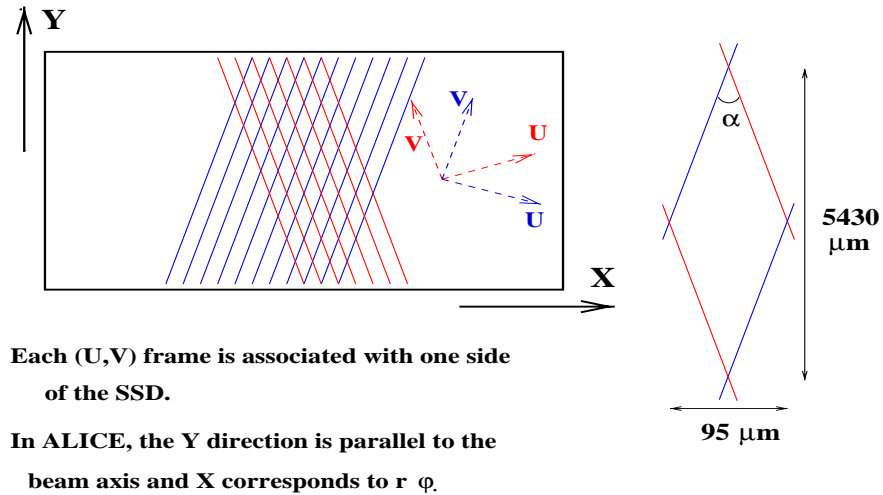

Figure 10: (u,v) frame and (x,y) frame used in the spatial resolution determination

The residuals x (orthogonal to the beam axis) and y (parallel to the beam axis in ALICE) are shown in Fig. 11 for the p- and n-side. They are typically of 15 μm in the x direction and around 750 μm in the y-direction, in agreement with ALICE requirements.
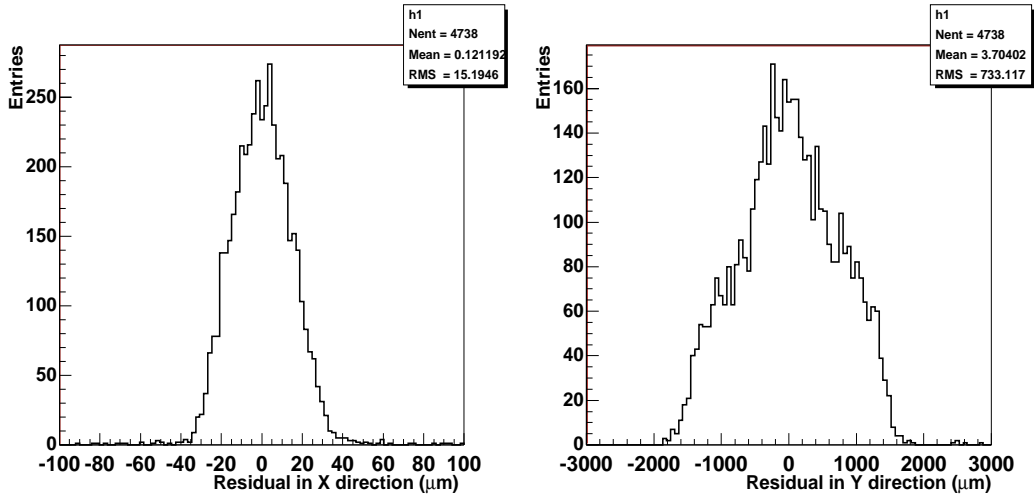

Figure 11: Resolution of an SSD in the (X,Y) frame defined by the edge

4   Conclusion :

Four double-sided SSD's, prepared at the general ALICE specifications and purchased from two different manufacturers have been tested off- and in-beam at the IReS and at the PS and SPS (CERN). The tests have been performed by using a read-out electronic chip, developed and designed jointly by the LEPSI and the IReS, to this purpose. The performances of these modules satisfy the ALICE requirements defined in the Technical Proposal, in particular, in term of charge matching and spatial resolution ($\sim$ 15 μm in the direction perpendicular to the beam). They indicate that the fixed milestone has been fulfilled.

On this basis, 320 modules are going to be produced and assembled in the near future, to fabricate the outer layer of double-sided SSD's, around the SVT of the STAR detector at RHIC.

References

[1] ALICE Technical Proposal, CERN/LHCC 95-71, LHCC/P3, December 1993

[2] M.Germain et al., Alice Note INT-99-07 (1999)

[3] Karl-Suss Probe-station PA200

[4] J.R. Lutz et al., Proc. of the Fourth Workshop on Electronics for LHC Experiments, Rome (1998)

[5] M. Ayachi et al., Proc. of the Fourth Workshop on Electronics for LHC Experiments, Rome (1998)

[6] A. Tarchini et al, ALICE Internal note, in preparation

[7] C. Colledani et al., *A submicron precision telescope for beam test purposes* NIM **A372**, (1996) 379

[8] R.Turchetta, Phd Thesis, Université Louis Pasteur de Strasbourg (1991).

[9] L.Arnold et al., ALICE Internal note, SIL-98-05 (1998)

[10] D.Meier, PhD Thesis, University of Heidelberg (1999) to be published