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New TDC electronics for a PesTOF tower - in NA49

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Abstract

A TOF spectrometer system based on a tower of 20 Pestov counters with a new, very compact electronic time measurement and read-out system was installed in the NA49 experiment. During the run in November 1999 about 200k Pb-Pb collisions have been recorded. For the first time the electronic system included 640 timing channels based on High Resolution TDC chips. The electronic as well as the counter time resolution estimated 'on-line' were 40 ps and 50 ps, respectively, agreeing well with the values measured at laboratory conditions.

1. Introduction

The NA49 experiment at the CERN-SPS [1] was built for the investigation of p-p, p-Nucleus and Nucleus-Nucleus collisions. It records charged particles over a large range of phase space with a set of 4 TPCs and time of flight walls. Two Vertex-TPCs are operated inside the Vertex-Magnets with a field strength of up to 1.5 T. The particle identification is based on energy loss (dE/dx) measurements in the TPC tracking system and time-of flight measurements in the forward rapidity hemisphere. Fig. 1 shows the experimental set-up of the NA49. During the lead beam time in November 1999 an additional TOF system based on a tower of Pestov counters [2] was operated at a distance of 4 m from the target behind V-TPC-1 in order to extend the particle identification to the backward rapidity hemisphere.

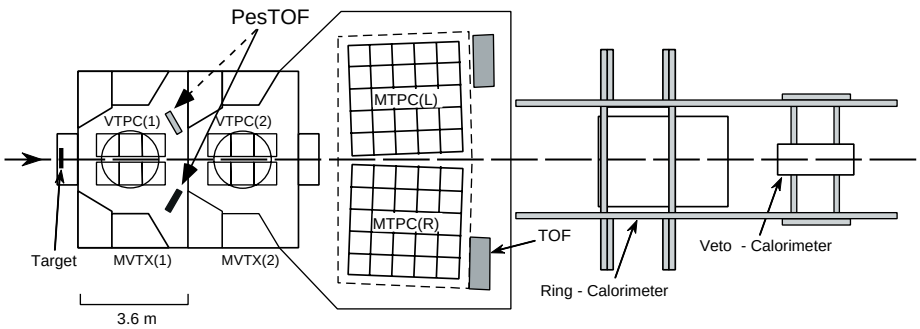

Fig. 1. Set-up of the NA49 experiment. The dashed arrow points to the planned second tower to be installed in 2000.

The tower consisted of 20 Pestov counters, which were mounted on a common ‘multiflange’. The counters were arranged in two staggered layers to provide full coverage in space with their active areas. This ‘multiflange’ allowed to distribute an equal fraction of the gas flow to every counter. The total surface of the PesTOF wall (taking into account the counter overlapping regions) was about $0.22m^2$ and each of the counters had a sensitive area of 40x300 mm^2 [2]. In this run a new modified gas mixture consisting of 0.07(bar) 1.3-Butadiene + 0.3 Propylene + 2.4 Isobutane +9.23 Ne = 12bar was used, which was shown to yield a better time resolution at lower HV values and a reduced tail in the time spectra [3].

The time and charge measurements and the read-out were done with a new, very compact electronic system. Each counter had 16 signal strips, which were connected to 32 TDCs and 16 QDCs. A new development was that not only the discriminators and QDCs [4], but also the TDCs were mounted directly on the counters, so that the whole system of 640 TDCs and 320 QDCs, apart from the necessary power lines, was connected by only 6 multiwire flat cables to a VME-crate. It is important to note that for the first time high precision time measurement for a large detector system was achieved by measuring ‘time-stamps’ and not ‘time differences’. This new technique leads to a significant simplification. The new TDC-system made use of 4-channel High Resolution TDC (HRTDC, Fig. 2) chips developed at CERN by J.Christiansen and M.Mota [5]. The necessary logic (Fig. 3) and the layout of the various boards including the VME-units were developed, tested and built by the group of J.Biri at the KFKI / MTA-ITA-LAI in Budapest.

The readout of the PesTOF tower was incorporated into the NA49 data acquisition. About 200k lead-lead events at 40 AGeV/c have been recorded in November 1999. The average multiplicity in the PesTOF tower was 8.8 particles per event. The whole system operated without any failure or necessity for a restart for a data run of two weeks. This report will give a short description of the TDC-system and of the time resolution, which was obtained.

2. The new TDC-System

2.1. The High Resolution TDC (HRTDC)

The HRTDC makes use of the intrinsic propagation delay of a signal through the gates of an array of delay elements locked in phase to a common 80 MHz clock. In case of a hit the status of all 140 gates together with an eight-bit coarse scaler are strobed into a register, thus giving a 'time-stamp' of the event. In this way a time resolution of 90 psec LSB (Least Significant Bit) has been obtained. More details on the HRTDC can be found under: http://pcvlsi5.cern.ch/MicDig/hrtdc.htm

The main advantages of using 'time-stamps', as done in the HRTDC, as compared to conventional TDCs are:

- By using 'time-stamps' the operation of the TDC can be described as common-stop mode, without the necessity of a prior arm signal. Thus no delays are required for the time signals.
- By feeding the digitized signal into a FIFO, the decision of whether the hit belongs to an event which fulfills the trigger conditions, is not required before the event is strobed out of the FIFO. In this way delays of several μsec can easily be obtained without loss in resolution and there is no need for a fast clear.
- Using an array of delay locked loops practically no calibration of the individual channels is required.

Since the START signal is treated in an identical way as the STOP signals, using however, a separate HRTDC-chip, the time of flight resolution depends crucially on the phase stability of the different chips with respect to the clock.

2.2. The control of the HRTDC

In Fig.2 the control of the HRTDC-chip is shown in a schematic way. Apart from the initialization two modes of operation, 'data taking' and 'readout', respectively, are determined by the status of a flip-flop (FF).

Data taking mode (FF=0):

Hits arriving at one of the four inputs of the HRTDC are digitized with respect to the phase of the 80 MHz clock and transferred into the FIFO via a multiplexer. The signal 'FIFO ≠ 0’ opens a gate and the next pulse from the 'Clear oscillator' will advance the pointer in the FIFO. Since the 'parallel port' is closed the hit is lost. This clearing of the FIFO continues until the signal 'FIFO ≠ 0' disappears.

Readout Mode (FF=1):

As soon as the FF is set the inputs of all HRTDC-chips are disabled (not shown in Fig.2) and the 'Clear Oscillator' is blocked by $\overline{Q}$. Control is given to the 'Readout Logic', which scans successively all HRTDC-chips on the board. If the selected one sends 'FIFO ≠ 0' then the readout logic advances the pointer in the FIFO and via the parallel port, which is now open, the data arrive on the data bus. Before transferring them to the VME-crate the logic adds the identification of the chip, the board and the tower. This process is repeated until the FIFO is empty and the logic switches to the next HRTDC-chip. After scanning the last chip the logic in the tower controller advances to the next board (Fig.3).

An essential feature for operating the TDC in such a simple way is that the transfer of a hit from the input of the TDC via the multiplexer into the FIFO takes a certain time, in our case at least 5 μsec. Therefore the trigger may arrive up to 5 μsec after the event thus giving ample time for the trigger logic and making fast clear operation unnecessary.

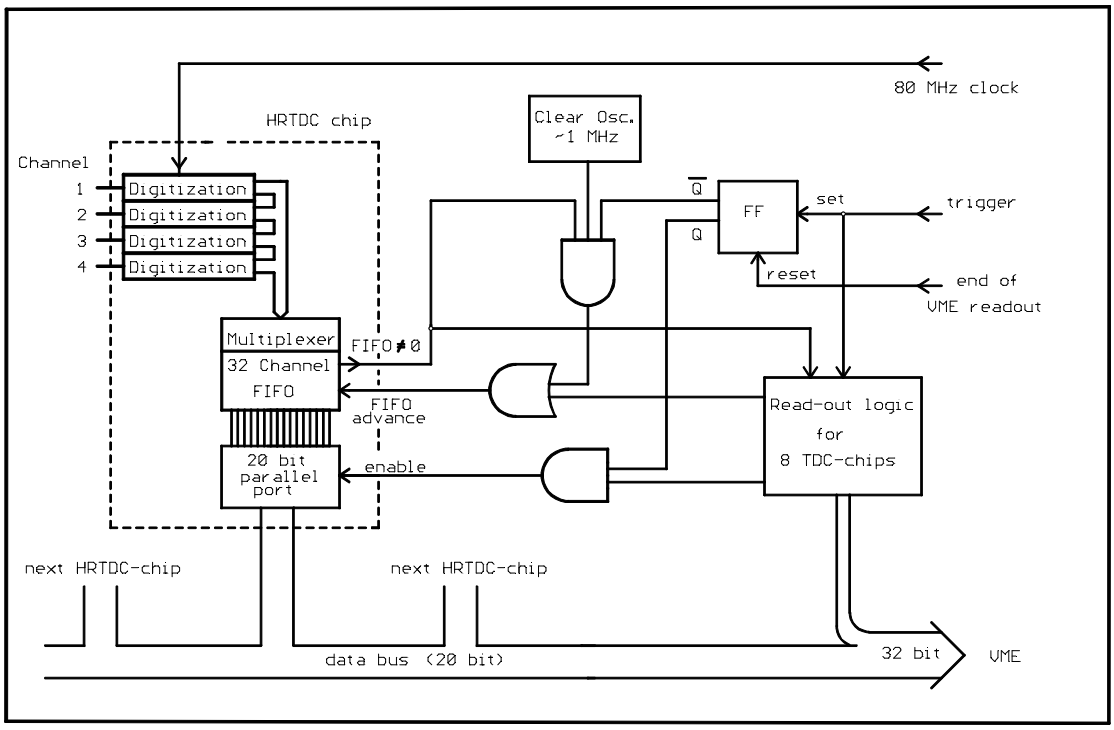

Fig.2. Principal circuit of the HRTDC-chip control.

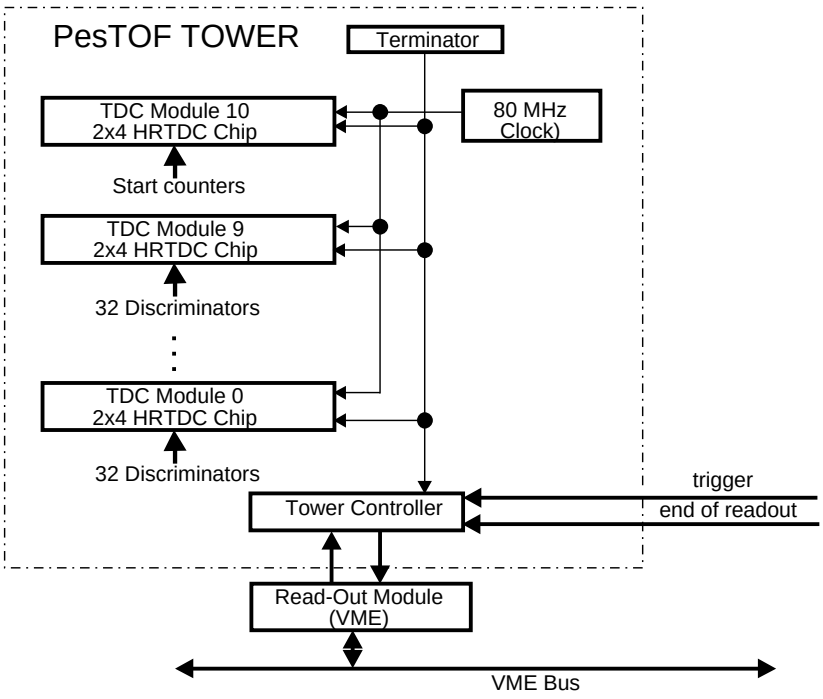

Fig.3. TDC electronics with VME read-out for the PesTOF detectors.

3. On-line results

3.1. Stability of the TDC- system

The chips (power consumption ≈ 1 W each) were brought into thermal contact with a 20 x 5 mm^2 water-cooled brass tube. No special care was taken to keep the water temperature constant. All 160 chips were then operated with the same initialization parameters and none of them failed to synchronize to the 80 MHz clock. The chips were never reset, either by software or by hardware except at initialization.

One of the big uncertainties when operating 160 HRTDC-chips in a densely packed environment was whether the 80 MHz distributed to them would influence the discriminators or even the NA49 TPC. In order to minimize any possible cross talk the TDC-board had 6 layers, one dedicated to the 80 MHz and the two neighboring ones grounded. As a result of this we did not find any influence of the 80 MHz clock neither on the discriminators nor on the NA49 TPC.

3.2. Electronic time resolution

The values for the time resolution, which will be given in the following always refer to one time channel or counter. They are the result of fitting the measured time spectra up to a FWHM level by a Gauss distribution, which then is divided by sqrt(2).

The signals of the two START scintillation detectors of the NA49 experiment were each given on 6 time channels in order to eliminate for this signal the effect of the comparatively large LSB of 90 ps. From the difference of two time channels of the same START detector, but also from the difference between the two START detectors, the electronic time resolution of the TDC-system could be determined to be slightly better than 40 psec over a period of 6 hours. This value is close to the value of 35 ps obtained during a short time in the lab for two channels within the same chip.

If we select events where a particle traversed a counter between two strips leading to similar pulse heights on both of them then the electronic resolution of the system including the double threshold discriminator can be determined. This distribution, shown in Fig.4, was determined for all 600 possible combinations of neighboring strips. From this distribution the average electronic resolution per channel was determined to be 58/• 2=42 ps.

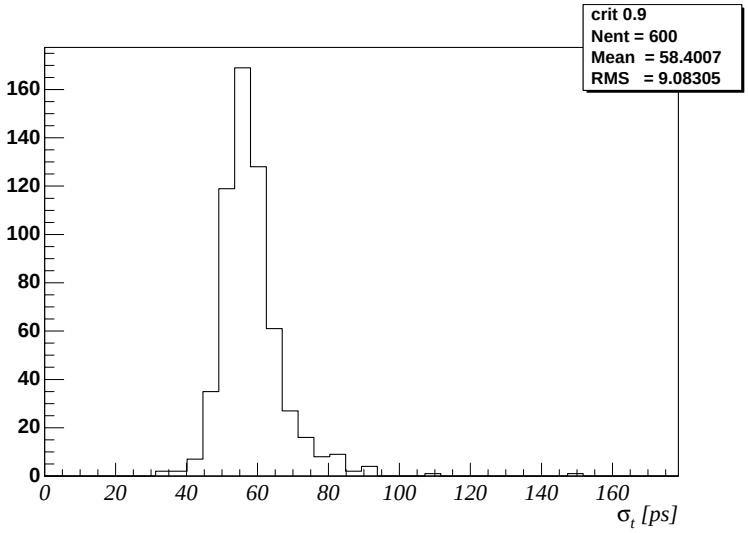

Fig.4. Electronic time resolution for different combinations of neighboring strips.

The effect of the START scintillation detectors on the TOF resolution was estimated from the time difference spectrum between two START detectors. A time resolution of σ=43 ps was measured for a single detector equipped by 6 time channels to reduce contributions from the comparatively large LSB of 90 ps. Therefore, from two START detectors a time accuracy of σ=43/• 2=30 ps is expected.

3.3. Counter time resolution

As long as the trajectory reconstruction through the TPC is not available the overall time resolution of the spark counter can only be determined from those events where a particle traverses two counters, one in the forward and one in the staggered backward plane. Since this can only occur for particles traversing the two detectors near their edges, the observed resolution of 91/• 2=65 ps (counter+ electronics) per counter refers to the edges of the counters and should be an upper value for the overall time resolution (Fig.5). Subtracting the contribution of the electronics (42 ps), an upper value for the intrinsic time resolution of the spark counter of ~50 ps was obtained.

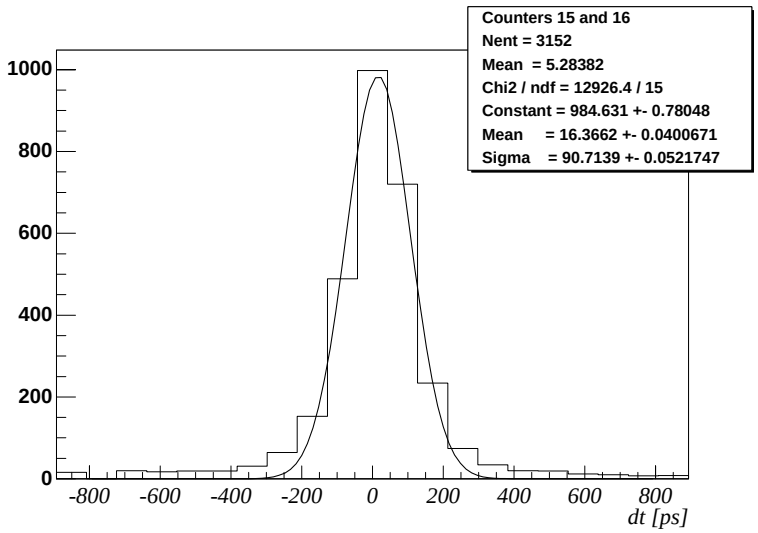

Fig.5. Time spectra from the overlapping areas of two spark counters (see text).

4. Conclusion

A tower of 20 Pestov counters in a configuration suitable for physics data taking was operated together with the NA49 experiment in November 1999. All components of the PesTOF tower including the new compact High Resolution TDCs, which were used for the first time worked reliably. For the next HI-period at CERN planned for 2000 the system will be enlarged to two towers.

References

1. NA49 Collaboration (S. Afanasiev et al.), .Nucl. Instrum. and Meth. A430 (1999) 210-244.
2 E.Badura, V.Dodokhov, J.Eschke et.al., .Nucl. Instrum. and Meth. A379 (1996) 468-471.
3 Y.Pestov, H.R.Schmidt and B.Schreiber, Report on V Workshop on Resistive Plate Chambers and related Detectors Bari, 1999.(in print).
4 U.Frankenfeld, GSI, DISS. 99-17, November 1999.
5 M. Mota, J. Christiansen. "A four channel self-calibrating, high resolution, time-to-digital converter", In Proc. IEEE ICECS98, Vol. 1, pp. 409 - 412.