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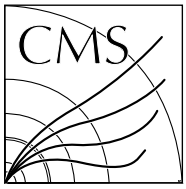

The Compact Muon Solenoid Experiment

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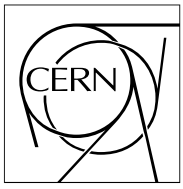

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Results of irradiating the APV5 chip

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Abstract

An APV5 chip has been irradiated in steps up to 16 Mrads using a ^{60}Co source in order to confirm the radiation hardness expected from individual transistor and sub-circuit measurements. Full functionality is preserved after irradiation and measurements of the amplifier pulse shape and noise are presented.

1. Introduction

The APV5 is a full size prototype of the 128 channel readout chip to be used for readout of the silicon and gas microstrip detectors in the inner tracker of the CMS experiment at the LHC. It was fabricated in the Harris AVLSIRA rad-hard bulk CMOS process and its functionality and performance in lab and beam tests have been described in detail elsewhere [1,2]. The radiation hardness of the Harris process has been thoroughly investigated [3,4,5] at the individual transistor and amplifier sub-circuit level leading us to confidently expect uncompromised operation of more complex circuits such as the APV5. The purpose of this work has been to confirm these expectations.

2. Irradiation test set-up

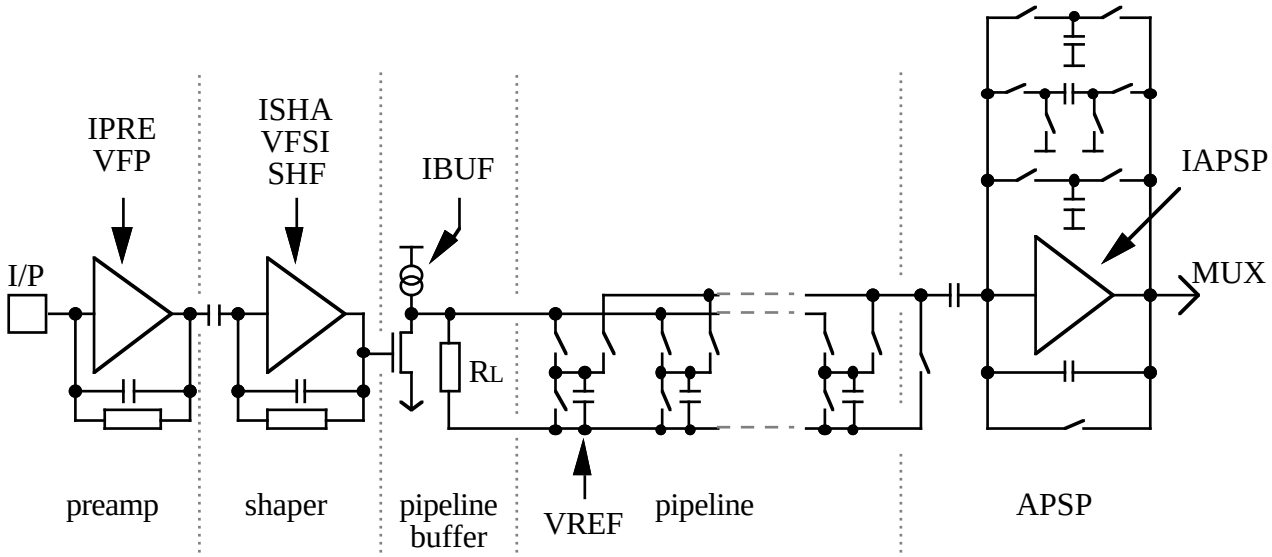
The APV5 die was mounted on a fineline PCB connected to peripheral PCBs which provided the bias levels and interfacing of clock, T1 and reset digital control signals to the chip. The fineline and service PCBs contained only passive components (metal film resistors and ceramic capacitors) which can withstand the radiation dose levels. The chip output was connected directly to a 50 Ohm coaxial cable so that the output data stream could be monitored on an oscilloscope outside the radiation cell. A VME crate containing a Sequencer module was also located outside the radiation area which provided the digital control signals at differential ECL levels. During irradiation a simple repetitive sequence was used to exercise the APV5 digital logic which consisted of a reset followed by a single trigger, and then a delay sufficient to allow the APSP and analogue multiplexer cycles to complete. The clock input to the chip was at 20 MHz and the peak mode of operation was selected.

The preliminary bias settings to the chip before irradiation are given in table 1. The nominal values shown are those required to ensure correct operation of the chip. Figure 1 shows a schematic of one channel of the chip which illustrates the functional blocks affected by each control setting. The function and value of each bias control will now be discussed in turn:

Table 1. Nominal (pre-irradiation) values of the APV5 bias control settings.

Bias setting	Magnitude
IPRE	500µA
ISHA	100µA
IBUF	100µA
IAPSP	50µA
ISHF	~few µA (see text)
VREF	-1V
VFP	-400mV
VFS	-1.50V

Figure 1. Schematic diagram of one channel of the APV5



IPRE: Determines the current flowing in the preamplifier. The mirroring is such that a value of 500µA for IPRE results in 300µA actually flowing in the PMOS input device.

VFP: Determines the resistance of the FET resistor in the preamp feedback loop. The value of this voltage setting is non-critical, as long as the resistance is sufficiently large to ensure that the charge integrating preamp output fall time is long compared to the subsequent shaping time.

ISHA: Determines the current flowing in the shaper. A value of 100µA results in approximately 80µA actually flowing in the NMOS shaper input transistor.
VFS: This voltage level is used to adjust the shaper feedback resistor and needs to be tuned to achieve the desired pulse shape. The effect of this control is most significant on the fall time of the pulse.

ISHF, **VREF**: ISHF is used to adjust the DC level at the output of the shaper such that the pipeline buffer circuit operates at the appropriate point on its transfer characteristic. For correct operation the quiescent DC level at the pipeline input should be around -1 Volt. VREF is the voltage on the back plates of all the capacitors in the pipeline and is common for all channels in the chip. The shaper/buffer circuitry is correctly set up when VREF is at -1V and no current flows in the buffer output load resistors R_L (on-chip), which is achieved in practice by driving VREF to -1V and adjusting ISHF (automatically by external circuitry) such that the current flowing in the VREF line is zero.

IBUF: This current is mirrored directly to the pipeline buffer transistor.

IAPSP: Determines the current flowing in the APSP circuit.

3. Irradiation procedure

The irradiation was performed in 4 steps, the details of which are shown in table 2. The dosimetry was carried out using a calibrated silicon photodiode. Unfortunately the power supply tripped at some time during the final 12 Mrad irradiation, which means that the chip was unbiased for an unknown period of time during this step. The radiation effects on an unbiased device differ from those occurring when the device is biased because the migration of charge generated in the gate oxide is different in each case. It should therefore be borne in mind that the results after the 4th step might be different if the device had remained biased throughout the entire irradiation.

Table 2. APV5 irradiation schedule

Start Date	duration [hours]	dose rate [kRad/hr]	cumulative dose [Mrads]
9/5/96	3	80	.25
21/5/96	9	80	1
24/5/96	120	25	4
13/6/96	120	100	16

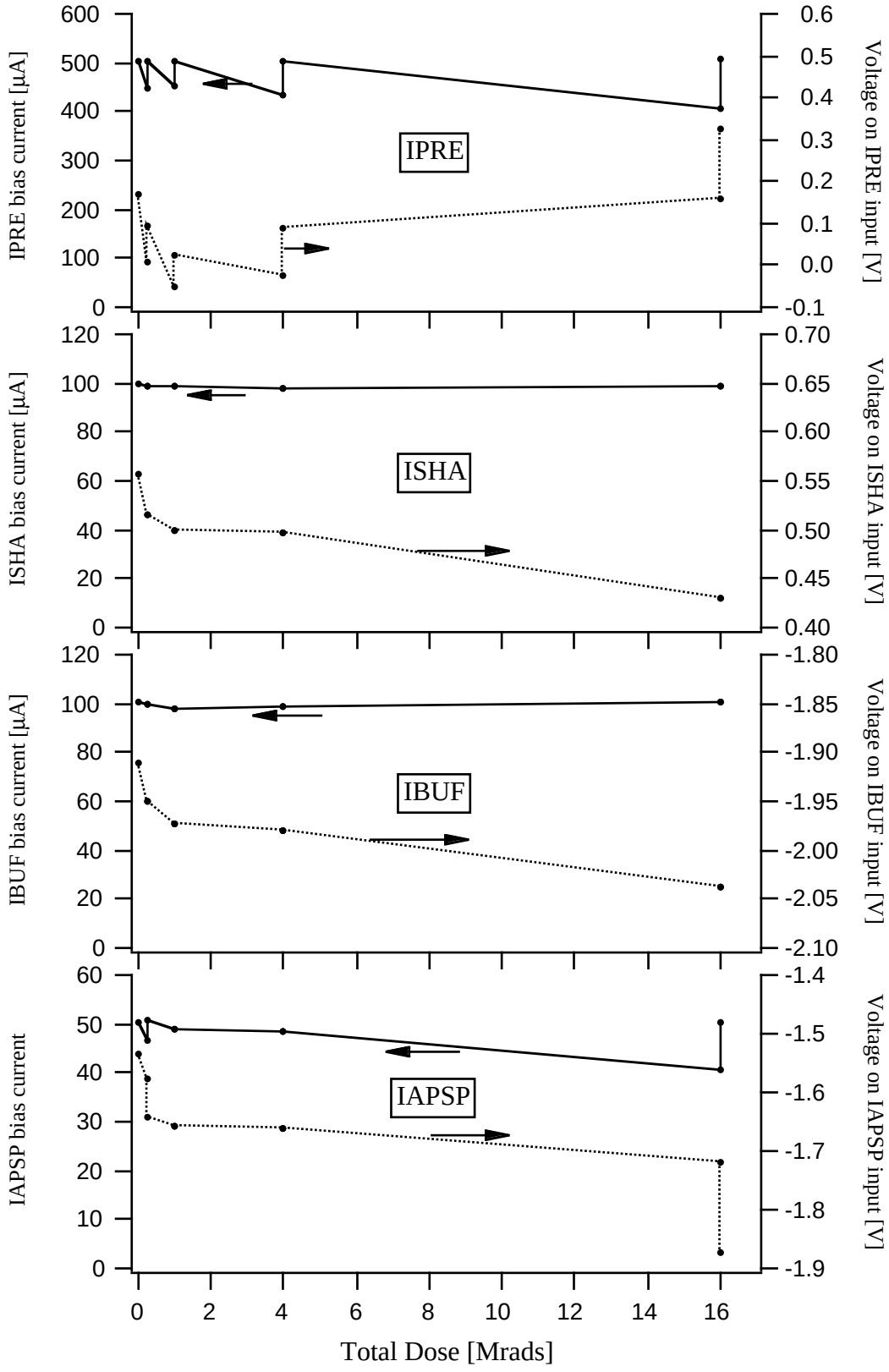
4. Measurement methods and results

For the purposes of measurement the APV5 PCB was transferred to the lab where the output data stream could be digitised by a data acquisition system consisting of a CAMAC ADC interfaced to a VME crate conrolled by a Macintosh running LabView. Data were acquired by triggering the chip repetitively (pulsing the T1 line) and digitising the resultant output data streams, allowing large data sets (typically up to 10,000 triggers) to be accumulated for processing and analysis. The APV5 PCB included a facility to inject signals directly into 12 of the 128 input channels allowing the amplifier pulse shape to be determined individually for these channels. The method used here was to fix the T1 latency and sweep the charge injection time in incremental steps such that the amplifier output pulses were sampled into the pipeline over the full duration of the analogue pulse. Averaging a number of values read out for each step increment allowed an average pulse shape to be recorded for each of the 12 channels. The noise of all channels was determined by a statistical analysis of data accumulated for 10,000 triggers.

4.1 Bias Settings

After each irradiation step the bias settings to the chip were examined to see whether any DC shift had occurred as a result of the accumulated dose. Figure 2 shows the results for four of the bias current settings throughout the whole irradiation procedure. To explain the form of these graphs let us take, for example, the top graph which shows the picture for the IPRE bias current:

Figure 2. APV5 bias current values during the irradiation



Initially (pre-irradiation) IPRE was set to 500μA and the actual voltage at the input to the chip was recorded. After the first irradiation step IPRE was found to have fallen to approximately 450 μA and the corresponding voltage at the chip input had also dropped. Before re-evaluating the chip IPRE was trimmed back to the desired value and the voltage re-measured. This procedure was repeated after each irradiation step, which accounts for the saw-tooth shape evident in the bias current data. The movement of the voltage on the IPRE input to the chip reflects the shifting of the primary current mirroring transistor threshold voltage.

The graphs for ISHA and IBUF in figure 2 show that these two currents did not require adjustment throughout the whole irradiation period, even though the chip input voltages for these two currents did shift significantly. The IAPSP bias current did require re-tuning twice, once after the initial 250 krads and again after the end of the final irradiation.

There is a noticeable difference in the form of the graphs between the IPRE results and the other three which can be attributed to the polarity of the device used for the primary current mirror. For the IPRE input this device is NMOS whereas it is PMOS for the other three.

To summarise, the current bias settings to the chip were adjusted to the initial values (table 1) following each irradiation before the noise and analogue pulse shape measurements were performed. For the voltage biases the value of VFP remained constant throughout, the value of VFS being adjusted if the pulse shape had altered significantly after the irradiation. The value of ISHF did alter during the irradiation but was adjusted automatically to maintain zero current in the VREF line.

4.2 Pulse Shape

Figure 3 shows the average analogue pulse shape for three typical channels of the APV5, obtained using the method described above. For the pre-irradiation case it can be seen that the gain (pulse height) varies from channel to channel, which is a problem previously identified with the APV5 [2]. The pulses shown are for an input test charge of 23,750 electrons (2mV test pulse on a 1.9pF capacitor) in each case. The pulse heights can be seen to decrease after each irradiation step. It was found necessary to retune the pulse shape using the VFS bias input after the second step (1 Mrad cumulative dose) and again after the final step (16 Mrads). Although not obvious from figure 3 it was not possible to exactly reproduce the pre-irradiation pulse shape after 16 Mrads because VFS had reached the limit of its adjustment range. After investigation this was found to be due to the fact that the pre-irradiation pulse shape was actually rather shorter (too steep a fall time) than for an ideal 50 ns CR-RC shape, so in fact the range of adjustment available for VFS was adequate after all. This is illustrated in figure 4 which shows the pulse shape for channel 2. The loss in pulse height after irradiation can be attributed to the reduced gain of the NMOS transistors in the shaper and pipeline buffer stages. Increasing ISHA and IBUF by approximately 50% each restored the pulse height to the pre-irradiation value. The pulse shape was then adjusted to closely approximate the ideal 50 ns shape which is included in figure 4 for comparison.

Figure 3 APV5 amplifier pulse shape dependence on dose

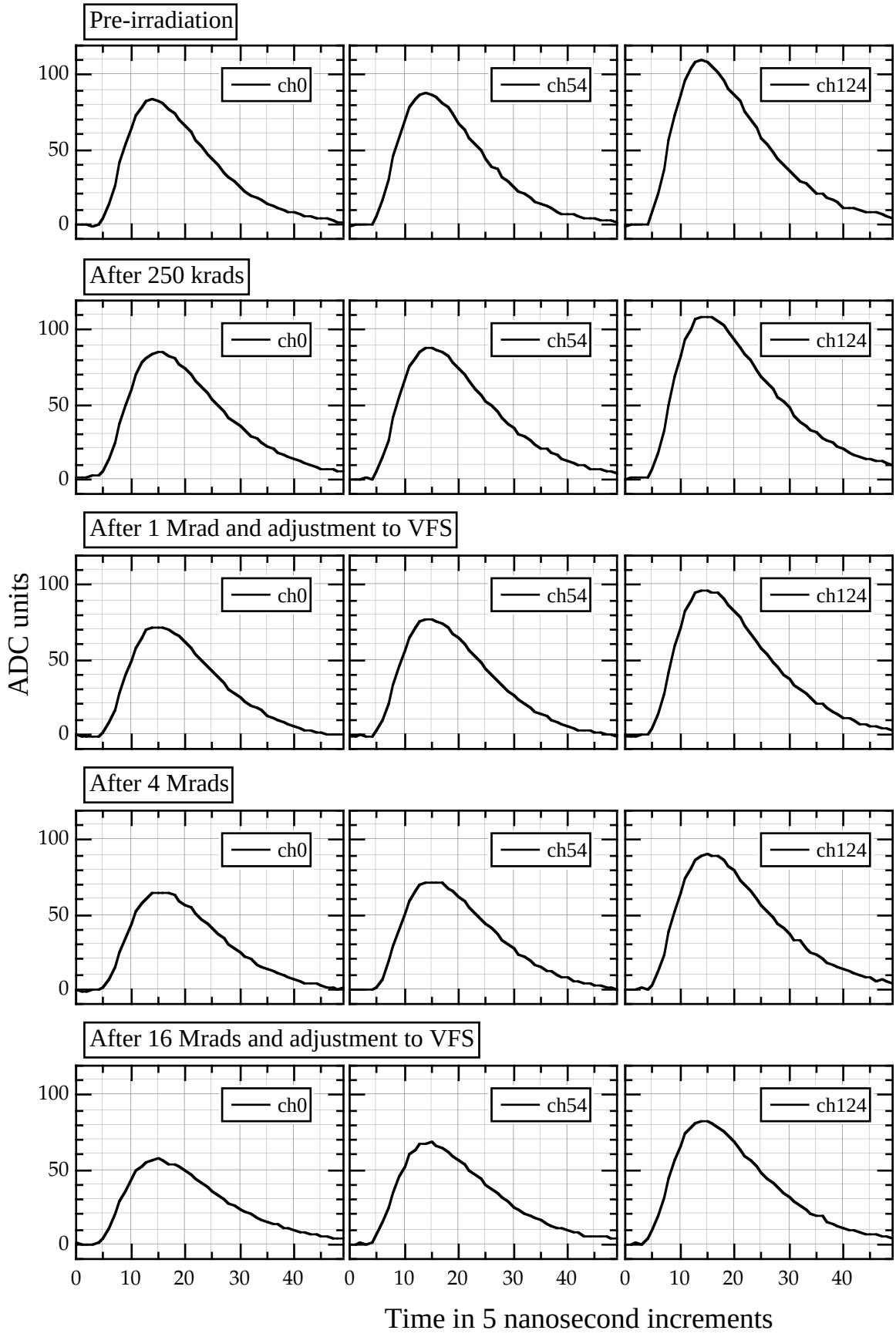
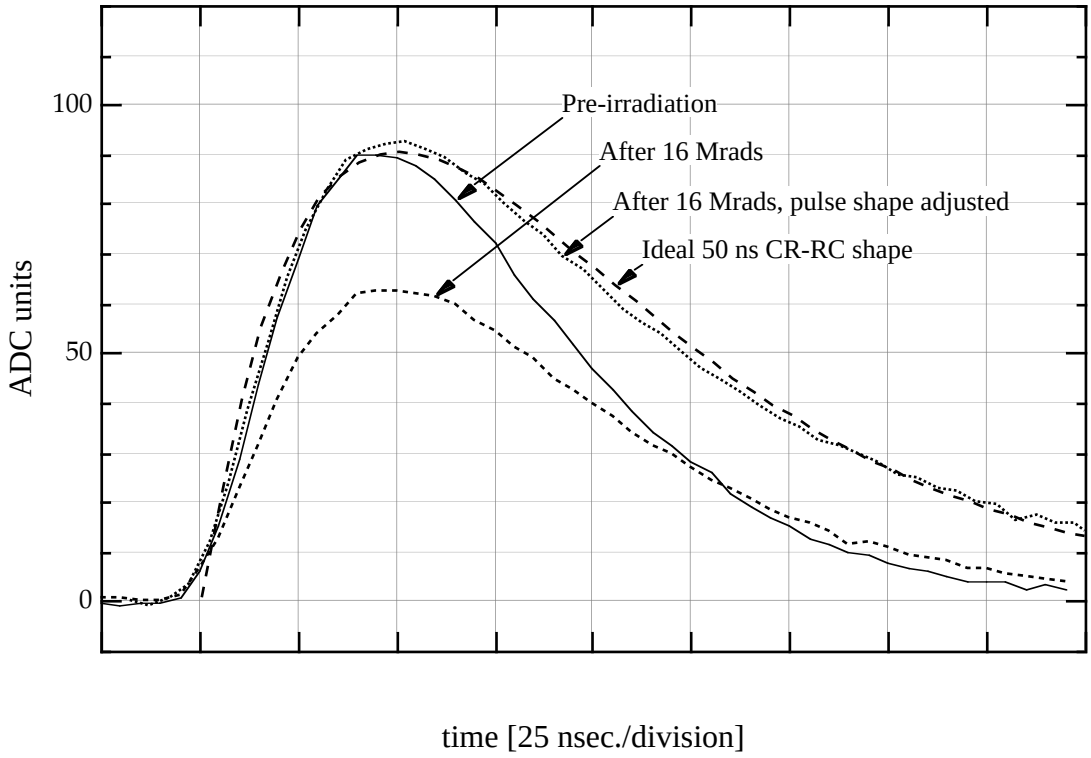


Figure 4. Pulse shape for channel 2, before irradiation, after irradiation and after adjustment to correct for gain reduction and fall time



4.3 Noise

The primary purpose of this work was to to verify functionality of the APV5 after irradiation and hence a detailed investigation of the noise performance of the chip was not included in the tests. Nevertheless the noise performance is of interest and a limited set of measurements were made to investigate this parameter. These measurements consisted of evaluating the noise of the bare chip (i.e. no added input capacitance) for all channels after every irradiation step. The results are shown in figure 5 where the individual channel noise for all 128 channels and the frequency distribution of the noise values are plotted for each irradiation step. The noise can be seen to increase slightly as the cumulative dose increases up to 4 Mrads, and then fall slightly after 16 Mrads with an increased channel to channel variation. As expected from previous studies [2] the noise is dominated by the APSP contribution, which is demonstrated in figure 6 where the noise after 4 Mrads is shown before and after the pipeline buffer is switched off (thereby removing the front end amplifier contribution). The increased spread of the noise values after 16 Mrads is not fully understood, but might be attributable to adverse effects caused by the loss of bias during the final irradiation step. In any case the noise is not substantially increased after the full 16 Mrads.

Figure 5. Noise of all channels dependence on dose

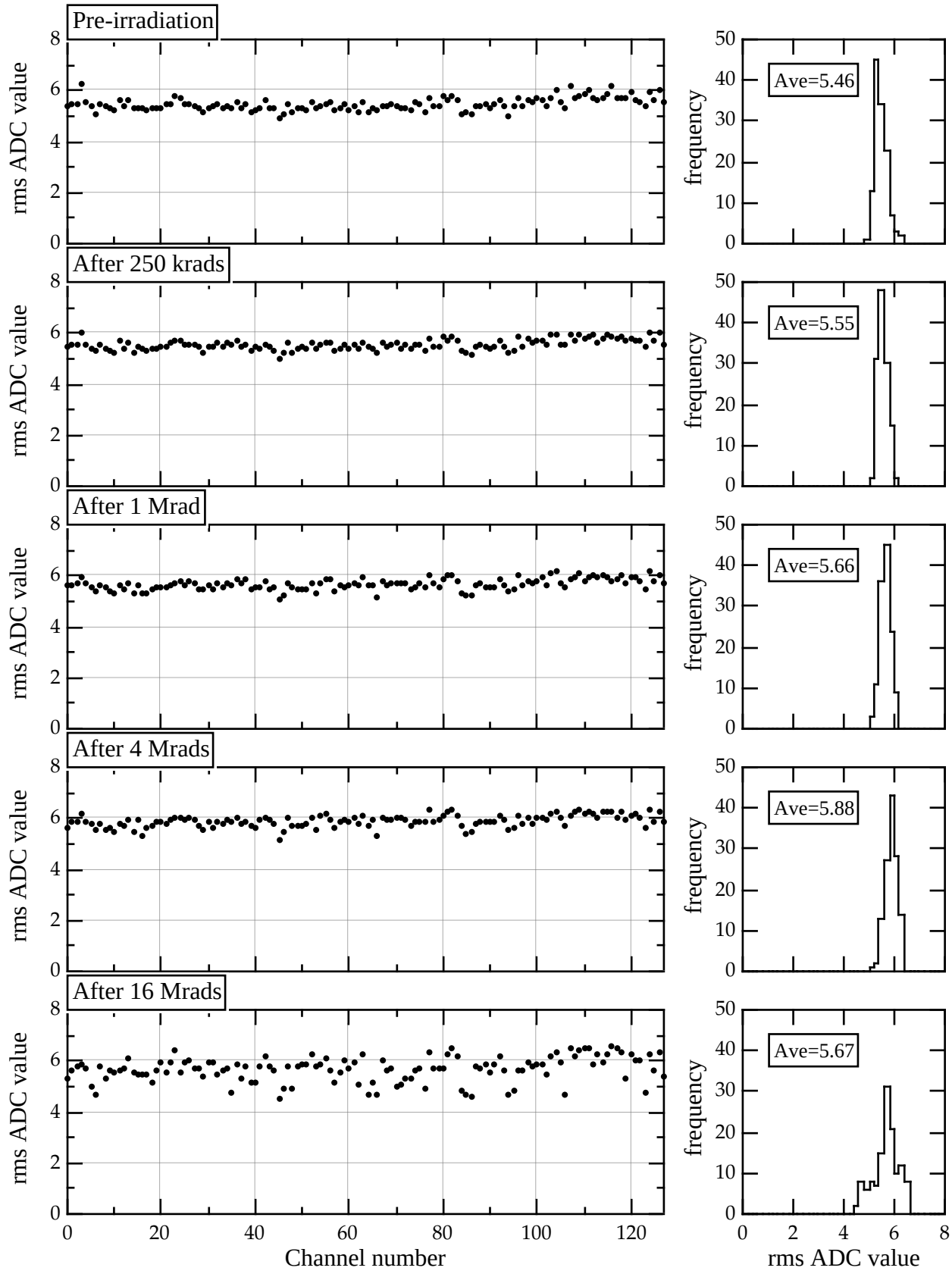
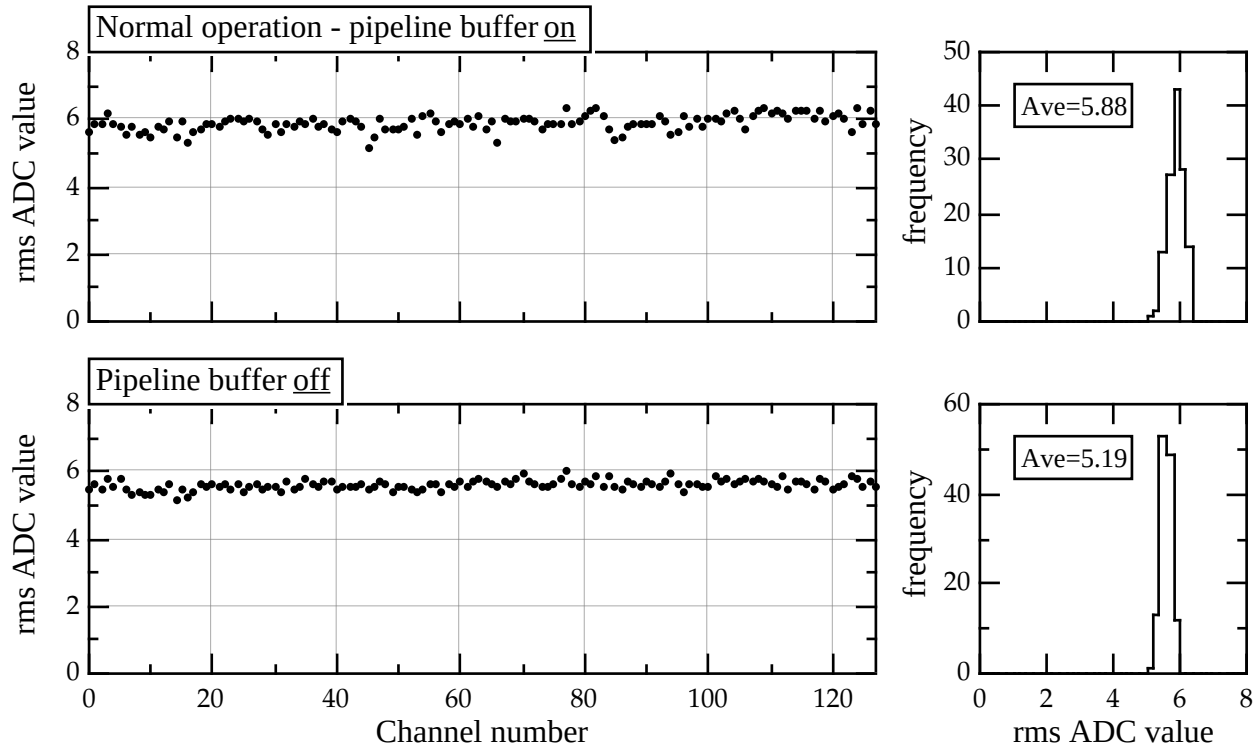


Figure 6. Noise dependence on channel number after 4 Mrads



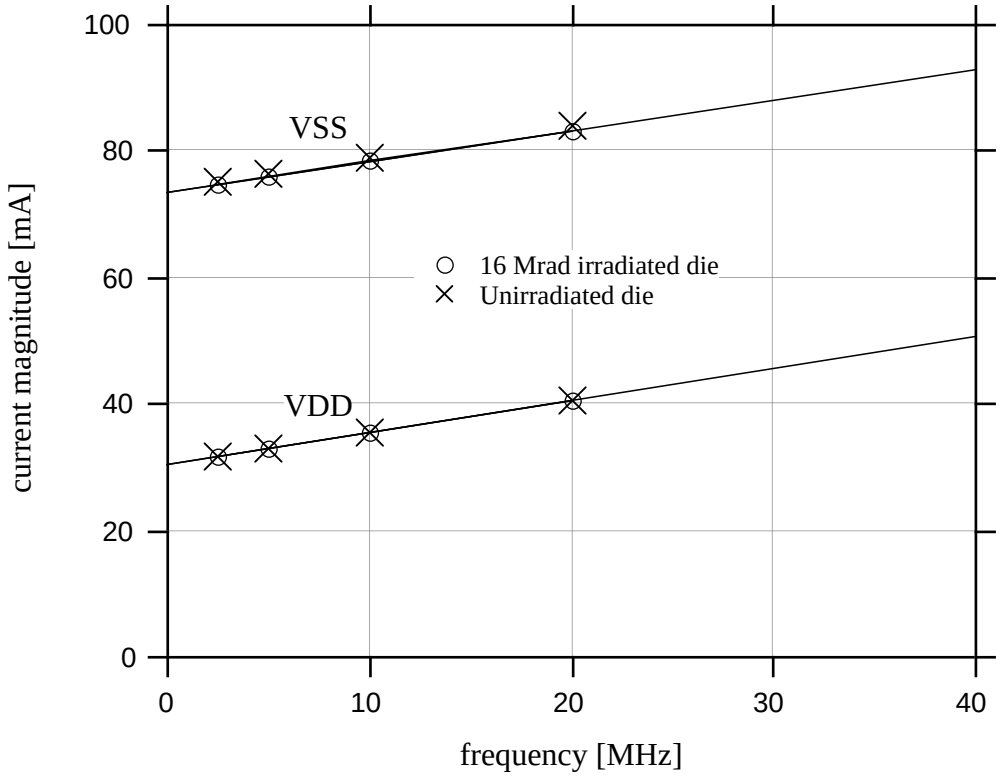
5. Power consumption

Figure 7 shows the current measured in the VSS (-2V) and VDD (+2V) power supply lines to the chip as a function of chip operating frequency. Two sets of data are included, for both the 16 Mrad irradiated die and an un-irradiated die. Both die were biased identically and close agreement in current consumption can be seen, indicating that the effect of irradiation on power consumption is negligible. The current in both lines shows the same increase with frequency, as would be expected since the digital circuitry operates between the +/- 2 Volt rails. The data can be seen to be linear and a straight line has been fitted and extrapolated to 40 MHz. The zero frequency intercepts are consistent with the calculated power consumption for the particular choice of analogue bias levels.

6. Conclusion

An APV5 chip has been irradiated to 16 Mrads with no loss of digital functionality. The front end amplifier gain reduces with dose, but can be compensated for by increasing the bias currents to the NMOS transistors in the shaper and pipeline buffer stages. This is expected from previous individual transistor measurements, and will not occur in the APV6 where the critical transistors have been replaced by PMOS devices. The noise performance of the chip is not substantially affected by irradiation, but in any case is dominated by the expected APSP contribution. This has also been rectified in the APV6 design. The power consumption is also unnaffected by irradiation.

Figure 7. APV5 power consumption dependence on clock frequency



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