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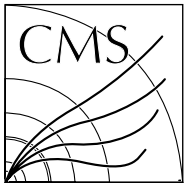

**The Compact Muon Solenoid Experiment**

# CMS Note

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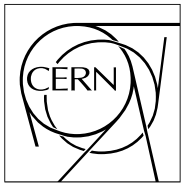

**2 July 2002**

# Compensation for the settling time and slew rate limitations of the CMS-ECAL Floating Point Preamplifier

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**Abstract**

The Floating Point Preamplifier of the Very Front End Electronics for the CMS Electromagnetic Calorimeter has been investigated on a 5×6 crystal prototype matrix. Discontinuities at the signal peak were observed in the pulse shape reconstruction from the 40 MHz sampled and digitized data. The propositions linked to those observations are described, together with a focalized overview of the detector readout chain. A settling time problem is identified and it is shown that a 5 ns delay applied to the ADC clock provides a secure solution. Finally, the implementation in the FPPA design of this delay is presented.

## 1 Introduction and hardware overview

The CMS electromagnetic calorimeter is a compact detector built out of more than eighty thousand lead tungstate ($PbWO_4$) crystals in its barrel and endcaps, which operates in a severe radiation and high magnetic field (4T) environment [1]. The present paper concentrates on the barrel, where the light collection is performed by high quantum efficiency avalanche photodiodes (APDs) with a nominal gain of 50, required by the low light yield of $PbWO_4$ crystals (5.5 p.e./MeV with 0.25 $cm^2$ APD pairs[2]). The Very Front End (VFE) electronics processes, in parallel, the signals from the APDs of 5 neighbouring channels in $\eta$. It amplifies them in multi-gain stages and outputs sampled, digitized data.

Shaping is performed by a low noise (10k electrons $\cong$ 36 MeV[1] for a 200 pF detector capacity) transconductance preamplifier with a design gain of 33 mV/pC[2] over the full dynamic range and a 43 ns peaking time for a $\delta$ input charge. In order to achieve a good resolution in the 90 dB dynamic range up to 1.5 TeV with a commercial 12-bit radiation hard ADC[3], a compression of the signal is needed [1]. It is performed by a Floating Point Unit (FPU) working at 40 MHz, which includes a 4-gain amplification, combined with track&holds (T/H)[4], comparators and an analogue multiplexer. The preamplifier together with the FPU are integrated in an ASIC called Floating Point Preamplifier [3] (FPPA : current release 2000), which is packaged in a 52-pin Quad Flat Pack. At each clock count, a gain is selected by the comparators. Its output is digitized by the ADC, serialized together with gain information in a 20-bit protocol.

In a test setup, the VFE electronics cards are mounted on a 5×6 crystal prototype matrix and optically linked to the Upper Level Readout (ULR) with opto-electronics by Siemens[5]. In this way the entire readout chain can be tested. The light from a 1 ns-pulsed green laser is monitored by an independent system and distributed via optical fibers to each single crystal. The pulse shape is reconstructed from the digitized data read by the ULR of numerous events readjusted with respect to the peak, making use of the trigger dispersion along a clock period.

Observation of the reconstructed signal showed a discontinuity in the vicinity of the peak —see section 2.3. A gap appears exactly one clock period after a gain switch. Studies indicate the origin of the problem to be a settling time limitation after gain switch. The ADC clock fixes the sampling instant, whereas the FPPA clock governs the gain switches. Measurements show that a 5 ns delay applied to the ADC clock with respect to the FPU clock removes the observed discontinuities.

In this paper, the propositions and the solution are discussed first. Then a series of measurements aimed at revealing the consequences of the delay are described. Finally, a possible implementation of a delay for the next release of the FPPA is presented.

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[1] The current noise is about four times higher. The main causes are understood at the simulation level. The next release of the FPPA is expected with a noise at design value.

[2] The current gain is 24 mV/pC, due to a modification of the feedback capacitor in order to correct undershoot defects.

[3] AD9042 : 12 bit, 41 MSPS monolithic A/D converter, Analog Devices Inc.

[4] is sometimes referred to as sample&hold (S/H).

[5] V23814(5)-K1306-M130 for TX(RX). Consult `http://www.siemens.com`.

## 2 Propositions and Solutions

### 2.1 Functionning principle of the FPPA

The signal from the preamplifier is amplified by four parallel amplifiers of different gain values. Design gain ratios are 33, 9, 5 and 1[6] [3]. At each clock, the logic chooses the highest gain whose signal fits into the specified range and multiplexes it out to the ADC for digitization.

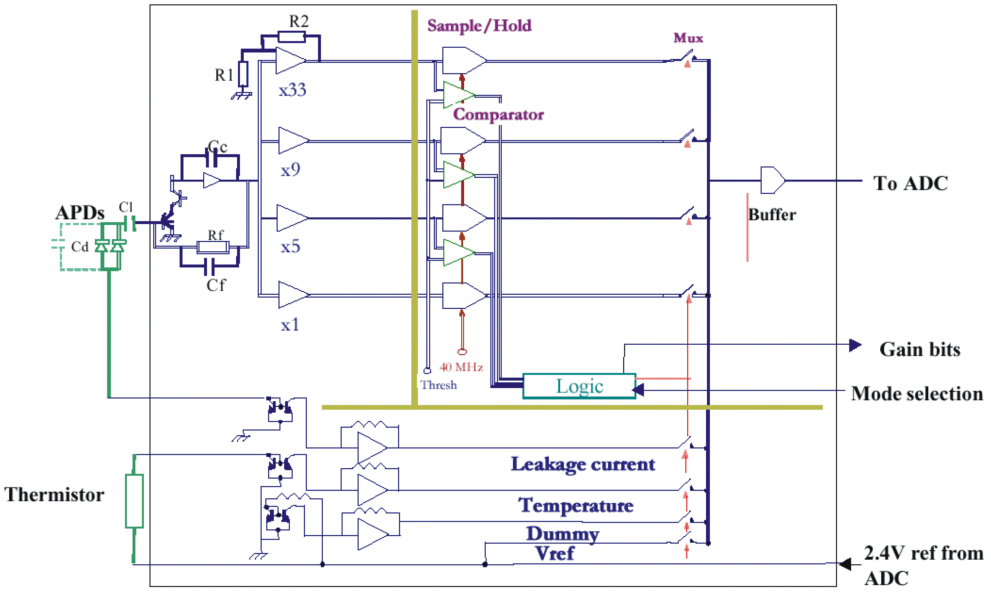


**Figure 1:** Block diagram of the FPPA [3].

The ideal behaviour of the FPPA is illustrated in Figure 1, which shows a block diagram of the FPPA from the preamplification stage down to the output buffering towards the ADC. The four-gain stages are represented in the upper part of the figure. The gain 33 amplifier is shown with the internal resistors fixing the gain. The T/H's are responsible for tracking the signal during the first half-period of the clock and thereafter holding the value for the second half-period. At the end of the track, the amplified signals are compared with a threshold set at 80% of the ADC full range. The highest signal which does not exceed the threshold is selected by the logic controlling the multiplexer (Mux). The hold period, where the signals are stable, is used for the gain switching. The selected signal is to be stabilized for digitization at the output buffer at least 1 ns before the end of the hold period.

### 2.2 Effective functionning of the FPPA

The effective behaviour of the FPPA is demonstrated in Figure 2, which is a snapshot taken from a digital oscilloscope with an analogue bandwidth of 1.5 GHz —used throughout this study. The output of the FPPA and the clock at the ADC are measured with a 10 pF / 10 MΩ

[6] The current gain ratios are measured to be 22, 6.21, 3.55 and 1. The cause is understood at the simulation level as parasitic resistance in the feedback strips of the gain amplifier. The next release of the FPPA is expected with gain ratios at design values.

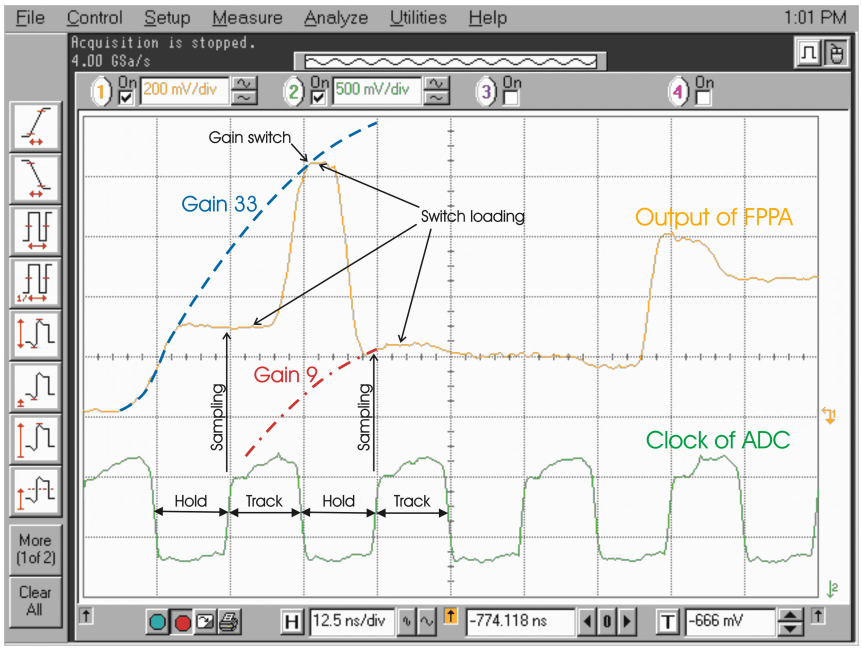


**Figure 2:** Snapshot from a 1.5GHz bandwidth digital oscilloscope. See next paragraph for details.

probe. They are displayed in the upper (orange) and lower (green) signals, respectively. The signals after amplification by gains 33 and 9 are superimposed with (blue) dashed and (red) dashed-dotted lines, respectively.

The track and hold half-periods are fixed by the FPU clock. (Note that the ADC clock is regenerated from the FPU clock with a ~1ns delay, which is not shown in the figure.) To switch from hold to track mode takes around 5-6 ns and during this time —referred to as the 'physical' hold in this paper— the output signal is stable. The effective tracking lasts for a short period of 1-3ns. At the end of the first annotated track, the FPPA is switching from gain 33 to 9. A similar delay is observed for the switching of the multiplexer. Another 5-6ns are needed to catch up with gain 9 within the hold half-period of 12.5ns. Immediately after its settling, the signal is sampled by the ADC. No time is available for settling.

### 2.3 Observation of discontinuities

The prototype matrix allows tests of the electronics, as well as for the development of calibration and signal analysis tools. Runs of typically 1k events are taken. The facility to adjust the laser intensity is used, together with the FPPA different working modes. Single fixed gains can be forced on all samples or be freely chosen by the FPPA logic in the so-called auto mode. The reconstruction and comparison of pulse shapes from various modes and different laser intensities have revealed problematic behaviours of the FPPA which have been further investigated.

Figure 3 shows the pulse shape of a single crystal channel from a run[7] in auto mode with a laser intensity such that the gain 5 saturates. The intergain gaps are striking. They appear

[7] All run information and data are available from the web-site `http://suncms100.cern.ch`.

three times, both on the rising and falling edges. These are assumed to be due to slew-rate limitation of the gain amplifiers. They appear with green laser light pulses which are fast — shorter than 1 ns. Test-beam observations on the FPPA 98 showed that the convolution of the slower pulse from scintillation light fills in these gaps. Similar behaviour is expected with the subsequent releases.

The issue discussed in this paper is related to the discontinuities, observed close to the peak of the signal, as well as in the middle of all gains. These occur always one clock period (25 ns) after change of the gain amplifier to which the signal is multiplexed. The first sample after a gain switch differs from the corresponding sample in forced-gain mode. Moreover, the rising edge shows an overestimation of this first sample, whereas the falling edge shows an underestimation.

When used in the LHC environment, the phase of the ADC clock will be adjusted to take one sample at the peak of the signal. The value of this sample should, taking the pedestal into account, be a linear function of the deposited energy. However, if artefacts as described above occur, the resolution of the measurements at the peak of the signals will deteriorate to unacceptable levels.

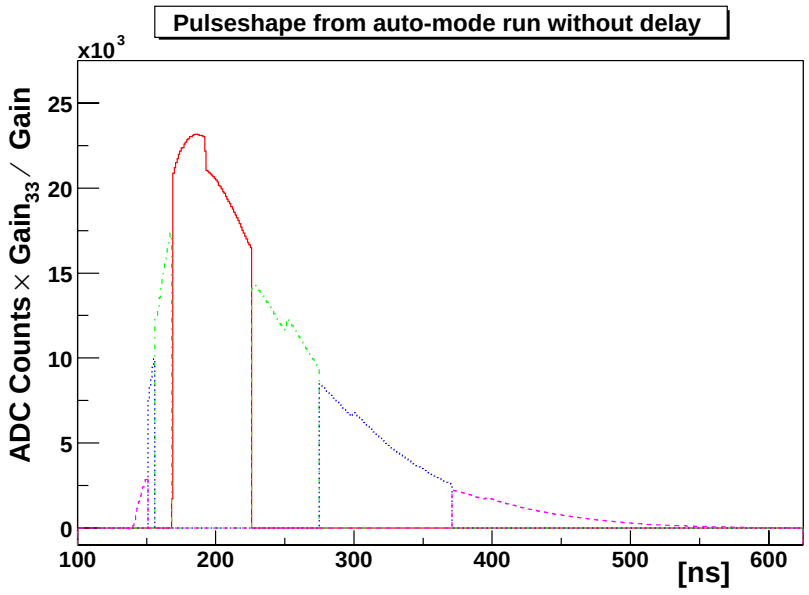


**Figure 3:** Reconstructed pulse shape for FPPA nº2690 (crystal nº12 out of 30 counting from 0) from laser run no. 11148 in auto mode. Pulse shapes are reconstructed from four gains according to the gain ratios given in the text. Gains 1, 5, 9 and 33 are displayed in continuous (red), dotted-dashed (green), dotted (blue) and dashed (magenta) lines, respectively.

### 2.4 Origin and solution

The observations described in the previous section indicate that the sampling occurs while the signal is still settling after a gain change has occured. Figure 2 is a measurement performed at the output of the FPPA. The signal is displayed together with the ADC clock, sampling at its rising edge. The first sample after the gain switch is taken, in the hold period, when the signal is not yet settled. Our assumption is that the sampling might occur even

earlier. For the sample at which the gain switching takes place, this would lead to an overestimation of a sample placed on the rising edge of the signal. On the other hand, a gain switch in the falling edge of the signal would lead to an underestimation for the same reasons.

Following this hypothesis, the problem would be alleviated if the sampling instant was delayed in order for the signal to settle and stabilize. The idea is to take advantage of the 'physical' hold which lasts beyond the hold period because of the switch delay. A 3 to 5ns delay applied to the ADC clock should be sufficient to remove the observed discontinuities.

# 3 Measurements

## 3.1 Delay Setup

The clock used by the ADC is derived from the FPU differential clock. Its phase with respect to the latter is adjusted with the help of a high speed digital buffer amplifier (HEL 16), which is connected as described in Figure 4. The buffer introduces a 1ns delay. It drives a pair of twisted wires —not shown in the figure— whose length determines the clock delay. Figure 5 shows a 5ns phase delay of the clock at the level of the ADC with respect to the FPU, as measured by the oscilloscope.

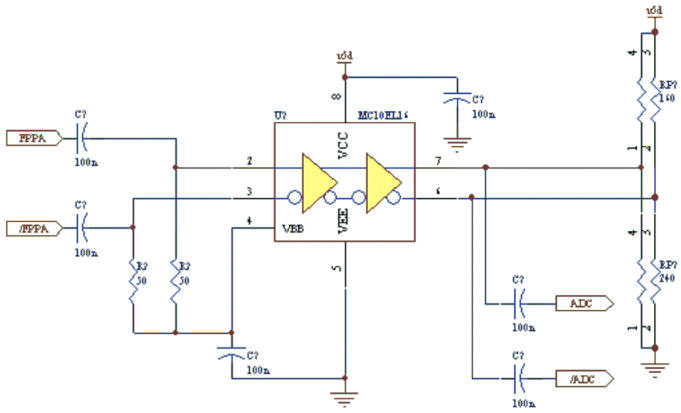


**Figure 4:** Schematic layout of the delay between ADC and FPU clock [5].

## 3.2 Shape observation with delay

The adjustment of the clock phase at the level of the ADC ensures that the sampling occurs after the signal is stabilized following a gain switch. At this point the signal is still to be physically held. Measurements showed that a 5ns delay is sufficient to remove the mid-gain discontinuities. A 3ns delay does not fully fill in the gaps, while a longer delay would distort the pulse shape. Figure 6 shows a pulse shape reconstructed from the same readout channel as in Figure 3 with equal laser intensity, but with a 5ns delay added. The gaps are strongly reduced. Identical results were obtained from the analysis of three other channels, both on the same and on a different card.

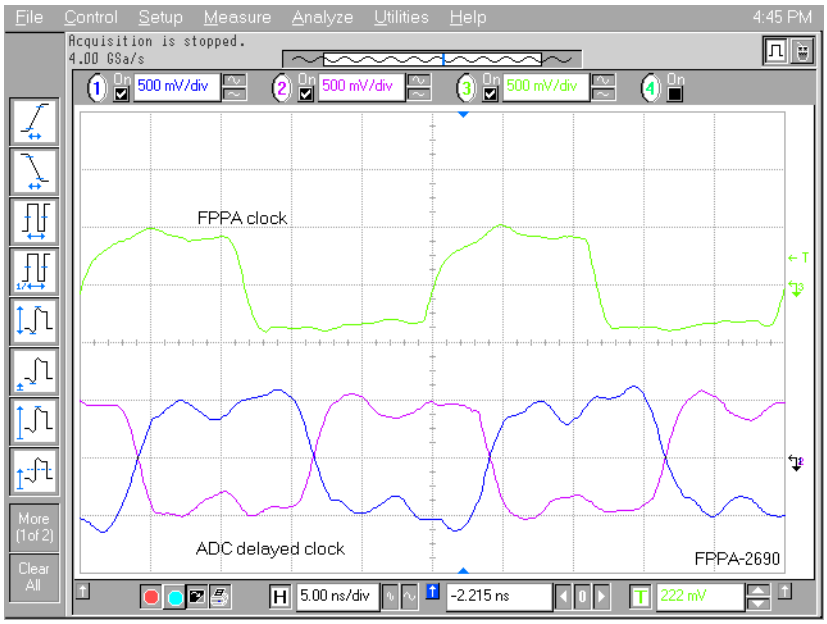


**Figure 5:** 4ns delayed clock at the level of the ADC with respect to the FPU.

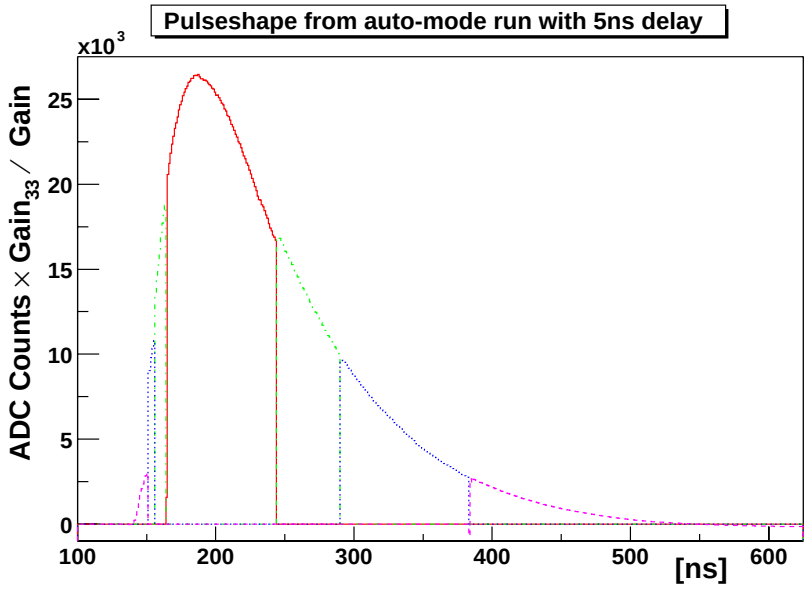


**Figure 6:** Reconstructed pulse shape for FPPA nº2690 (crystal 12 out of 30 counting from 0) from laser run no. 11153 in auto mode. Pulse shapes are reconstructed from four gains according to the gain ratios given in the text. Gains 1, 5, 9 and 33 are displayed in full (red), dotted-dashed (green), dotted (blue) and dashed (magenta) lines, respectively.

### 3.3 Pulse shape integrity in forced-gain mode

The stability of the 'physical' hold might be compromised by the $dV/dt$ of the signal in the T/H switches, in particular in the rising edge. When a delay is applied to the ADC clock, the sampling might occur at an instant where the hold is not stable. As a consequence, the pulse shape would be distorted with regard to its original shape without delay.

Comparisons of pulse shapes from configurations with and without delay allow us to unveil such a phenomenon. Two runs of equal laser intensity were acquired in forced-gain mode. The reconstructed pulse shapes were subtracted from their pedestal and normalized with respect to their maximum; then subtracted from each other.

Care was taken that no time shift was introduced between both pulse shapes. Therefore peaking time and height were determined by means of a 4th-order spline interpolation[6] applied on a 2.5ns binning. Then the shapes were time readjusted —typically a tenth of a nanosecond— before being subtracted.

Figure 7 shows the result of the analysis of a forced-gain-1 data acquisition, which is representative of the behaviour of all gains. The application of a delay clearly underestimates the sample values in the rising edge by up to 3.5%, and overestimates them in the falling edge by up to 0.5-1%. The maxima exactly match each other due to the normalization. Therefore the shape is biased, but the main point is the peak linearity, which is addressed in the next section.

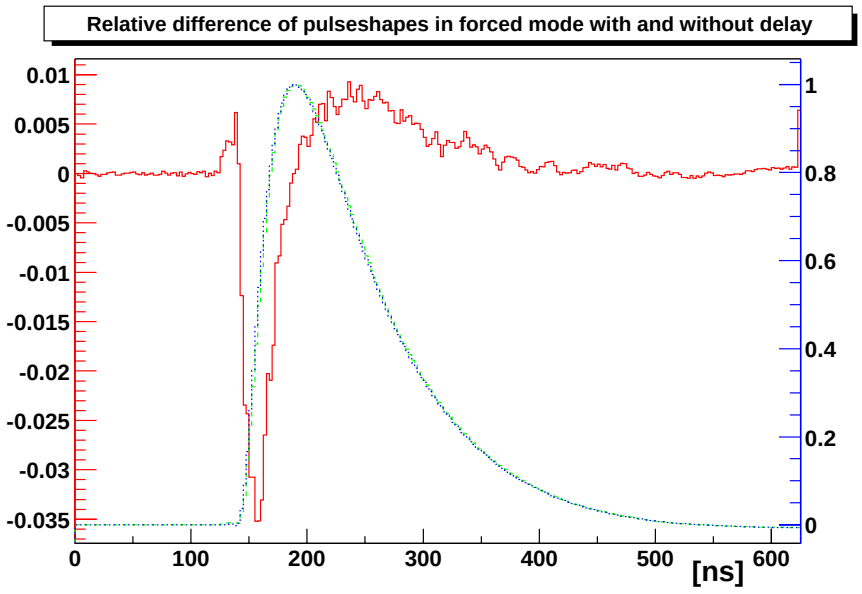


**Figure 7:** Relative difference of normalized and time readjusted pulse shapes with and without delay from runs (11212 and 11229) of equivalent laser intensity in forced-gain-1 mode on FPPA nº2690 (crystal 0+12 /30). The difference is shown in the (red) continuous histogram with its scale on the left side. The pulse shapes in auto and forced-gain mode are represented by the (green) dashed and the (blue) dotted lines, respectively, with their scale on the right side.

### 3.4 Linearity

A major concern is the conservation of the peak height linearity when a delay is applied to the ADC clock. The comparison of runs acquired in forced-gain mode allow us to measure whether the linearity is deteriorated.

Figure 8 shows the relative difference in peak height with and without delay as a function of laser intensity. It is computed from two ramps in laser intensity covering a major part of the dynamic range in forced-gain-1 mode. The laser intensities are read from the data acquired by the laser monitoring system. A 4th-order spline interpolation is used to adjust both ramps in laser intensity for the peak height subtraction. A mean relative difference of -1.7 % (±0.4%) is observed, which is constant over the entire range. Thus one can conclude that the linearity is not degraded in forced-gain mode by the delay.

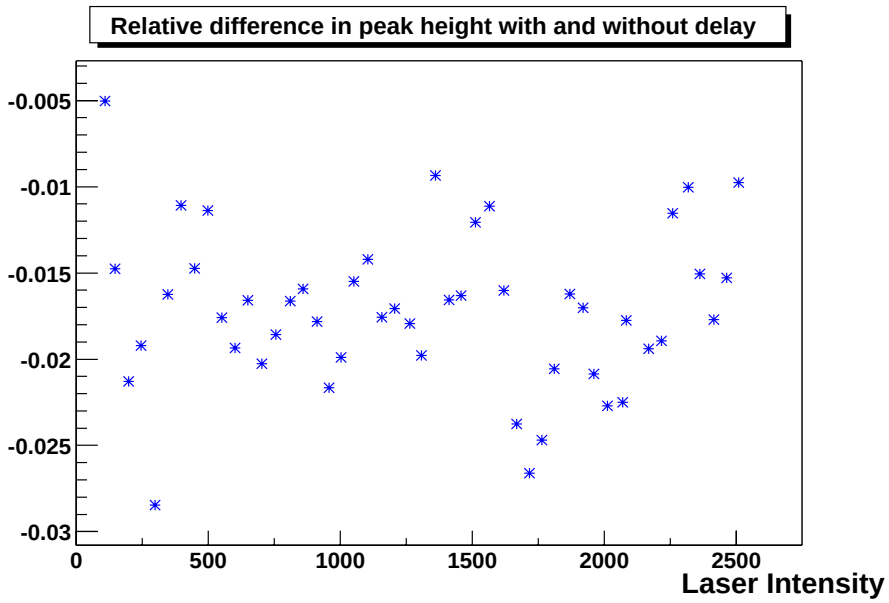


**Figure 8:** Relative difference in peak height as a function of laser intensity from two runs (11305 and 11311) on FPPA nº2690 (crystal 0+12 ⁄30) in configurations with and without delay.

### 3.5 Pulse shape integrity in auto mode

The reconstructed pulse shapes in auto mode are smoothed —as shown in Figure 6— by the application of a 5ns phase shift to the sampling clock. It is now possible to compare these to the forced-gain mode pulse shapes, which in principle are their building blocks. This study checks the consistency of the FPPA operation, since it observes the conservation of the pulse shapes from forced-gain to auto mode. To the first order, this observation is independent of the preamplifier shaping. It will still be valid for the next release of the FPPA, where some modifications will be introduced in the preamplifier only.

A sequence of five runs were performed in auto mode and in all four forced-gain modes with identical laser intensity. A pair of pulse shapes, which correspond to acquisitions in forced-gain and auto mode, are reconstructed from all gains in their proper selection ranges. They are pedestal subtracted —the pedestal values for the other gain ranges are obtained

from the first using the known pedestal ratios. They are not normalized, in order to highlight the distorsion at the peak. For the same reason the pulse shapes are not time readjusted to each other as in section 3.3. The forced-gain mode pulse shape is subtracted from the auto-mode pulse shape and then normalized with respect to the peak height.

Figure 9 presents the result of such an analysis. The subtraction is shown in the continuous histogram on which the pulse shapes in forced-gain and auto mode are superimposed. Globally, the auto-mode acquisition underestimates the sample values. The effects of the discontinuities are observable at the times 190ns and 240ns where the pulse shape in auto mode is flattened and reduced by 1.5-2%.

It follows that the pulse shape in auto mode is still affected by a gain switch when a delay is applied to the ADC clock. The forced-gain mode pulse shape is not completely recovered, especially at the peak. The delay strongly reduces the discontinuities, it does not eliminate them.

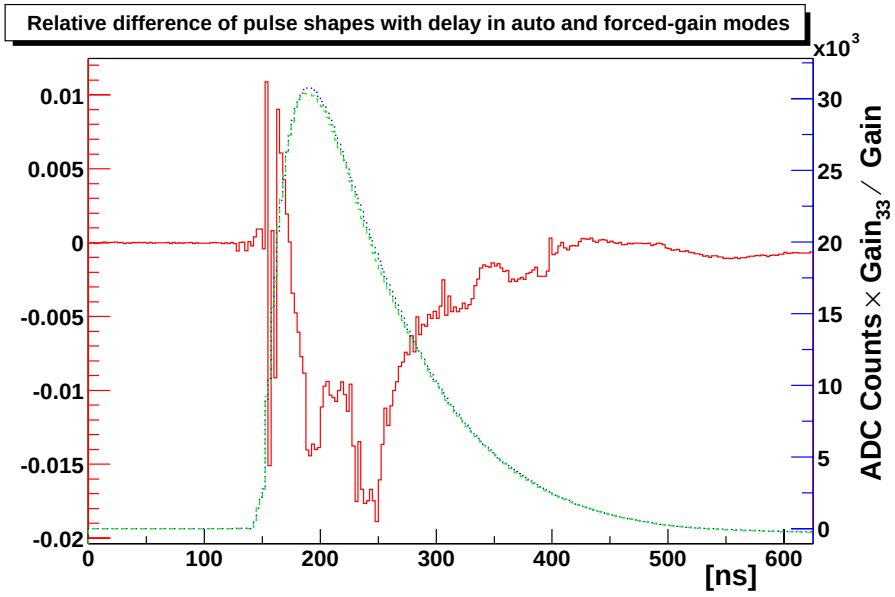


**Figure 9:** Relative difference of auto mode (run 11192) and forced-gain mode (runs 11188, 11189, 11190 and 11191 for gains 1, 5, 9 and 33) pulse shapes from FPPA nº2690 (crystal 0+12 ⁄30), constrained in their proper selection ranges, in case of 5ns delay. The difference is shown in the (red) continuous histogram with its scale on the left side. The pulse shapes in auto and forced-gain mode are represented by the (green) dashed and the (blue) dotted lines, respectively, with their scale on the right side.

### 3.6 Lower clock frequency

The discontinuities observed in Figure 3 are the result of the fact that the FPU system is not able to switch the gains and settle the signal in the time boundaries fixed by the clock. The switching time is proportional to the standing current in the switches. However, the settling of the signal is determined by the settling time and slew rate of each stage of the FPU, from the T/H to the ADC, via the output buffer. The delay of the ADC clock gives the system more time to stabilize before the sampling. It then compensates the limitations in settling

time and slew rate, independently of their origin in the FPU. The effect is equivalent to leaving the ADC clock undelayed, but to lowering the clock frequency in order to increase the time between the switching and sampling operations. Measurements show that a clock frequency lowered to 30 MHz —which corresponds to a ~4 ns delay— fills in the gaps.

Figure 10 shows the relative difference between auto and forced-gain mode acquisition with a system clock at 30 MHz. The result is similar to the case of 5 ns delay, shown in Figure 9. The gaps are filled in equally well. An equivalent flattening is observed at the peak of the pulse by up to 1.5%.

It follows that the reduction of clock frequency acts equally on the discontinuities as the application of a delay on the ADC clock. This equivalence hints at a bandwidth limitation in the inner functioning of the FPU, which limits the performance of the tracking in auto mode.

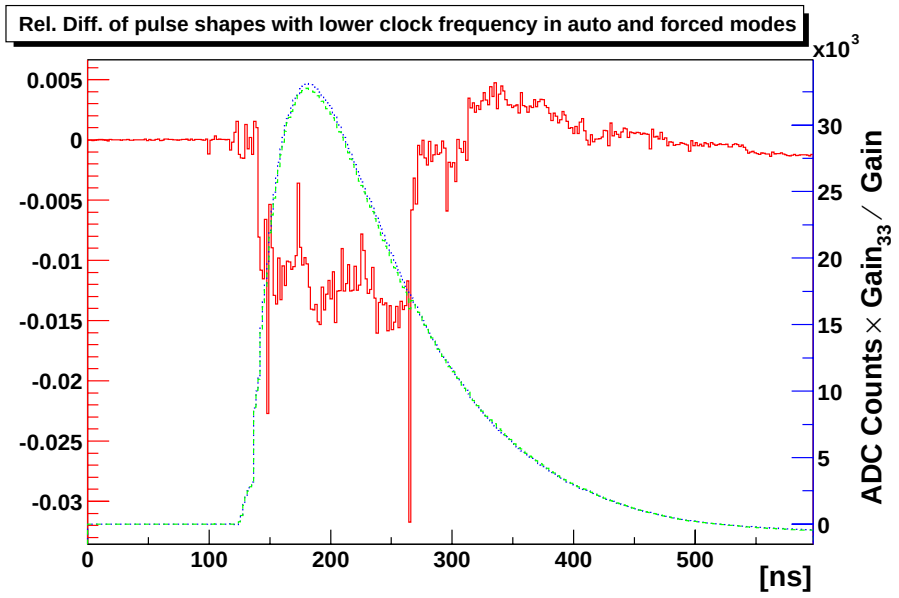


**Figure 10:** Relative difference of auto mode (run 11262) with forced-gain mode (runs 11260, 11259, 11255 and 11261 for gains 1, 5, 9 and 33) pulse shapes from FPPA nº2690 (crystal 0+12 ⁄30), constrained in their proper selection ranges, in case of lower clock frequency at 30 MHz. The difference is shown in the (red) continuous histogram with its scale on the left side. The pulse shapes in auto and forced-gain mode are represented by the (green) dashed and the (blue) dotted lines, respectively, with their scale on the right side.

## 4 Implementation

Following the observations of discontinuities and the results obtained by the application of a delay, simulations have been performed at LBL focusing on the origin of the delay [4]. A four-fold effect was noted. There is a combination of an unwanted delay in the FPU signal at the level of the Mux(i) and of the output buffer(ii), to which a large settling time(iii) is added, and a slew rate limitation(iv) in the switches.

The decision was taken to implement a variable delay in the next release of the FPPA. The FPU clock will be supplied with a fixed delay of 6.2ns and the ADC clock delay will be adjustable by an external resistor. In this way the system will allow a relative phase shift of the ADC clock with respect to the FPU clock between –1ns and 6ns. Figure 11 shows the diagrammatic scheme of the new clock distribution for the next release of the FPPA.

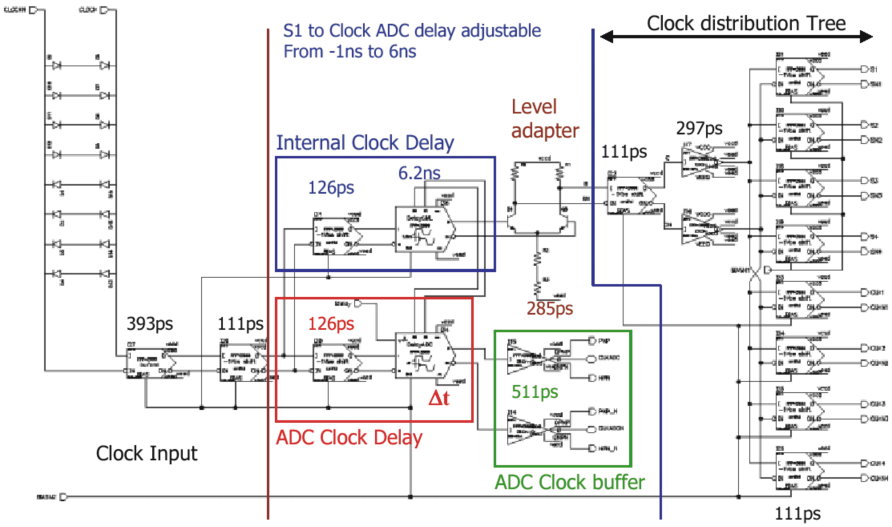


**Figure 11:** Diagrammatic scheme of the new clock distribution for FPPA2001 [4].

## 5 Conclusion

The study presented in this paper shows how the application of a 5ns delay to the ADC clock reduces discontinuities in the vicinity of the pulse peak. The source was found to be a settling time problem at the level of the FPU. The effects of the delay on the pulse shape and on the peak linearity have been analyzed. The delay has been shown to be needed to adjust the ADC sampling. Its implementation in the next release of the FPPA has been presented. It is to be noted that the delay improves the auto-mode behaviour of the FPU, but does not solve the problem of the discontinuities entirely. An effort needs to be made to adjust the electronics system in order to correct the intrinsic causes.


## Acknowledgements

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