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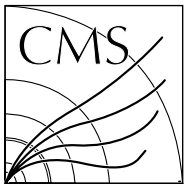

The Compact Muon Solenoid Experiment

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Antifuse-FPGAs for the Track-Sorter-Master of the CMS Muon Barrel Drift Tubes: Design Issues and Irradiation Test

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Abstract

The Track Sorter Master (TSM) is an element of the on-chamber trigger electronics of the Muon Barrel Drift Tubes of the CMS experiment. We describe how the stringent requirements on the TSM can be met with an architecture that makes use of three antifuse-FPGAs. The devices (Actel A54SX), tested with a 59 Mev proton beam, show a radiation tolerant behaviour; we calculate a Single-Event-Upset cross-section upper limit (at 90% c. l.) of $\sigma_{SEU} < 2.9\ 10^{-12}$ cm^2 per A54SX32 chip.

An overview of the trigger electronics [1] of a Muon Barrel Drift Tubes (DT) chamber is presented in figure 1. The system is a synchronous pipelined system partitioned in several Trigger Boards (TB) and a Server Board (SB). In addition there is a Control Board not shown.

A Phi TB contains 37 ASICs:

- 32 BTI (Bunch and Track Identifier) chips: a BTI finds track segments in a portion of one of the two phi Super Layers (SL) of a DT chamber and calculates their impact parameter (position, angle). A good track is put on output with a fixed delay with respect to the beam bunch crossing (BX) in which the originating particle traversed the chamber, thus allowing BX identification.
- 4 TRACO (Track Correlator) chips: a TRACO associates tracks in the inner SL and in the outer SL
- a TSS (Track Sorter Slave) chip: it selects the two tracks with higher quality and smaller angle of impact (i.e. higher transverse momentum) in that portion of a chamber.

There can be up to seven Phi TB in a chamber.

In a Theta TB there are no TRACOs, since there is only one theta SL in a DT chamber.

The SB hosts the chamber Track Sorter Master system (TSM), which delivers the best two identified tracks over a complete DT chamber to the sector Track Finder of the Regional Trigger.

The trigger electronics will be produced during 2001/2002 in order to be ready for the DT chamber installation.

The TSM system functionality has two distinct aspects:

- It performs the final track selection. Together with the TSSs it constitutes a two-stage sorting tree (the Trigger Server) [2] which selects the two best tracks in the chamber
- It interfaces the trigger with the chamber Controller. It handles the read/write access to the trigger elements for configuration and monitoring.

Since the TSM is the last element of the DT on-chamber electronics, the most important requirement in the TSM design is robustness.

Stringent requirements on the sorting process come from dimuon physics and impose high reliability also for the second track delivered to the Regional Trigger. For a 1% contribution of fake second muons in single muon events, the fake dimuon rate becomes comparable to the true dimuon rate. The TSM has to suppress noise and ghosts in a DT chamber, such that the level of fake muons found in the Regional Trigger is smaller than 1%; it should also detect and treat segments assigned to a wrong BX.

Furhermore, the system should fulfil tight latency requirements (3 bunch-crossings).

In order to match the robustness requirement, the system is segmented in blocks with partially redundant functionality. We favour an architecture where the TSM consists of three parts: a Selection (TSMS) block, two Data multiplexing (TSMD) blocks (called TSMD0 and TSMD1, covering half a chamber each) (figure 2). The TSMS receives Preselect Words (PRW) carrying the information of the first stage of sorting performed by the TSSs. The TSMDs have as an input the full TRACO data of the track segments selected by the TSSs.

The TSM can be configured into two distinct processing modes:

- Default processing: the TSMS performs as a sorter while the TSMDs act as data multiplexers. The TSMS can select two tracks in TSMD0 or two tracks in TSMD1 or one track each.
- Back-up processing: the TSMS is inactive. Each TSMD performs as sorter and as multiplexer on data from half chamber. Each TSMD outputs one track.

The Default processing implements the full performance and guarantees that dimuons are found with uniform efficiency along the chamber.

In case of failure of one TSMD, the PRW of the corresponding half chamber are disabled in TSMS sorting, so that full efficiency is maintained in the remaining half chamber.

The Back-up processing mode is activated in case of TSMS failure. It guarantees full efficiency for single muons and for open dimuon pairs (one track in each half chamber).

The sequence of processing operations performed in the Default mode in the three blocks is illustrated in figure 3. Two clock cycles are used, i.e. the total latency is two BXs. Two tracks, one per clock cycle, are presented on the common TSMD output bus. The track selection is performed by the TSMS, which applies the second stage of the sorting algorithm on the PRW data, processed by the TSS during the first sorting stage. The addresses of the selected tracks are used to multiplex the data from the TSMD registers and to enable the three-state output buffers of the corresponding TSMD.

The sequence of processing operations performed in Back-up mode in the three blocks is illustrated in figure 4. In this mode the TSMS is bypassed and each TSMD selects the best track in half-chamber data. Here the selection is not performed on PRW data, instead it is performed on the full track data received from the TRACOs and selected by the TSSs during the first stage of sorting. The quality (3 bits) of the selected track in TSMD1 is compared to the one of the TSMD0 track for enabling the corresponding three-state buffer on output. One track is output per clock cycle. The total latency is two BXs.

Besides performing the second stage of the sorting algorithm initiated in the TSSs, the track selection procedure also applies data masking, ghosts and fakes rejection, in a consistent manner to the TRACO-TSS system. In the TSM, ghost rejection is expanded to a new kind of ghosts: a single good track that produces two segments, one each in two neighbouring TRACOs, which then forward their segments to two different, although contiguous, TSSs. Both segments appear at the TSM input. In fact, since each TSS serves four TRACOs and this particular kind of ghosts can only appear in two contiguous TRACOs, each TSS forwards to the TSM two bits giving the relative address of the selected TRACO. The TRACO with address 00 of the TSSi is adjacent to the TRACO with address 11 of the TSSi-1. In case such adjacent segments are found, one is cancelled if it is a segment only observed in the outer SL: no duplication of the inner SL segments is possible in the TRACOs by construction.

In the hardware design the TSMS, TSMD0 and TSMD1 blocks are implemented as three distinct ICs. Each block has independent power lines. Three separate lines, from the chamber Controller, are used to provide enable signals (nPWRenSort, nPWRenD0 and nPWRenD1) for the power switches. When one IC is powered down, also all I/O lines to the chip are disconnected via bus isolation switches driven with the same enable signals. Three independent power fault signals are generated and reported to the Controller when an overcurrent condition is detected in the corresponding power net.

The TSM processing configuration can be changed from the Controller by acting directly on the power enable signals. The TSMS also receives the power enable state of the TSMD0 and of the TSMD1, then it can change its processing mode to select two tracks from the same TSMD, when the other TSMD is powered off. Similarly each TSMD receives the power enable state of both the TSMS and the other TSMD, and it can switch to the back-up processing mode when the TSMS is not powered. The system can still run in the extreme scenario of only one functioning TSMD block and its connections undamaged.

The processing mode is selected via configuration registers in all three devices. Registers are also used for the set-up of the sorting and the fakes rejection algorithms. Access to the configuration registers is possible in two independent ways: through a serial JTAG net for boundary scan and through the DT parallel access bus with an ad-hoc protocol, hereafter called Parallel Interface (PI).

Figure 5(a) shows the JTAG net through the three ICs: the net can be configured to run only through the chips that are powered on, using isolation switches controlled via the power enable lines.

Figure 5(b) shows how the PI bus is distributed through the TSM system; each IC has its own TSM address.

The PI commands from the chamber Controller are forwarded to the trigger boards through the TSMS. The TSMS gives access to only one trigger board in turn. In case of TSMS failure the trigger boards can still be configured via their individual JTAG nets. The PI utilises the same lines used for propagating the PRW data; the PRW bus is bi-directional.

The most important aspect is the choice of technology in developing the TSMS and TSMD ICs.

There is one TSM system in each DT chamber, that is a total of 250 TSMS and 500 TSMD ICs in the entire muon barrel detector. This is a too limited production volume for justifying the risk of developing two ASICs

The use of FPGAs has two advantages:

- The same type of device can be used for both the TSMS and the TSMD, because the chosen architecture requires a comparable number of pins for both ICs.
- It leaves flexibility for fine-tuning of the sorting and ghost rejection algorithms.

However standard FPGAs are disfavoured because of their low level of radiation tolerance, which can easily result in erasure and uncontrolled corruption of the programmed logic.

A solution is a new generation of FPGAs, the antifuse-FPGAs, also called pASICs (programmable ASICs). They are based on the silicon antifuse technology: silicon logic modules in a high density array are interconnected using 3 to 4 metal layers where metal-to-metal amorphous silicon interconnect elements (the antifuses) are embedded between the metal layers. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection. Once programmed, the chip configuration becomes permanent, making it effectively like an ASIC.

Tested for space applications [3], antifuse-FPGAs show good tolerance to high radiation doses of up to 10 to 50 Krads and high thresholds of 7 to 10 MeV·cm^2/mg for Single Event Upsets (SEU). Simulation studies [4] exist to estimate the radiation environment in CMS. When comparing the results in [3] with the simulation predictions, we expect no permanent damage in ten years of LHC running and a negligible yearly SEU rate for a pASIC chip operating in the TSM of a DT chamber. Both the Quicklogic QL3025 chips [5] and the Actel A54SX chips [6] can fit the TSM design constraints.

A prototype of the TSM system with pASICs has been built in which Quicklogic QL3025 and Actel A54SX chips are interchangeable. The prototype printed circuit board has a large size (a 6U VME board) for easy access to all critical nodes in the circuitry. A VME based system is used for providing the clock and control signals and for feeding the system with bit patterns mimicking real trigger data [7]. For any given input pattern, the TSM output is compared to the expected one. The TSM has been extensively tested with randomly generated patterns and in particular with ad-hoc sets of patterns devised to verify each specific aspect of functionality. The system internal timing has also been studied in details. The TSM prototype has successfully passed all tests with only minor modifications. Both QuickLogic and Actel chips have performed very closely to what expected from their electronic CAD simulations.

Although both succeeded, we prefer the Actel A54SX chip. It has shown a slightly better performance and Actel provides a better CAD environment, with VHDL entry for both design and simulation. It has also a lower cost.

The relevant characteristics of the A54SX32-3PQFP208 chip, which is used for implementing either the TSMS or the TSMD functionality, are summarised in table 1, as extracted from the Actel data book [6] and the Actel reliability reports [8]. The TSMS implementation uses 69% of the chip logic resources; the TSMD implementation uses 55% of the chip logic resources. These leave enough margin for adding more functionality if needed.

We have then studied the placement of components: due to the large number of signals processed in the TSM system, the small dimensions of the Server Board constitute an important design constraint. Therefore, we have built a full-functionality prototype board with final dimensions (98x206 mm^2). It has been possible to find a placement of the components that allows efficient routing and good high-frequency behaviour, using six signal layers and a standard 5 mils routing technology.

Thus, the Actel A54SX chips have been chosen for building the TSM. A final direct test of their radiation tolerance has been performed. Samples have been exposed in the 59 Mev proton beam of the Cyclotron Research Centre (CRC) at the Universite Catholique de Louvain (UCL), in Louvain-la-Neuve, Belgium, in October 2000. At this energy 10^{10} protons/cm^2 correspond to a dose of 1.4 krads. Four pASICs, each implementing a 450 bit register, refreshed and monitored at 1 MHz, have been irradiated up to 40 krads/chip (one of them up to 70 krads). There has been no failure and no latch-up. The Total Irradiation Dose (TID) result

is summarised in figure 6: no significant increase in current is observed for doses well above that of at most 1 krads expected for the CMS barrel muon chambers in 10 years of LHC operation.

We have observed one Single Event Upset. The event has been recorded and studied off-line. The 450 bit register dump shows that in the event about 1/3 of the FFs have changed state, with no obvious correlation in pattern. With the help of Actel CAD tools, we have inferred that most probably the internal clock distribution to the register cells has failed. Because of this, we quote a SEU cross-section measurement per chip instead of per bit, as it is usual in literature. With one observed event and a total fluence of $1.4\ 10^{12}$ protons/cm^2, we calculate a SEU cross-section upper limit (at 90% c. l.) of

$$\sigma_{SEU} < 2.9\ 10^{-12}\ \text{cm}^2 \qquad \text{per A54SX32 chip.}$$

According to the procedure established in [4], we can use this measurement for estimating the SEU rate in CMS. The flux of neutrons with energy exceeding 20 MeV is expected to be of at most 10^9 neutrons/cm^2 in the CMS muon barrel region [4] in 10 years of LHC running. Since the complete TSM system will consist of 750 A54SX32 chips, the expected SEU rate is

$$R_{SEU} < 2.2 \text{ events} \qquad \text{in 10 years of DT chambers data taking.}$$

Full functionality is recovered when refreshing the registers. The irradiation test results agree with the NASA results and have been obtained with a completely independent sample.

Acknowledgments

For the irradiation tests, we are grateful to the Cyclotron Research Centre (CRC) at the Univertite Catholique de Louvain, Louvain-la-Neuve, Belgium, in particular Dr. G.Berger, and to the CERN RD49/COTS collaboration, in particular Dr.F.Faccio. We recognize the important support provided by Dr.Eng.I.D'Antone and the I.N.F.N. Electronics Group in Bologna.

References

[1] CMS Collaboration**,** The Level-1 Trigger, Technical Design Report, CERN LHCC 2000-038, 15 December 2000, section 9

[2] G.M.Dallavalle, I.D'Antone, S.Marcellini, A.Montanari, F.Odorici and G.Torromeo, Proceeedings of the Fourth Workshop on Electronics for LHC Experiments, CERN LHCC 98-36 (1998) 294

[3] For a review of test reports see: NASA "programmable and quick-turn technologies for space flight applications, FPGAs and ASICs", http://rk.gsfc.nasa.gov/fpgas.htm

[4] M.Huhtinen and F.Faccio, Nucl. Instr. and Meth. A-150 (2000) 155; see also CMS Collaboration, The Muon Project, Technical Design Report, CERN/LHCC 97-32, CMS TDR 3, 15 December 1997; see also M.Huhtinen, CMS COTS Workshop, Nov.1999

[5] www.quicklogic.com/devices/pASIC/pasic3/Default.htm

[6] www.actel.com/user/html/databook99.html: see "SX Family FPGAs"

[7] G.M.Dallavalle, I.D'Antone, I.Lax, A.Montanari and F.Odorici, Proceeedings of the Fourth Workshop on Electronics for LHC Experiments, CERN LHCC 98-36 (1998) 291

[8] Actel reliability report 2000: www.actel.com/docs/devicedata/reliability.pdf

Actel A54SX32-3PQFP208
0.35 μm CMOS, 3.3 V core
48,000 System Gates, 2880 Logic Modules, 1080 Register Cells
4.6 ns Clock-to-Out, 0.1 ns Input Set-up, 0.25 ns Clock Skew
Plastic Quad Flat Pack, 208 pins
Failure Rate 29.2 FITs
Mean Time Between Failures $3.43 \cdot 10^{7}$ hours
Power Consumption <200mW

Table 1: Actel chip used in the TSM prototype. Failure rates are from [8]: the tests are performed with temperatures from -65^{o}C to $+150^{o}$C and relative humidity up to 85%.

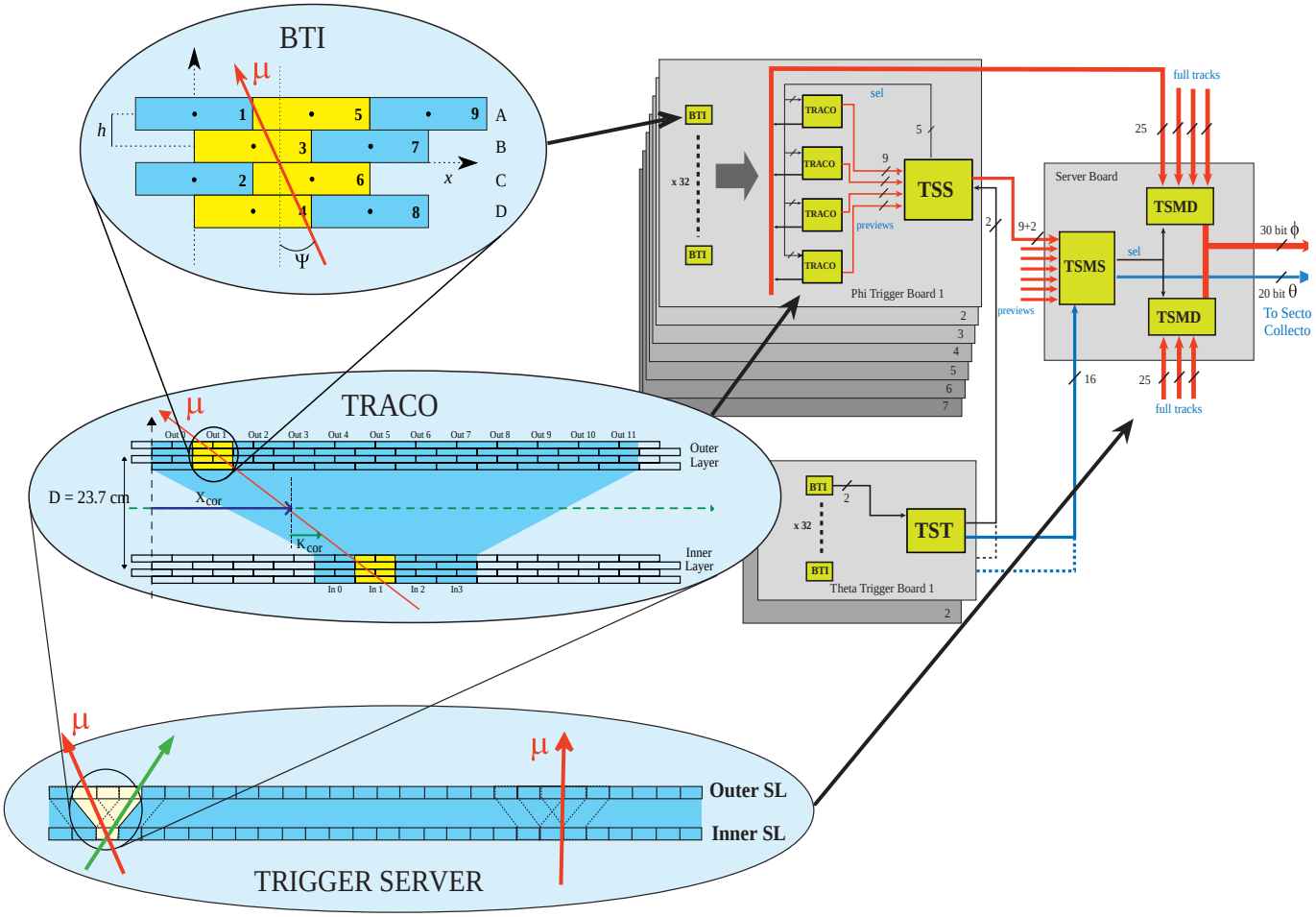

figure 1 CMS Drift Tubes on-chamber trigger electronics overview

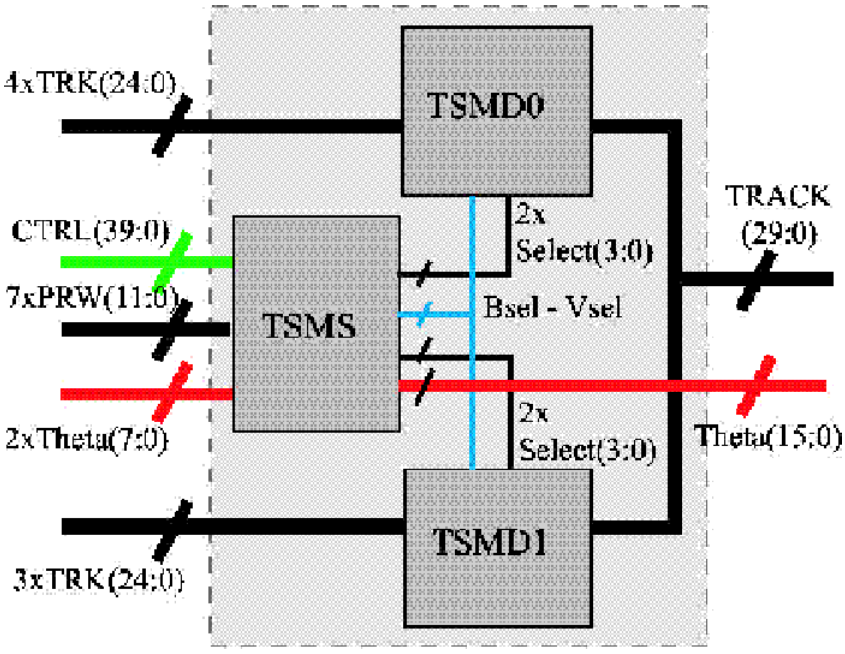

figure 2 Track Sorter Master I/O overview

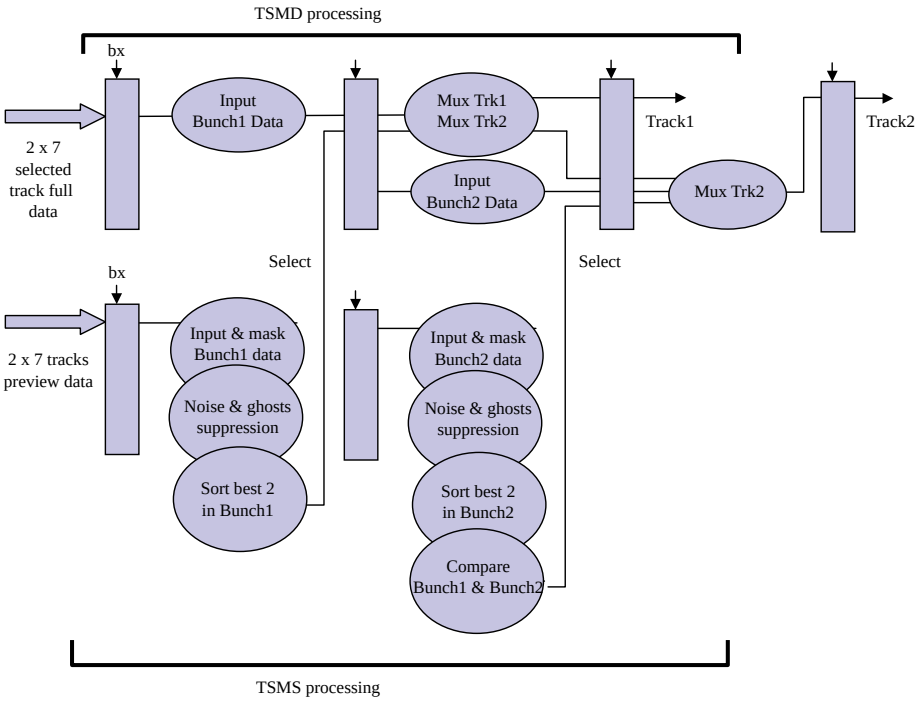

figure 3 TSM Default processing

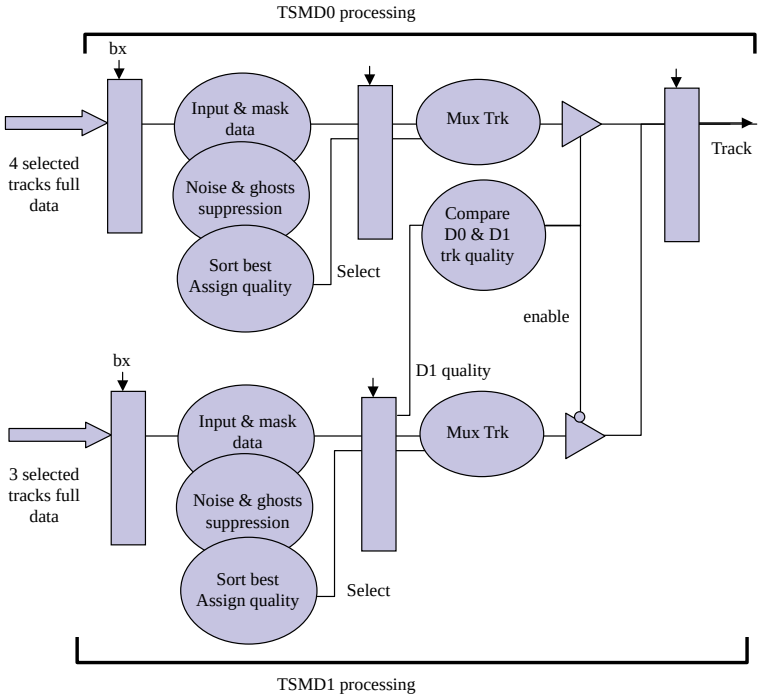

figure 4 TSM Back-up processing

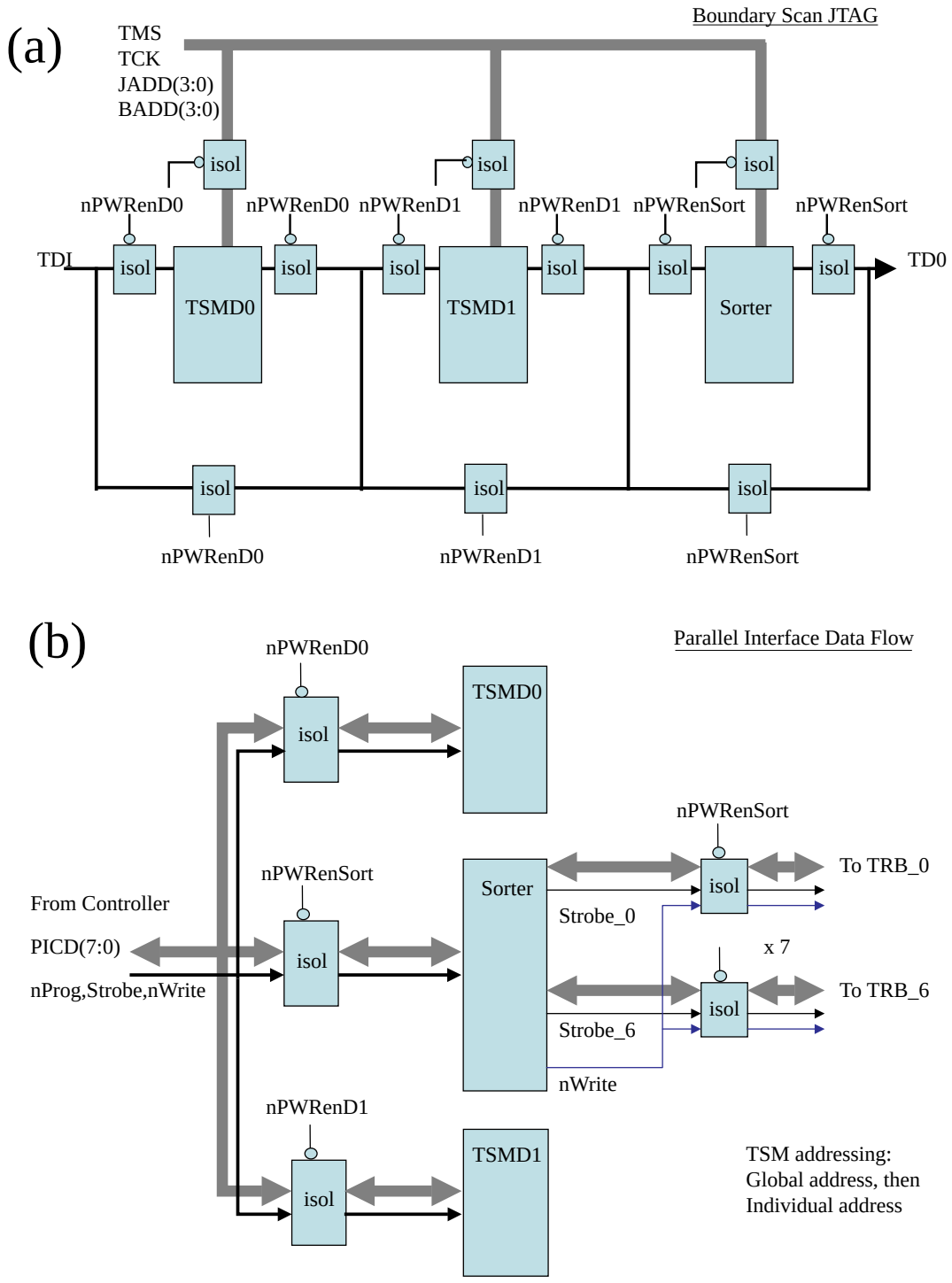

figure 5 (a) TSM JTAG net; (b) TSM Parallel Interface net

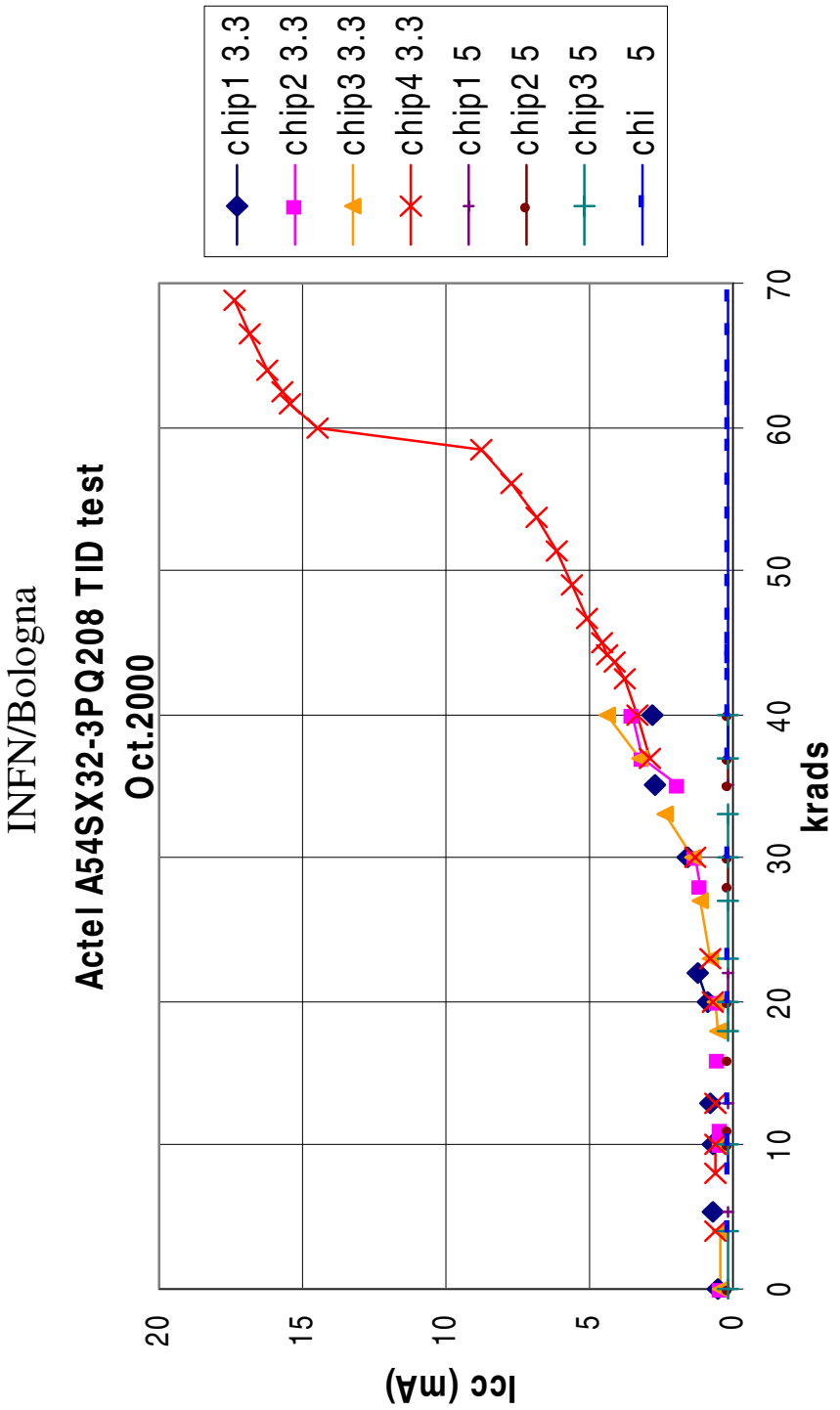

figure 6 Total Irradiation Dose test of the Actel antifuse-FPGAs for the Track-Sorter-Master of the CMS Muon Barrel Drift Tubes