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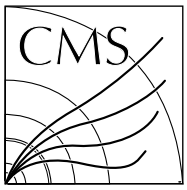

The Compact Muon Solenoid Experiment

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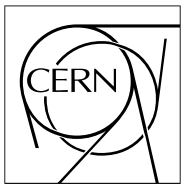

11 May 1999

Properties and performances of a frontend ASIC prototype for the readout of the CMS Barrel Muon Drift Tubes Chambers

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Abstract

A frontend Application Specific Integrated Circuit (ASIC) prototype developed for the read out of the CMS barrel muon drift tubes chambers has been produced in 100 samples. Several chips were used to read out one superlayer (224 drift tubes) of a full size prototype chamber. The properties of the chips and the performance of the chamber part equipped with the frontend prototype are presented.

1 Introduction

This frontend ASIC prototype has the task of producing a timing signal as accurate as possible when signals are picked up by chamber wires. To do that it has to compare, after suitable integration and amplification, the input current pulses with an external threshold. More than 100 prototype chips have been fabricated in two Multi Product Wafer (MPW) runs and then tested with a total yield better than 85% and very good performances. These chips have been mounted on Printed Circuit Boards (PCB). One full scale prototype of a CMS barrel muon chamber (MB96 [1]) has been equipped in the quadruplet characterised by $2\ m$ long wires (SL2) with 14 of these PCB (224 channels). The other two quadruplets (SL1,SL3) have been equipped with ASD8 [2] integrated circuits. This detector has been tested with a muon beam during August 1998 in operating conditions close to those expected in the CMS environment at LHC. Beam test as well as some bench test results will be presented here.

2 Circuit description

The prototype chip has been fabricated using 0.8 micron BiCMOS technology by AMS Austria; four complete channels find place in a die area of $2.5 \times 2.3\ mm^2$ and use $\sim\ 400$ bipolar transistor arranged as in the block diagram of Fig. 1. The input stage of each channel is a charge preamplifier with Gain Band Width (GBW) in excess of 1GHz and a feedback time constant of $16\ ns$ or $32\ ns$ depending on MPW run. The shaper is a low gain, high frequency integrator inserted in the feedback loop of an Operational Transconductance Amplifier (OTA) thus implementing a time invariant baseline restorer that forces the output level of this stage to the voltage applied to V_{REF} pin (common to all channels). The output of the shaper is directly connected to one input of a latched discriminator while the other input (the threshold voltage) is connected to V_{TH} pin, again common to all channels. The discriminator triggers a one shot that in turn activates the latch so helping in avoiding oscillations with slow or weak signals and producing an output pulse whose width (externally adjustable) is independent of input amplitude. The output of the one shot is buffered by an LVDS compatible cable driver and then made available at the output pins.

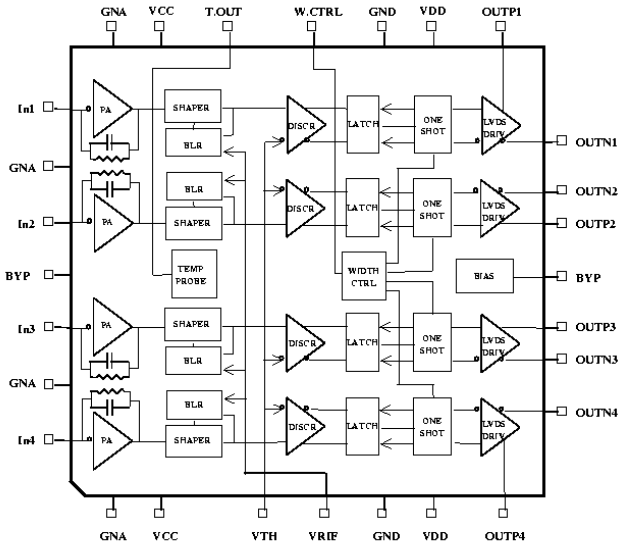

Figure 1: Block diagram of the MAD chip.

Tha ASIC requires two supplies ($V_{CC} = +5\ V$ for the analog chain and $V_{DD} = +2.5\ V$ for the output section) and one reference voltage ($V_{REF} = +1.5\ V$). The total power consumption is $25\ mW/channel$ in average. Input noise is about 1500 electrons @ 0 detector capacitance while maximum input charge before saturation is about $800\ fC$ and threshold range is $0 - 500\ fC$ with nonlinearity better than 1%. The propagation delay from charge input to cable out is about $3.5\ ns$ and time walk is about $3.5\ ns$ (@ $C_D = 0$) for input signals varying in the range $3\ fC\ -\ 1\ pC$. For a more detailed description refer to [4].

3 Test of the frontend boards

The relation between threshold voltage and input charge has been measured with δ-like current pulses on a sample of 74 chips (296 channels) [4]. Fig. 2 shows a linear relation for input charge pulses from 2 to 50 fC. The slope is $3.35\ mV/fC$. Fig. 3 and 4 show the threshold distributions for 3 and 9 fC input charge. The r.m.s. in this threshold range is about equal to $0.50\ mV$ ($0.15\ fC$). The r.m.s. is the effect of gain inaccuracy and of discriminator offsets (+ baseline restorer). The latter effect accounts for $0.44\ mV$ ($0.13\ fC$) r.m.s. inaccuracy and it was calculated by extrapolating for each channel the threshold characteristic to $0\ mV$ [4]. The relation between threshold voltage

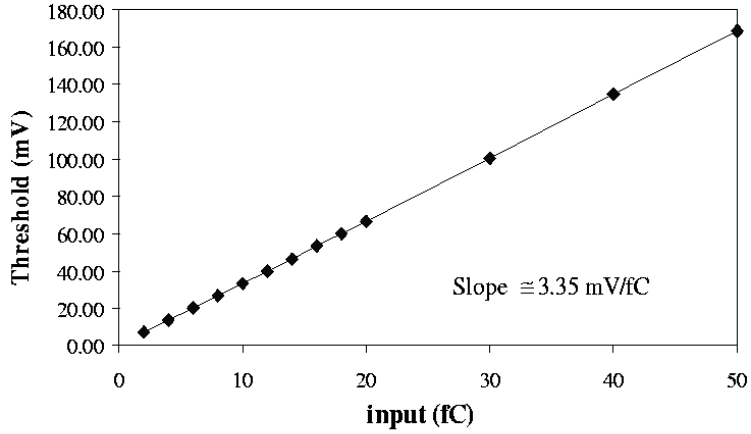

Figure 2: Threshold as a function of input charge for the MAD integrated circuits.

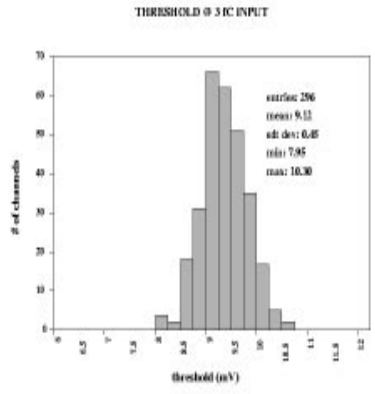

Figure 3: Threshold distribution for 3 fC input charge.

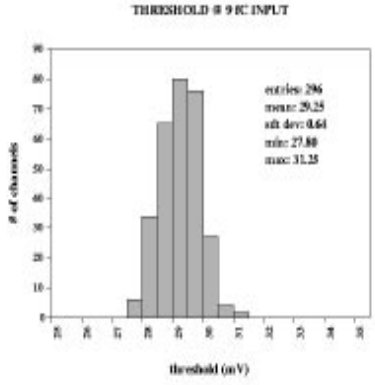

Figure 4: Threshold distribution for 9 fC input charge.

and charge has been measured for the ASD8 integrated circuits on a sample of 2 chips (16 channels). Fig. 5 shows the slope in the range between 2 and 6 fC after offset correction on a chip by chip basis. The error bars are the r.m.s. of the threshold distributions. For an input charge of $6\ fC$ the standard deviation is about $50\ mV$ ($0.5\ fC$). The relation is linear only in a limited range of input charge. The slope is about $-100\ mV/fC$ up to $6\ fC$.

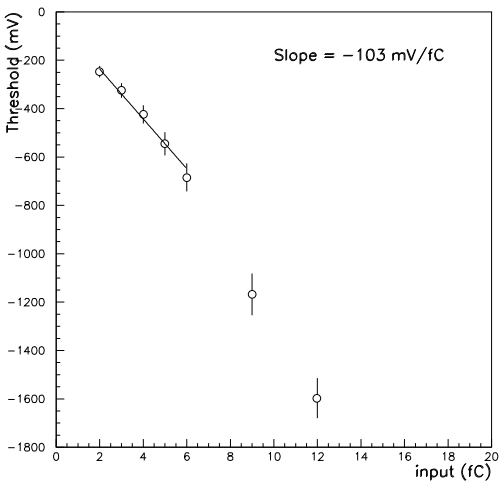

Figure 5: Threshold as a function of input charge for the ASD8 integrated circuits.

4 Results from a prototype chamber

4.1 Noise vs threshold

The noise rate has been studied as a function of threshold level on the 224 cells of the SL2 quadruplet equipped with the MAD chips. This test has been done in LNL (INFN National Laboratory in Legnaro) with two high voltage sets:

$$V_{cathode}/V_{strip}/V_{wire} = -1800/1800/3600\,V \qquad V_{cathode}/V_{strip}/V_{wire} = -1800/1800/3700\,V$$

These voltages at the sea level ($p = 1\ Atm$) are about equivalent to the following voltages at CERN ($p = 0.95\ Atm$)

$$V_{cathode}/V_{strip}/V_{wire} = -1700/1700/3400\,V \qquad V_{cathode}/V_{strip}/V_{wire} = -1700/1700/3500\,V$$

These values were choosen being the first outset of the efficiency plateau (3^{th} point in Fig. 12), the second being close to the end of the same plateau (5^{th} point in Fig. 12). The result is described in Fig. 6. The noise rate has to be compared to the physics rate at LHC of about $1\ kHz/m$ (in one cell).

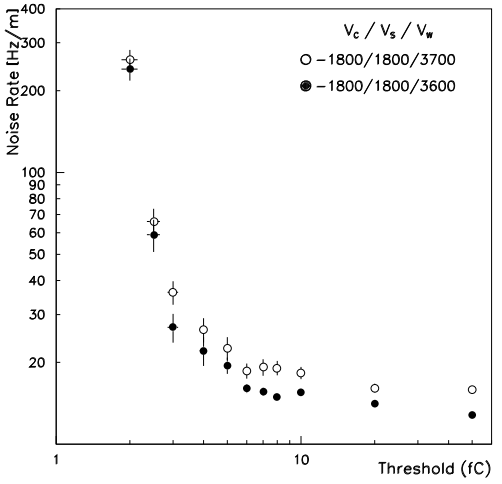

Figure 6: The mean noise rate for the cells in the SL2 quadruplet as a function of threshold level.

4.2 Test-beam setup

The MB96 chamber has been exposed to a muon beam with about $100\ GeV$ energy in the Gamma Irradiation Facility area (Fig. 7) at the CERN-SpS during August 1998. The 15 Curie Cesium source produces a high flux of $0.66\ MeV$ photons, simulating the LHC environment. The main purpose of this test was to study efficiency, resolution and wires current as a function of radiation level [6]. At the same time we took advantage of the muon beam to study the behaviour of the frontend boards.

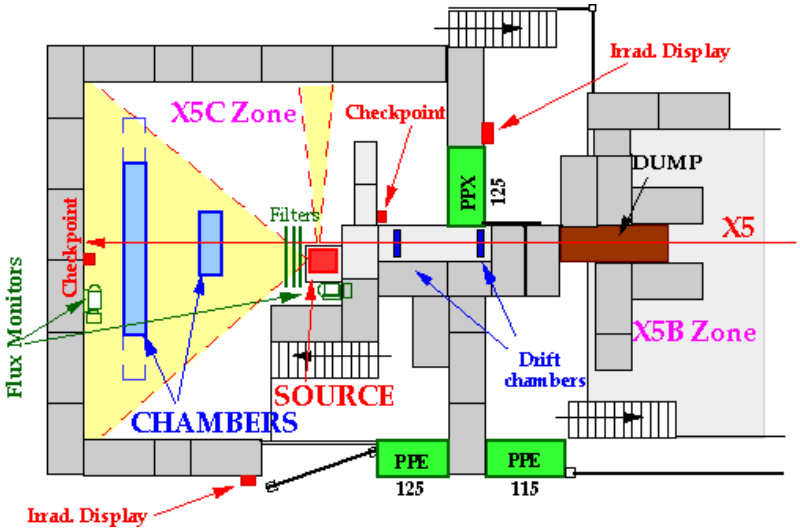

Figure 7: The Gamma Irradiation Facility (X5 beam) at CERN

4.3 The threshold scan for different integration times

The signal shape was already studied with a current preamplifier with cosmic rays [3]. The rising time of the full signal is related to the number of clusters arriving to the wire. The signal for a single cluster (due to the first electron in the primary ionization) has a rise time of about $10\ ns$. The integration time of the preamplifier has to be of the order of the rising time of the signals in the cell. Two preamplifiers, with $16\ ns$ and $32\ ns$ integration time, were compared in the test beam. The degradation along the wire is expected to be important in the MB96 prototype due to the high resistivity of stainless steel wire used ($\sim\ 500\ \Omega/m$). Four threshold scans were performed at the two extremes of the wires and for the two different preamplifiers. Fig. 8 and 9 show the resolution and the efficiency as a function of threshold for the four considered cases. The standard H.V. setting was:

$$V_{cathode} = -1700\ V \qquad V_{strip} = 1700\ V \qquad V_{wire} = 3400\ V$$

The resolution does not depend on the integration time. The difference between the H.V. side (white symbols) and the F.E. side (black symbols) is due to the spread of signals when propagating along wires. Varying the threshold from $10\ fC$ to $3\ fC$ the resolution drops from $4.6\ ns$ to $3.4\ ns$ in the F.E. side and from $5.5\ ns$ to $4.0\ ns$ in the H.V. side. The differences in efficiency are smaller than 1% for thresholds lower than $10\ fC$.

4.4 Position scan

To test the MAD chip uniformity a scan across the different cells of SL2 was performed with the standard H.V. setting. Fig. 10 and 11 show the efficiency and resolution as a function of cell and column number. One column is defined as the four aligned half cells on the four layers. This superlayer (SL2) equipped with 56 MAD chips results to be uniform in efficiency and resolution. Holes in the efficiency distribution correspond to cells without wire.

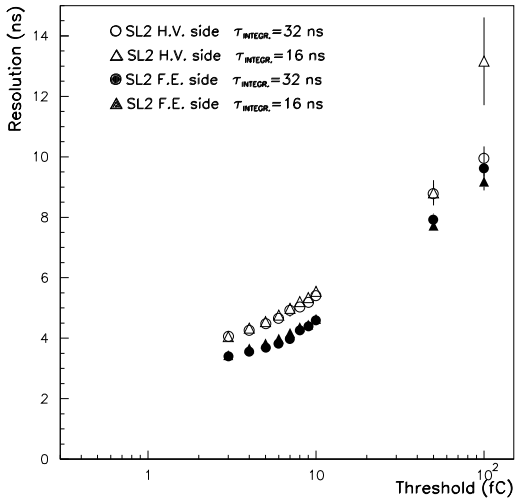

Figure 8: Resolution as a function of threshold for the MAD chips with $32\ ns$ and $16\ ns$ of integration time

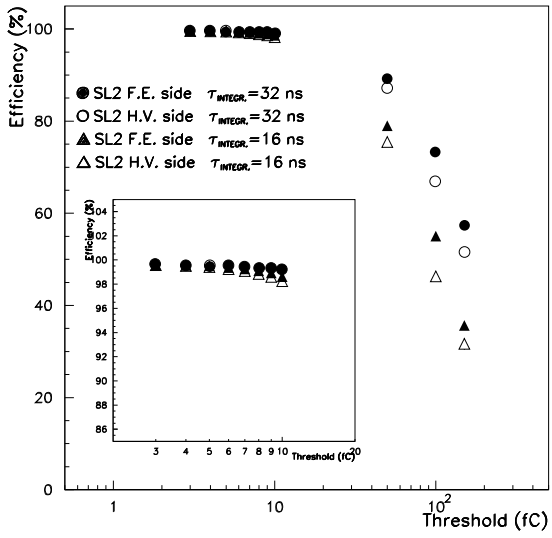

Figure 9: Efficiency as a function of threshold for the MAD chips with $32\ ns$ and $16\ ns$ of integration time

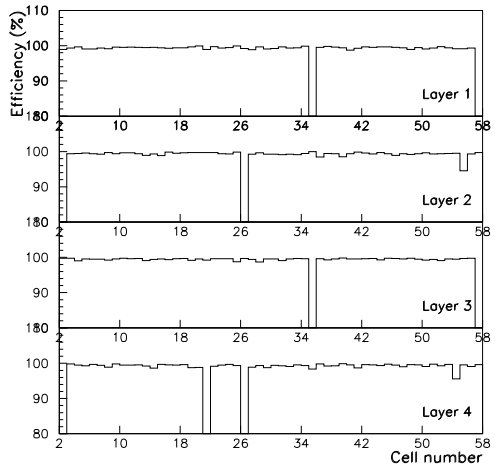

Figure 10: Efficiency as a function of cell number for the four layers of SL2.

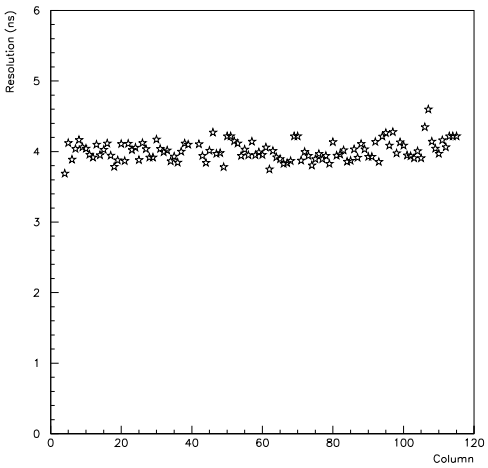

Figure 11: Resolution as a function of column number for all the cells in SL2.

4.5 Efficiency and resolution vs Veff

Efficiency and resolution differences between the front end and the high voltage side of the wire are related to the H.V. setting as like as the threshold level. Efficiency and resolution are given in Fig. 12 and 13 as a function of the effective voltage V_{eff}, which is a quantity proportional to the electric field on wire surface. V_{eff} can be parametrised as a function of voltage settings (in Volts):

$$V_{eff} = (V_w - V_s) + \alpha V_s - \beta V_c \tag{1}$$

$$\alpha = 0.126 \pm 0.002 \qquad \beta = 0.0184 \pm 0.0004 \tag{2}$$

The parameters where determined experimentally through an extensive study of the gas amplification with a radioactive source [5]. There's no difference in efficiency between the F.E. and the H.V. side of the wire. The difference in resolution between the two sides depends on V_{eff} and is about $0.8\ ns$ at the standard H.V. setting (Fig. 13, $V_{eff} = 1945\ V$).

4.6 Test pulse

The T0 is defined for each cell as the starting point of its drift time box. We computed the T0 cell by cell from the time box derivative as $\mu - 2\sigma$ (Fig. 14 and 15). Using identical frontend cables and receivers it does not avoid to have T0 differencies between cells. One useful method for a fast T0 correction is to send at the same time a test pulse to all the channels. Fig. 16 shows for 24 different cells and 4 different layers equipped with the same electronics the T0 distribution before and after the time correction from the test pulse run. Fig. 17 shows the T0 as a function of threshold for the MAD chips with two different integration times and for two different positions along the wire.

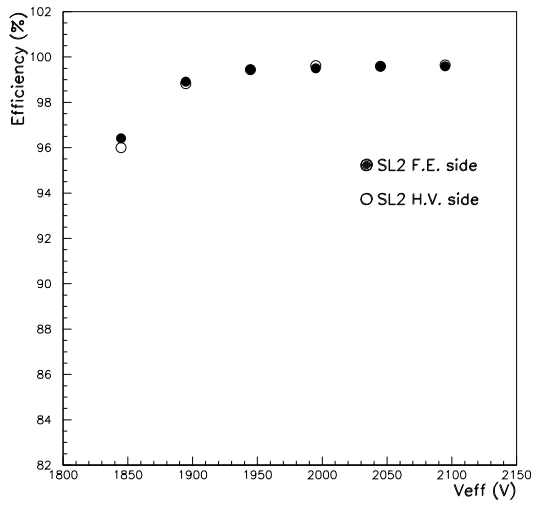

Figure 12: Efficiency as a function of effective voltage V_{eff}.

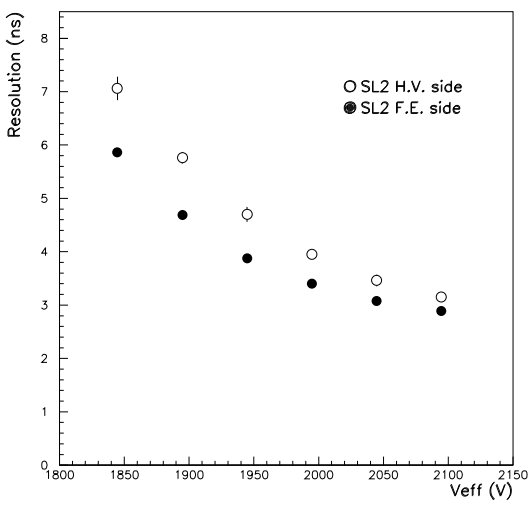

Figure 13: Resolution as a function of effective voltage V_{eff}.

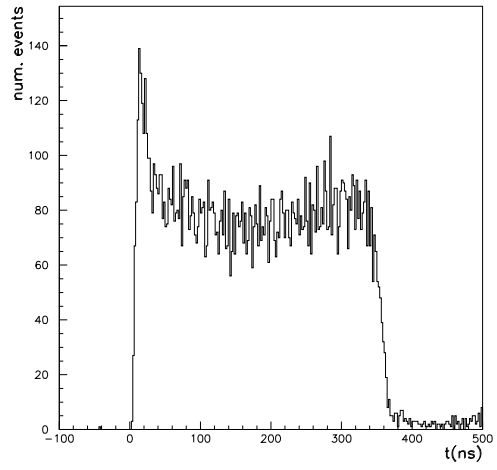

Figure 14: Time box distribution for hits in one cell.

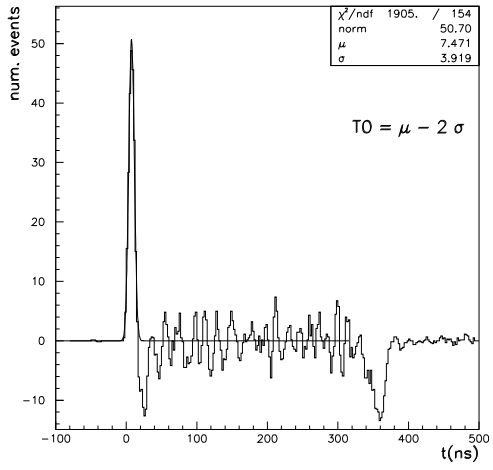

Figure 15: Time box derivative.

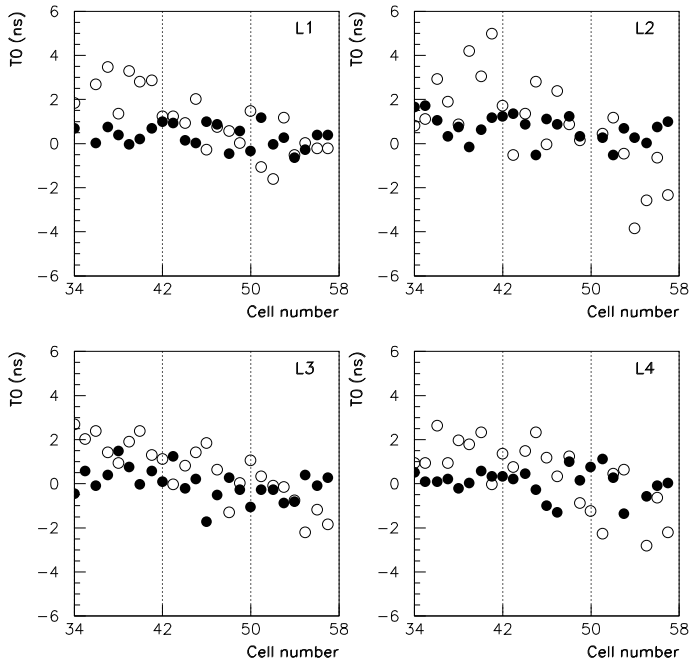

Figure 16: T0 from time box derivative without (open circles) and with (full circles) correction for the single channel time from the test pulse run.

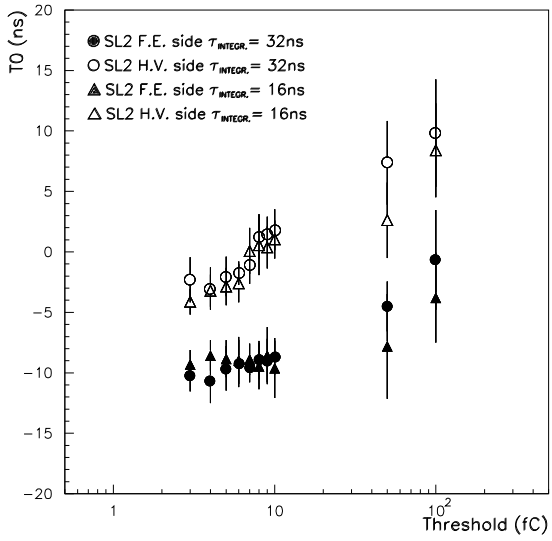

Figure 17: T0 as a function of threshold for the MAD chips with integration time of $32\ ns$ and $16\ ns$.

5 Conclusions

The relation between the threshold voltage and the threshold charge has been measured for the MAD and the ASD8 integrated circuits. The results are: $Slope_{MAD} = 3.35\ mV/fC$, $Slope_{ASD8}(2 \mapsto 6\ fC) = -100\ mV/fC$.

For the two MAD preamplifiers with $16\ ns$ and $32\ ns$ of integration time the resolution is the same for every threshold, the differences in efficiency are smaller than 1% for thresholds lower than $10\ fC$.

One superlayer with 224 cells equipped with MAD chips shows a good uniformity in efficiency and resolution.

There's no difference in efficiency between the front end and the high voltage side of the wire. The difference in resolution between the two sides is about $0.8\ ns$ at the standard H.V. setting.

Testpulse runs was found to be useful to correct T0 differencies between different channels.

References

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[5] E. Conti, *private communication.*

[6] E. Torassa, *CMS WEEK, Lyon 15 September 1998, presentation at the BMU meeting.*