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The Compact Muon Solenoid Experiment

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Six Layer P1 Cathode Strip Chamber Prototype
(Construction and first results)

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Abstract

A full scale six layer Trapezoidal Cathode Strip Chamber Prototype of 0.8m x 1.2m x 3.3m was constructed and tested at Fermilab. The chamber construction and the first results on the chamber characteristics are presented in this paper.

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1 Introduction

The main goal in constructing this full scale prototype was to test new technologies of construction in developing a reliable and cost efficient design for Cathode Strip Chambers which will provide the required performance for the CMS Endcap Muon detector.

2. Chamber construction

A six layer P1 prototype (Fig.1) was constructed from commercially made PLASCORE panels with polycarbonate core and 1/16" FR-4 copper clad skins. The radial cathode strips (64 strips per layer) were milled directly on the panel with a 45 degree CNC milling cutter. Strips width varied from 15.8mm to 9.7mm from the outer to inner ends. Spacing between strips was 0.5mm. The strips stagger by a half width in alternate gaps. The strips were staggered ± 1/4 strip width with respect to the centerline of the chamber. Anode panel artwork was also milled directly on the panel with a 45 degree CNC milling cutter. Precision ground wire support bars with etched Au plated artwork were glued to the machined anode panels. The wires were wound directly on the anode panels (using precision combs on edges) to preserve panel flatness, save labor, and wire wastage. The anode planes have 50 μm diameter Au plated tungsten wires (SYLVANIA). The wire spacing is 3.17mm, and the wire tension is 250gm. The anode wire planes are split into 5 independent HV segments (Fig.2) to test the feasibility of HV segmentation within a single wire plane. In this case, two adjacent wires (one from each group) are removed and isolated FR-4 guard strips were installed at the gaps. Also, instead of thick guard wires on the ends of the wire planes, FR-4 guard strips were used. The FR-4 gap bars which fix the cathode - cathode gap were ground to a specified thickness (9.53 ± 0.05mm). These bars were bonded to the cathode panels with 3M double scotch tape and the edges glued and sealed by epoxy. Four buttons were installed along the centerline to maintain the gap in the central chamber area. To prevent panel gas pressure bulging, the panels are joined by tierods through the buttons. An external RTV gas seal (at one panel face of each gap) was made on the outside edge of the gap bars. After the chamber was assembled, the measured strip capacitance to ground (Fig.3) was about 270 pF, and interstrip capacitance (Fig.4) was about of 160 pF. Some periodical structure in the distribution reflects the connector artwork lead length variation. Also we have measured the wire group capacitance to ground (Fig.5). This capacitance varied from 100 pF to 140 pF in conformity with wire length variation. We can see from this plot that two wire group were interconnected and one wire group was disconnected. This measurement will be done before any future chamber is assembled to have quality assurance control on continuity of wire groups.

3 Experimental set-up

Fig.6 shows the experimental set-up being used for testing the P1 prototype with cosmic rays. The 36cm thickness granite table serves to reject soft muons. The signals from the four scintillators were put in coincidence and serve as the trigger. The coincidence count rate of cosmic rays is about 2 muons/sec in an angle range about ±10 degree. The anode and cathode electronics was designed and built at Ohio State University. A new DAQ developed by Purdue University is being used for data taking. Four channel amplifier/shaper boards with a fast discriminator are connected to the anode wires. The shaper has a peaking time of about 30 nsec. The nominal gain of the anode channel is 3mV/fC. The amplifier has two different types of discriminators: a zero crossing and a leading edge. The analog output from the amplifier was used for amplitude measurements and a digital ECL pair timing pulse output was used for timing measurements. The cathode strip read-out electronics boards consist of a 16-channel Gasplex amplifier/shaper chip and a CAMAC Gasplex/ADC controller. The sample and hold time on Gasplex board is set to about 400 nsec in order to assure maximum linearity. The ADC has 10 bits with a full scale of 1V, which corresponds to a charge of 200fC. The nominal gain of the system is 5mV/fC. The chamber is equipped completely with cathode electronics (384 channels) and partially with anode electronics (144 channels of 384 channels). An event display (Fig.7) shows the typical distribution of the induced charge on the cathode strips and the anode wire group position for a muon hitting the 6 layer P1 chamber. All electronics is mounted on the face of the chamber and connected to the wire groups or strips with short shielded cables. The internal ground is filtered and the chamber is shielded by a dirty ground.

4. Measurements and results

The first measurements of efficiency, gas gain, and time resolution for leading edge discriminators at 20 fC threshold were performed for a wide range of voltages. All measurements were carried out with gas mixture: 50% CO_2 + 30% Ar + 20% CF_4. The P1 prototype was tested from 3.7kV to 4.5kV. Currently P1 holds 4.6kV without any significant leakage current ($I<1\mu A$). Fig. 8 shows the typical chamber wire signals from a digital scope for three chamber layers in coincidence with a trigger signal from the scintillators.

The dependence of the cathode signal amplitude from the Gasplex electronics on high voltage was measured for one local chamber area (0.2m x 0.5m) and the results are shown in Fig. 9. It can be seen that all six layers have roughly the same gas gain value; well within the 50% gain variation tolerance allowed.

The time characteristics of the P1 six layer prototype for anode leading edge discriminators was studied. Fig.10 shows the dependence of time resolution, in terms of RMS, on high voltage for the single layers. We observed that the time resolution varied from 17nsec to about 8nsec over the high voltage range.

We measured the single layer efficiency of the CSC for all planes and the results are shown in Fig. 11. The efficiency plateau reaches nearly 100% between 4.1kV and 4.5kV.

For track selection criteria we have taken events with not more than 2 TDC hits on a plane and a minimum 4 planes with hits (4 or more hit track). Time resolution for the earliest time (first out of six hits) and the second out of six hits is shown in Fig. 12. The time resolution for the second out of six hits is a little better than the first out of six hits and reaches about 5 nsec at the lowest operational point (4. lkV). The beam crossing interval at the LHC will be approximately 25 nsec, so it is important to define the time resolution of the muon chamber for 20 nsec or 25nsec gating windows. Fig. 13 shows the fraction of events for a single plane and for the first out of six anode signals in 20nsec and 25 nsec software windows. The single layer "gate efficiency" varied from 60% to 90% depending on the high voltage. Chamber time efficiency for the first signal out of six varied from 95% to 99% for the chamber on the efficiency plateau (4.1kV - 4.5kV).

5. Conclusion

The full scale six layer P1 prototype has been constructed and the first results on chamber performance have been obtained. The technology of P1 reflects an evolution developed through the T0, T1A, T1B, and P1A prototypes. This includes inexpensive simply cut-ground-drilled gap frames with external RTV gas sealing, high voltage segmentation in each plane (5 segments), simple guard strips, gap spacing buttons, antibulging tierods through the buttons, gold plated etched wire support bars, no clean solder, and epoxy/RTV dispensing.

There were no problems observed in the chamber assembly or operation. High voltage training was achieved in a few hours.

6. Acknowledgments

We would like to especially thank the Fermilab Physics Department for their support of this effort. We are also grateful to all the members of the Endcap Muon group for their numerous discussion and suggestions.

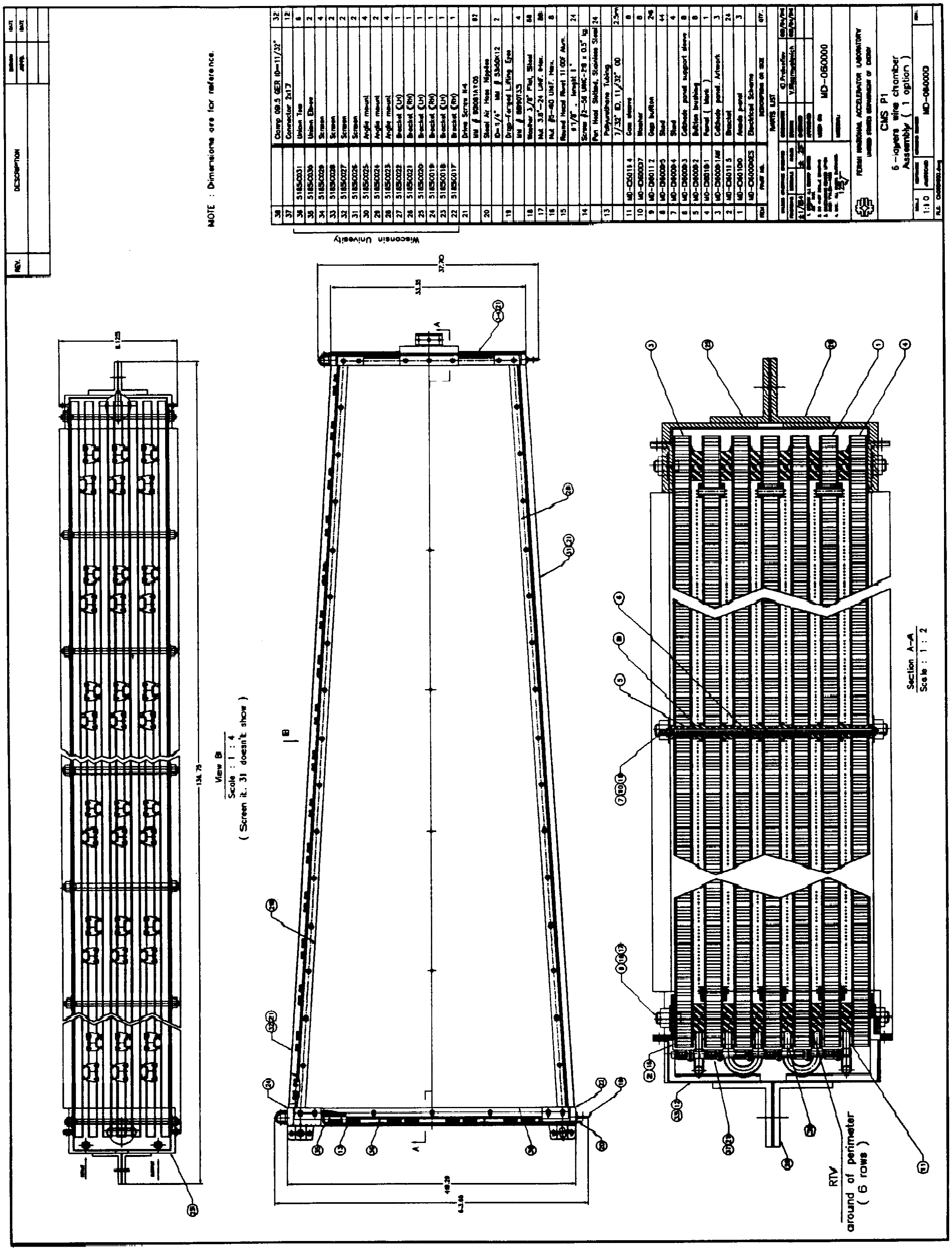


Fig. 1. Construction of 6 layer Cathode Strip Chamber.

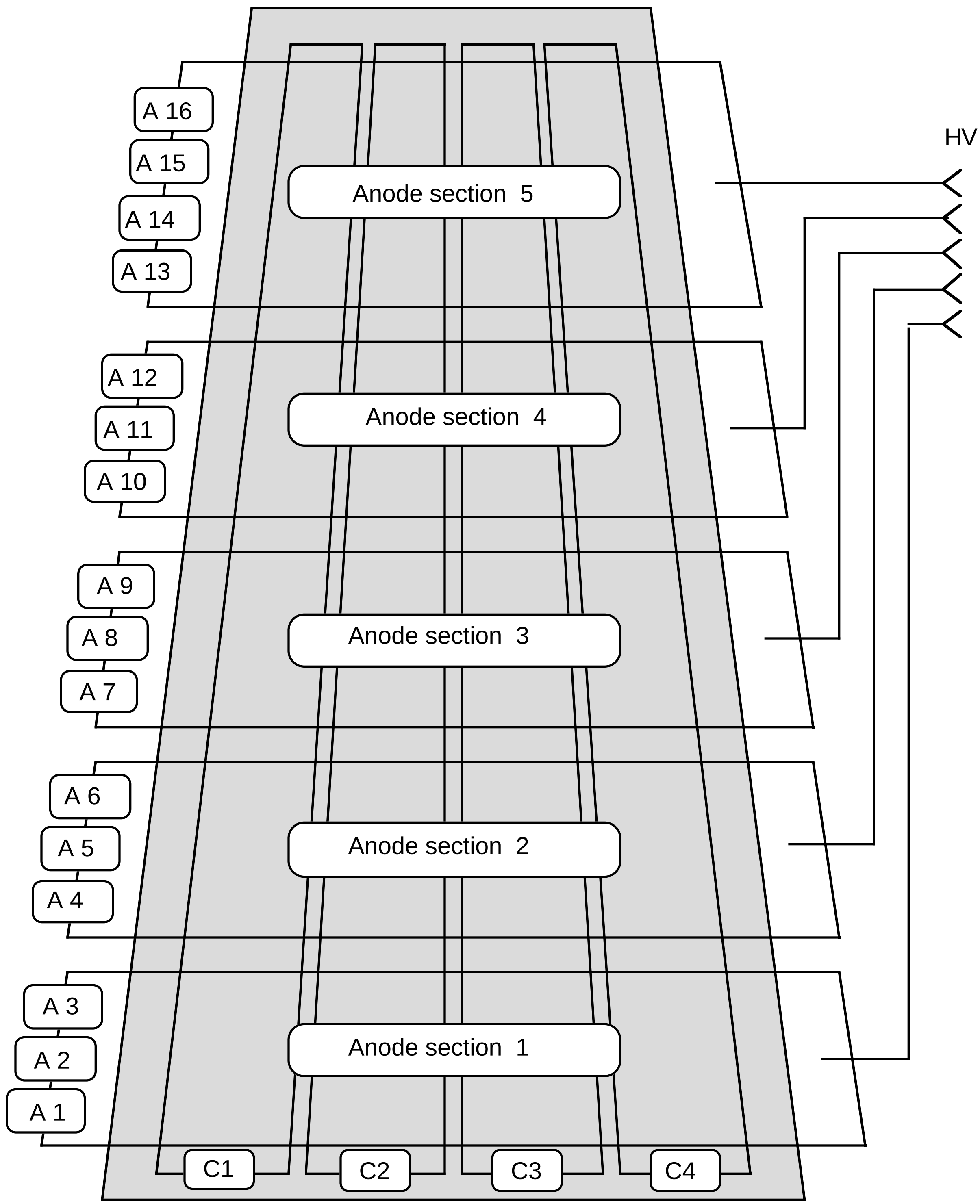


Fig. 2. High voltage segmentation of the CSC.

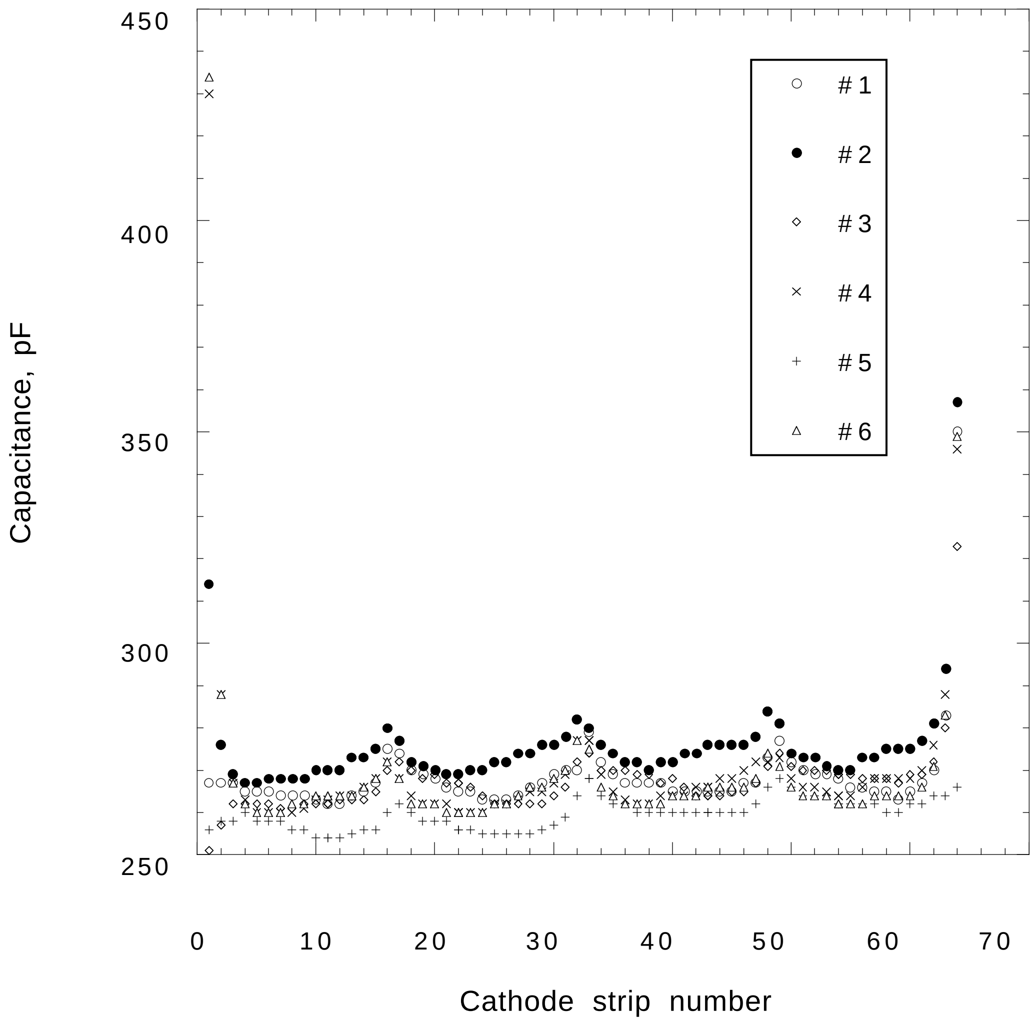


Fig. 3. Strip to ground capacitance for individual layers.

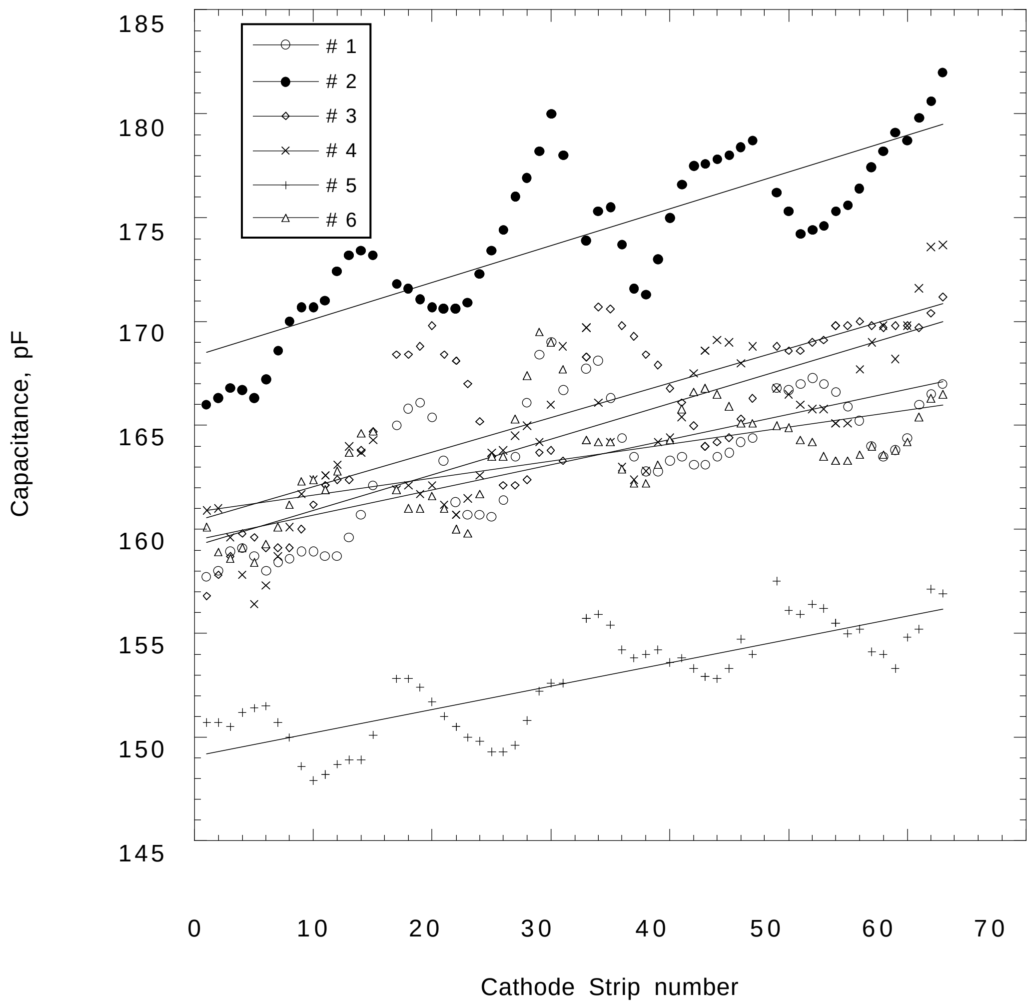


Fig. 4. Interstrip capacitance distribution.

Periodic structure is defined artwork traces going to connectors, slope is due to wearing out milling bits.

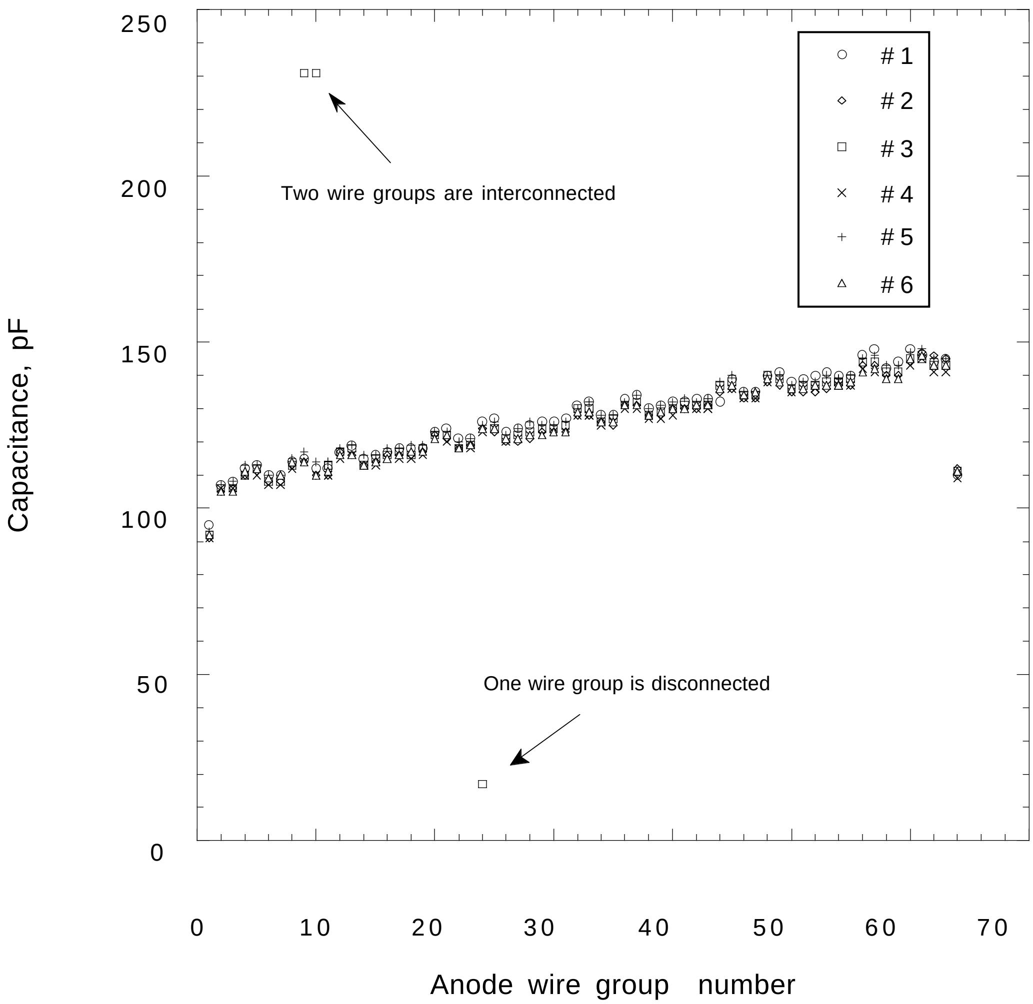


Fig. 5. Anode wire group capacitance to ground.

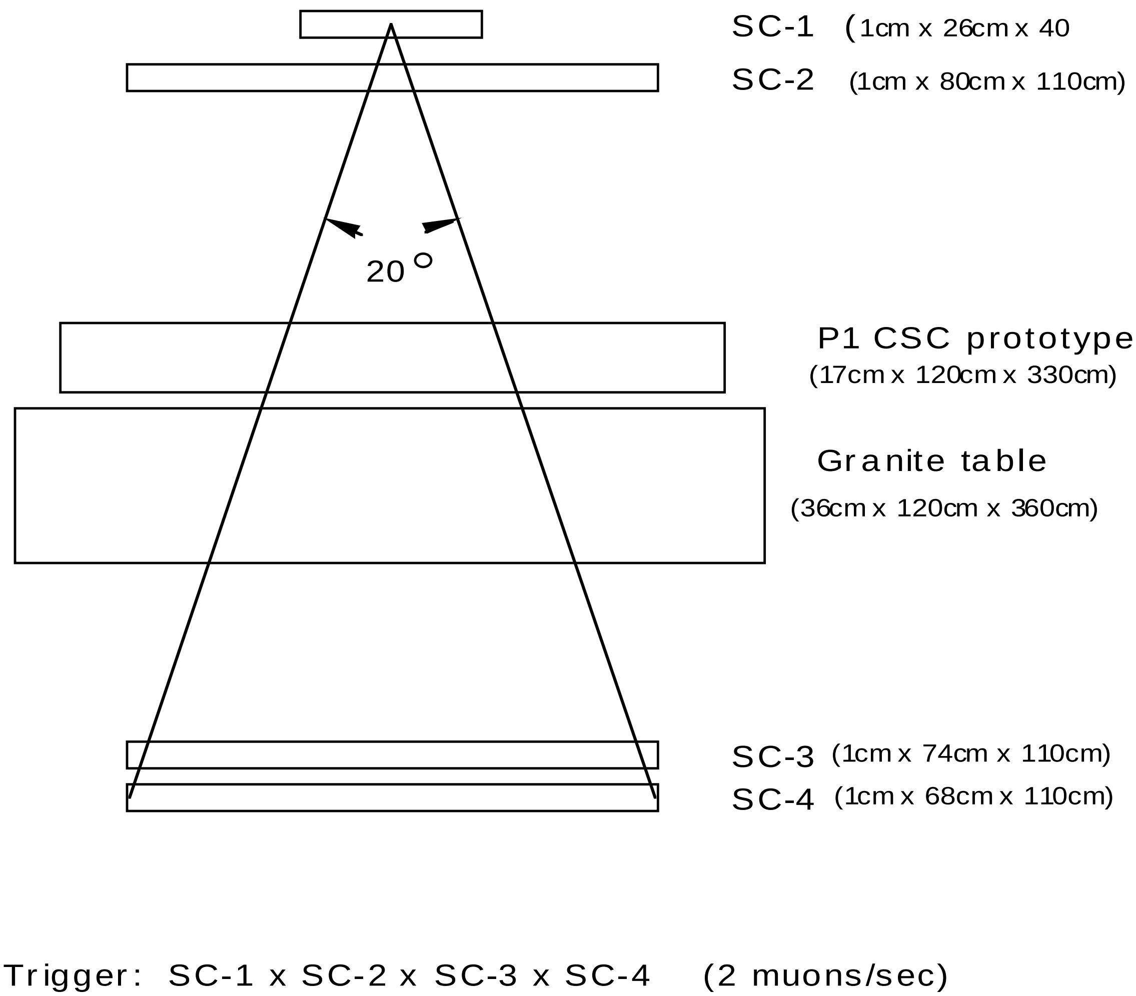
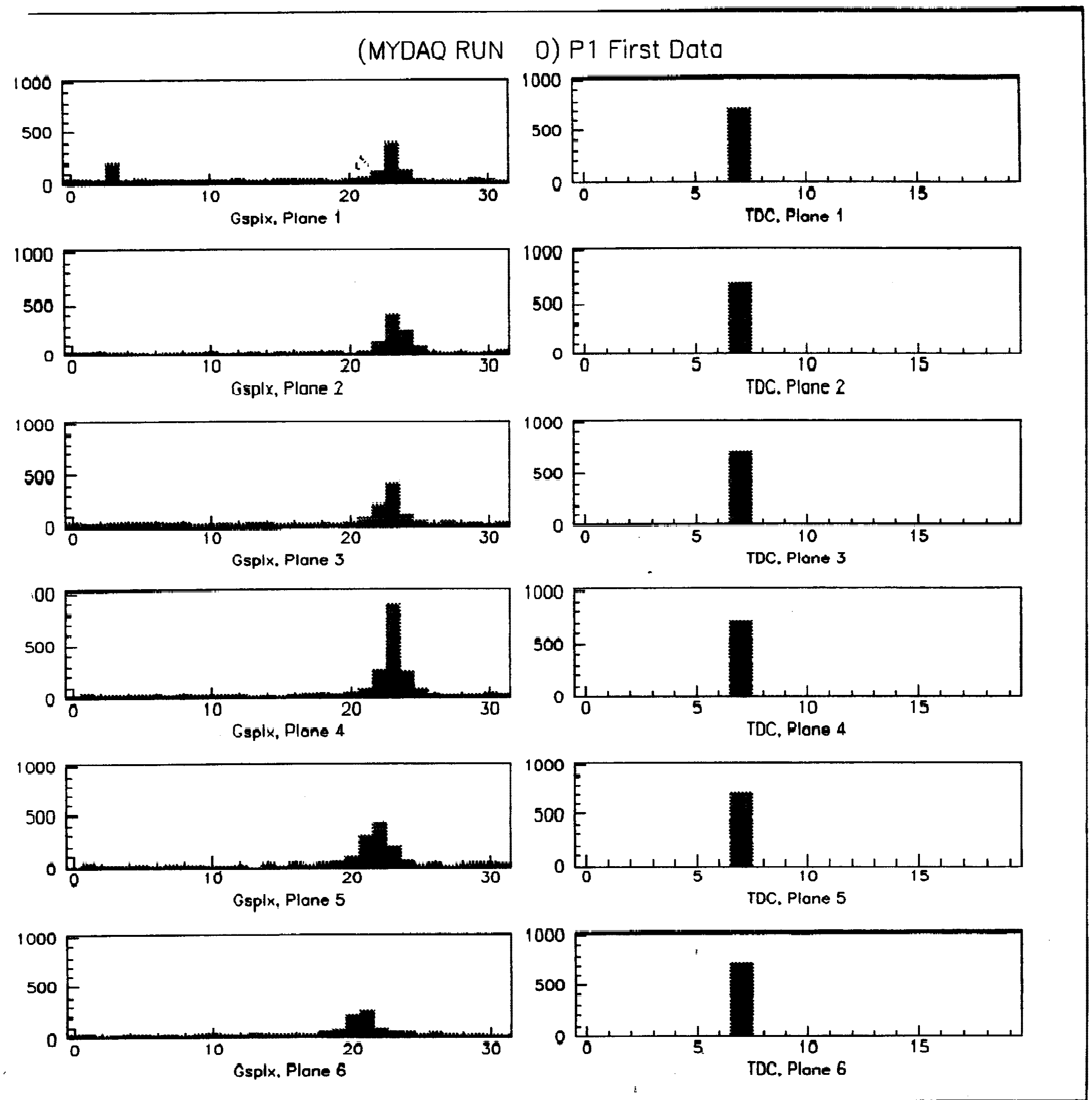


Fig. 6. Cosmic test stand scheme.


(MYDAQ RUN 0) P1 First Data
Gsplx, Plane 1
TDC, Plane 1
Gsplx, Plane 2
TDC, Plane 2
Gsplx, Plane 3
TDC, Plane 3
Gsplx, Plane 4
TDC, Plane 4
Gsplx, Plane 5
TDC, Plane 5
Gsplx, Plane 6
TDC, Plane 6