The Compact Muon Solenoid Experiment

CMS Note

October 20, 1998

Readout of a Micro Strip Gas Chamber Prototype with the APV6 Front-end Chip

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Abstract

It is foreseen that all the microstrips of the Silicon and MSGC tracker in CMS will be read out by the same front-end electronics. The APV6, a 128 channel pipeline chip developed and optimized for silicon detectors, has been used for the first time to instrument one prototype MSGC built and operated according to CMS specifications. The low noise amplifier is identical to the one included in the version of the chip optimized for MSGC which has recently been prototyped. In their low luminosity operation mode (*peak mode*) the two chips behave in identical way. Some results are presented of the performance of the system stimulated by a Sr^{90} source and operated in peak mode.

1   Introduction

The CMS central tracker contains 5.6×10^6 channels implemented as silicon microstrips and 6.4×10^6 channels in gas microstrip (MSGC) technology. Analogue readout without data sparsification at the front-end has been chosen in order to achieve robustness of the system against common mode noise effects, to simplify debugging and ultimately to improve the overall performance for physics. Analogue data will be transmitted optically to the external digitizing stages. Detector and electronics control and monitoring will be implemented digitally and will make use of similar optical technologies.

Because of similarities in detector capacitance and signal sizes it is foreseen to employ the same front-end electronics to readout both kind of detectors. Some inevitable differences, however, dictate modifications.

The APV series is the result of the efforts of the RD20 collaboration which have culminated in the APV6 [1], the final prototype of the readout chip optimised for silicon microstrips in CMS. It is a radiation hard CMOS circuit which consists of 128 amplifier, pipeline and signal processing stage channels multiplexed onto a single analogue output line. The APVM is the version of the chip optimised for the CMS gas detectors. It has recently been prototyped [2] and is currently under test. It features larger protection diodes at the inputs, includes an analogue signal processing stage optimised for MSGC signals [3, 4] and the on-chip capability to generate an alarm in case of an imminent discharge in the detector. Test structures of a circuit meant to quickly restore the baseline level following the very large pulses generated by heavily ionizing particles have been prototyped as well.

Two modes of operation are possible for both chips: in *deconvolution mode* the analogue signal processing stages will be used to achieve optimal bunch crossing identification during high luminosity running; in *peak mode* no signal processing takes place and the behaviour of the two chips is identical. This paper presents some results of the performance of a system which makes use for the first time of one APV6 chip operated in peak mode to readout a prototype MSGC built and operated according to CMS specifications.
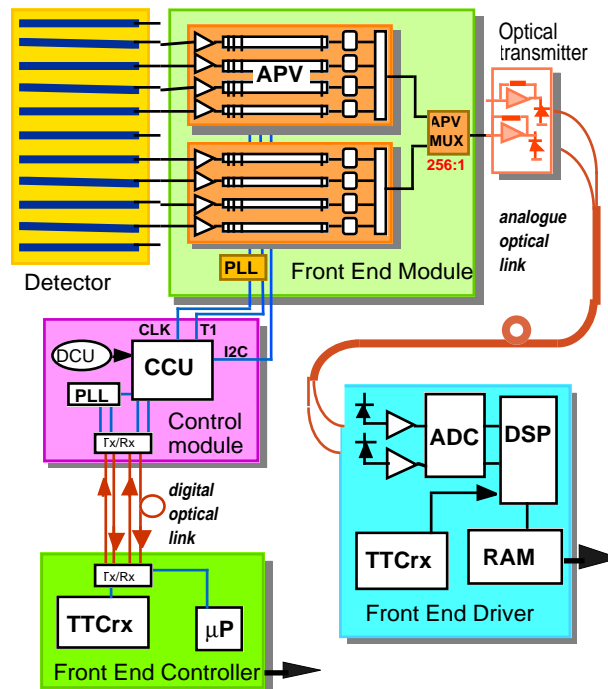
2 CMS Tracker Readout Scheme

Figure 1. CMS tracker system.

A block diagram of the CMS tracker readout scheme is shown in figure 1. On each of the Front End Modules the data from a pair of APVs are multiplexed onto one line by one APV MUX chip. Multiplexing is done at 40 MHz, therefore the APV output multiplexing stage must run at 20 MHz. The analogue signals are subsequently transmitted optically to the barracks for digitization and sparsification on a Front End Driver (FED) module. The Front End Module receives from a Control Module the slow control signals on a 2-wire bi-directional bus conforming to the commercial I^2C standard. The 40 MHz clock and T1 trigger signals are transmitted differentially and are recovered on the front End Module by an additional chip.

The tracker target performance can be summarised as follows:

- Low noise (CMS goal: <2000 e⁻ during the full operational lifetime).

- Low power consumption at the front end (CMS goal: ~2mW/channel)

- Adequate Bunch Crossing (BC) Identification (CMS goal: 1 BC (silicon) - 2 BC (MSGC)

- Synchronization desirable through the whole tracker

However it has been gradually understood that the BC identification issue is much more challenging than originally thought. This is discussed later.

3 The APV Front-end Chip

3.1   APV6 and APVM Common Features

The layout of the APV front-end chip is shown in figure 2. Each microstrip is read out by a charge sensitive preamplifier with a time constant of 50ns whose impulse response closely approximates an ideal CR-RC shape. This resulting pulse is sampled at the beam crossing frequency and stored into the analogue pipeline for up to the level 1 trigger latency of 3.2μs. Additional pipeline cells provide buffering for events awaiting to be read out.

Following a trigger to the chip (T1) the data will be read out and there are two possible modes of operation:

- in *peak mode* only the sample corresponding to the peak of the analogue pulse shape is read out for every channel and subsequently multiplexed out.

- in *deconvolution mode* three consecutive samples are read out from the pipeline for every channel and processed by an analogue circuit forming a weighted sum which is sent to the multiplexer stage for output.

A nested multiplexer architecture [5] allows some power saving and causes the analogue data to be output in a non-consecutive channel order.

Slow control of the APV is implemented using the 2-wire I²C serial bus. The master in the system is located in the Control Module (figure 1) and up to 15 APVs individually addressable can be connected to one bus and will always act as slaves. It is thus possible to access individually all the internal registers of the APV for appropriate setup, control and monitoring. Table 1 shows a list of the registers. All can be written to and read from except for the *error* and the *I-threshold* registers which can only be read from.

The APV6 and APVM have identical dimensions and pad layout thus allowing the development of common front-end sub modules both at prototyping and construction stages.
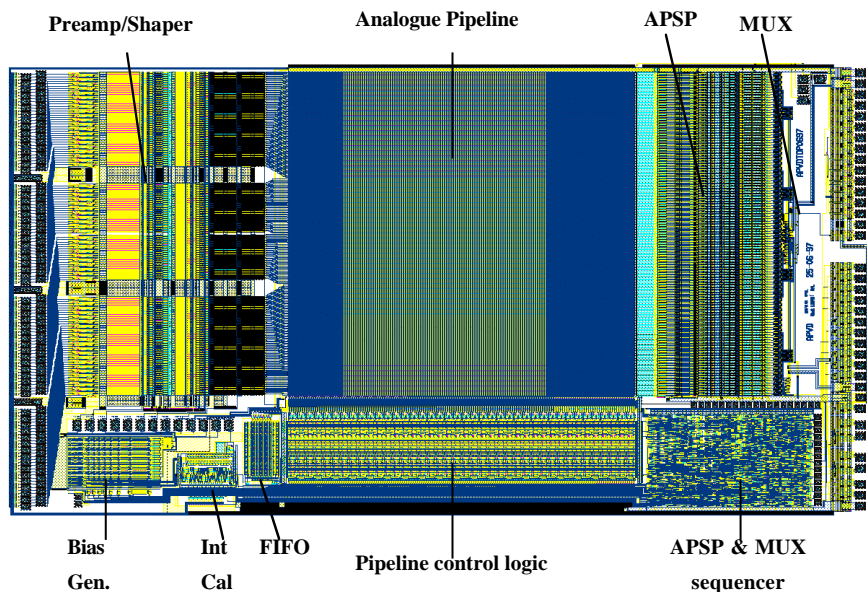

Figure 2. The APV front-end chip.

Table 1: APV6 internal registers

Register	Description
latency	distance between write and trigger pointers to pipeline. Value up to 160
analogue bias	4 currents and 4 voltages. Programmed values converted by on-chip DACs
mode	peak/deconvolution multi-sample (APVM only) bias ON/OFF power up/down) internal calibrate ON/OFF
cal pulse amplitude	programmable in ~625 electron steps up to ± 6 MIPs
cal skew	8 steps of 3.125 ns
cal mask	which of 8 cal lines to drive
error (read only)	latency error bit set if value read on chip ≠ programmed value. FIFO overflow bit set if too many triggers in too short a time
I-threshold	threshold for current sensing (APVM only)

3.2 APV6 and APVM Differences

The deconvolution operation is described in detail in [6]. In the case of silicon detectors, whose signals resemble delta impulses very well, the pulse produced by the preamp/shaper stage approximates very well an ideal CR-RC shape which is uniquely defined and can be described analytically. Inverting the transfer function of the shaper it is possible to calculate a set of three weights which, applied to three consecutive samples, ideally confine the signal to one bunch crossing only. This set of weights has been implemented in the APV6.

In the case of MSGCs, signals from the detector have a complex time structure which fluctuates greatly with an average charge collection time of 50ns. Consequently the pulse resulting from the preamp/shaper suffers from fluctuations in peaking time and amplitude. It is impossible in such a case to use the deconvolution method to obtain single bunch crossing identification. Even the CMS goal of two bunch crossings is hard to achieve and it has been shown [4] that an inevitable compromise between time tagging capabilities and signal size/noise performance must be reached. A set of three weights optimized according to these considerations for use with MSGC detectors has been defined [4] for implementation in the APVM. They are applied, as in the APV6, to three consecutive samples, so synchronization is trivially achieved across the whole microstrip tracker.

Another feature of the APVM dictated by necessities of operation in conjunction with a gas detector is a current sensing circuit at the input. Leakage current from groups of 32 adjacent channels is summed and compared against a threshold programmed via slow control. In case the threshold is exceeded, which can be a symptom of an imminent discharge in the gas detector, an alarm bit is set which can be transmitted to the control system for triggering a precautionary procedure to avoid the discharge.

4 Lab System Setup

A Sr^{90} collimated source is placed in front of the detector, a 100mm x 100mm x 3mm chamber filled with Ne(33)/DME(66), and a scintillator behind for triggering purposes. Simple NIM logic vetoes triggers in a 7μs window following a T1, the time needed to read out a complete data frame. It also provides synchronization to the DAQ. A prototype of the CMS Front End Driver (figure 1) module is used for digitization and the slow control is implemented via a simple VME I^2C interface card. The system can be remotely controlled via VME and the control and DAQ software are developed in LabView running on a PowerPC.
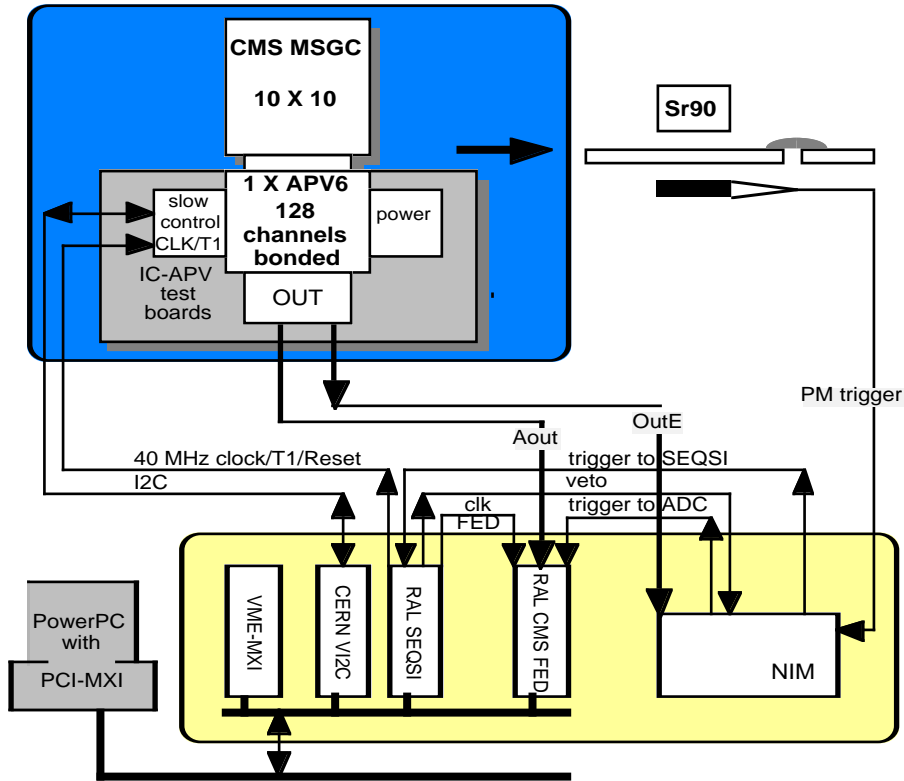
Figure 3. Schematic of the lab setup.

5 Lab System Calibration

The system calibration procedure included the tuning via I^2C of the pulse response of the preamp/shaper to approximate the ideal CR-RC shape, characterisation of the response of the 128 amplifiers and pedestal/noise measurements to identify channels behaving incorrectly. These procedures have been carried out before and after the bonding of the detector. Figure 4 shows the pulse shape of a typical channel bonded to the detector after tuning. The on-chip internal calibration system has been used for this purpose. Eight calibrate lines feed groups of 16 channels individually selectable via I^2C (cal mask, table 1). Following a Calibration Request pulse (two
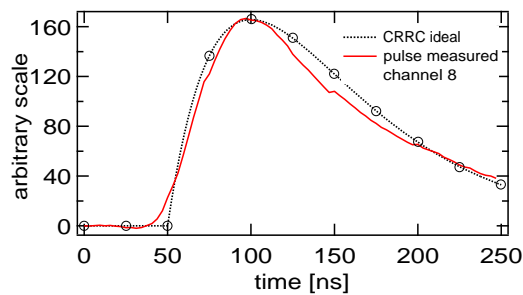

Figure 4. Impulse response of a typical channel tuned to approximate CR-RC shape.

consecutive T1 pulses), a voltage step is applied to a capacitor and the charge injected into the preamp. There is a capacitor for each channel whose value is known to within 20%. A T1 pulse is sent at the appropriate time to perform readout. Fixing the latency and T1 and moving the calibrate request in steps of 25ns, a coarse mapping of the pulse shape is possible at 25ns intervals. The cal skew register (table 1) can be used to delay the calibration pulse in fine steps within the 25ns intervals, thus achieving finer time resolution (3.125ns). The amplitude of the pulse can be programmed via I^2C (cal pulse amplitude in table 1). Using this procedure the impulse responses of the 128 channels have been measured and are shown in figure 5
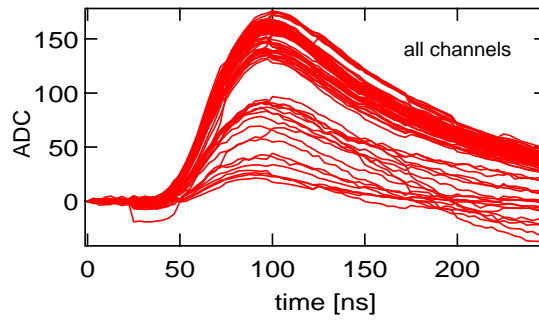
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Figure 5. Impulse response of the 128 channels bonded to the detector.
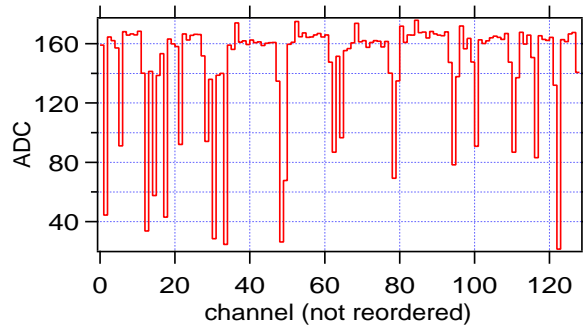

Figure 6. Gain of the 128 channels before reordering.

after baseline subtraction, while figure 6 shows the values of the peak of the pulse for the 128 channels in the order in which they come out from the chip and figure 6 illustrates their distribution. A conversion constant of 1 ADC channel ≈ 200 electrons can be calculated for the system. This value is consistent with other cross-check measurements performed. Typical channels exhibit a channel-to-channel gain spread consistent with the differences between the internal capacitor values. Incorrect behaviour of channels showing lower gain has appeared only after bonding to the detector.
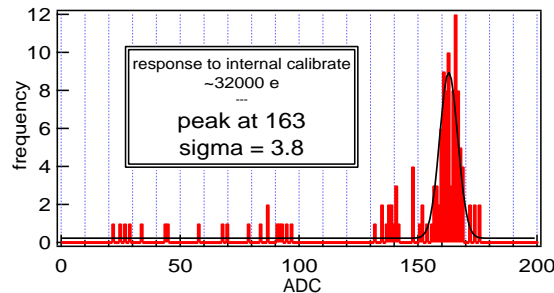

Figure 7. Gain distribution for the 128 channels.

Figure 8 shows a typical noise measurement before and after the bonding of the detector. Values are common mode subtracted and reordered to the correct channel sequence. Noise figures are consistent with expectations from previous measurements [1] for a strip capacitance of 5pF (0.4pF/cm, 12.5cm) but in this case anomalies in the noise performance of some channels have also appeared after detector bonding. This clearly indicates that anomalous behaviour is related either to the detector or the bonding. The gain values normalised to the most probable value of 163 ADC counts and reordered are superimposed in figure 8. A one-to-one correspondence between channels exhibiting anomalous values of noise and gain is clearly visible. In particular, the channels whose noise is lower than expected show minimal response to the calibration pulse. Channels with conspicuously higher noise show lower gain. A number of channels have gain slightly lower than the typical values (>0.8) while their noise values are as expected.

Looking at figure 6 it can be noted that these channels precede or follow in the readout sequence other channels with much lower response, which thus appear to be responsible for this effect.
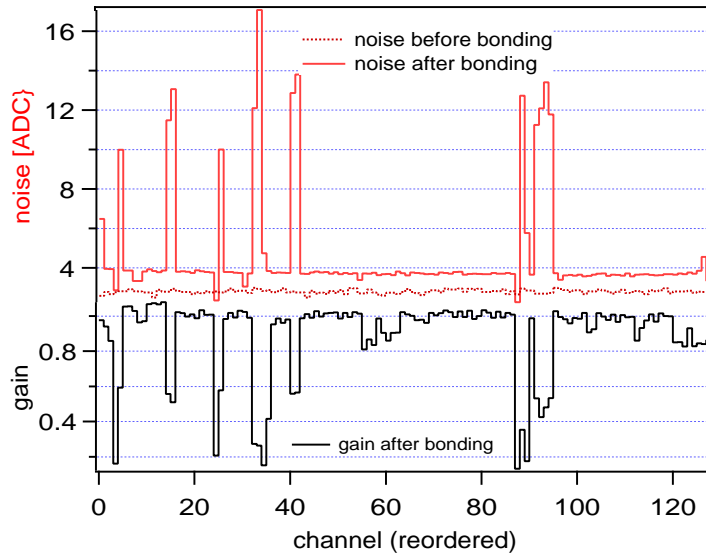
Figure 8. Gain and noise values after common mode subtraction and reordering

Going back to figure 8 it can be observed that channels showing anomalous behaviour are never physically isolated, but always come in groups of at least two adjacent. One possible explanation of this effect could be found in the bonding. The procedure is in fact quite laborious, involving two bonds per channel and rather long wires. Since bonding pads are laid out in a double row on the chip and on the intermediate pitch adapter, the bonding wires of adjacent channels stay on two different levels; they could touch each other shorting the inputs of the corresponding amplifiers, which could result in the anomalies observed. A couple of channels began showing higher noise and lower response only after several weeks of testing. This observation could support the hypothesis, in that mechanical stress could have lead to a contact between the two bond wires. A closer inspection under the microscope supports this hypothesis as well, although does not provide definitive confirmation.

6 Lab System Performance

The amplifier response to detector currents generated by ß's traversing the detector has been investigated. Given the nature of MSGC signals it is impossible to map the amplifier pulse shape for a single event using the APV6. A facility has been implemented as a testing tool on the APVM, in which, following a single T1, it is possible to send out 3 samples. With a sequence of 6 T1 separated by 75ns intervals it is therefore possible to readout up to 18 consecutive samples stored in the pipeline. It is however possible with the APV6 to perform a pipeline scan fixing the T1 time and changing the latency value in steps of 25ns. Acquiring a statistically significant number of events per step, it is possible to reconstruct an average pulse shape. Figure 9 shows the result of such measurement.
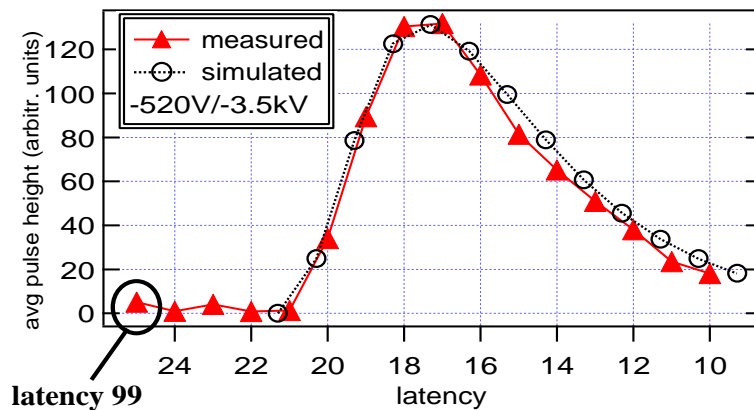

Figure 9. Average amplifier response to MSGC currents

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The chamber is operated at the nominal CMS working point (Vcath -520 V, Vdrift -3.5kV) and 10000 events acquired at each latency value; the averages of the charge spectra obtained after off-line cuts are then plotted (solid line). The dotted line corresponds to the average response of an ideal CR-RC amplifier with 50ns time constant to 10000 detector current generated with a Monte Carlo program [6]. The agreement with the measurement is excellent, especially on the rising slope, where are located the samples used in the APSP filter optimized for MSGC. Figure 10 shows the pulse height spectrum measured at the latency which ensures maximum efficiency. The noise of a typical channel is superimposed. S/N[1] is in excess of 25, again in good agreement with simulation predictions.
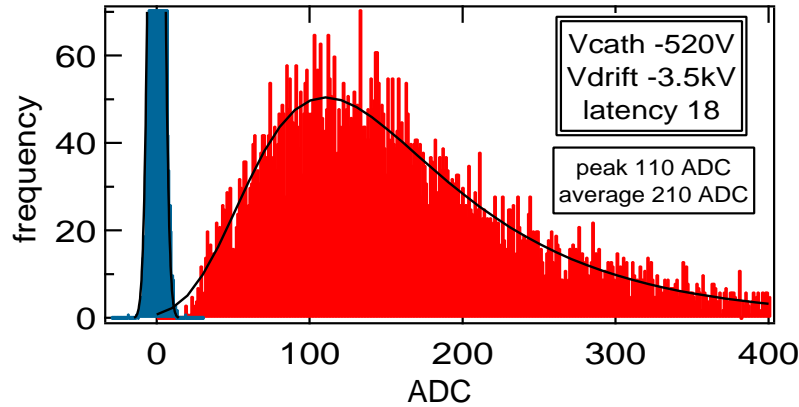

Figure 10. Pulse height spectrum with the trigger timed at the peak of the amplifier response.

Figure 11 shows the result of a cathode voltage scan. Even when a large voltage is applied to the chamber, no appreciable distortion from the logarithmic behaviour is visible. This shows that the dynamic range of the amplifier is suitable for application in CMS MSCGs. The gain is calculated acording to the following formula:

$$gain = \frac{ADC * 200}{N_{prim+sec} * BD}$$

where:

$N_{prim+sec}$ = 18 (peak) [7] and BD = 0.7 (loss due to ballistic deficit). This is estimated to be 0.25 due to 50 ns shaping [8] and 0.05 additional contribution due to the time jitter for different clusters.
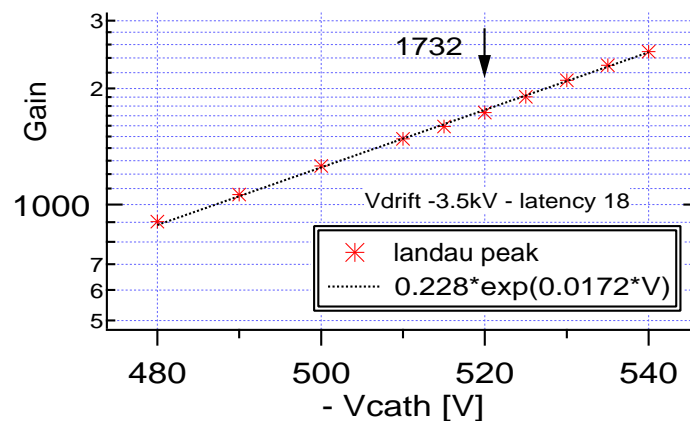

Figure 11. Gain of the chamber measured at different cathode voltages applied.

7 Conclusions

An APV6 chip operated in its low luminosity *peak mode* has been used for the first time to instrument a portion of a gas detector prototype for the CMS detector at the LHC. Even if optimized for readout of silicon detectors, the APV6 has been shown to be suitable to reading out gas detectors.

[1] S/N is defined, according to the CMS definition: peak of the landau over noise of one single strip (typical)

All the on-chip system features have been successfully used to tune-up and calibrate the system. The average amplifier response to detector signals has been reconstructed showing excellent agreement with predictions from simulations. The noise performance is as expected from previous measurements.

The APV6 design has been modified for optimal performance in conjunction with MSGC, resulting in the APVM chip, recently prototyped. It features an analogue pulse filter optimized for MSGC signals and a current sensing circuit at the input able to issue an alarm in case of imminent discharge in the detector. An additional operation mode has been implemented which allows multi-sample output for testing purposes. However, when operated in *peak mode* the chip should behave as the APV6. In this sense the measurements described in this paper are an indication of the suitability of the APVM for reading out MSGCs.

APVM prototypes have recently been shipped and are currently under test. Figure 12 shows the impulse response of the newly implemented APSP filter as measured in early tests. Agreement with expectation from simulation is excellent. Noise figures are in agreement with expected values as well. When the testing procedures will be complete, the APVM will replace the APV6 in the lab setup described in this paper. Once correct functioning is demonstrated, studies will concentrate on the performance of the APSP filter.
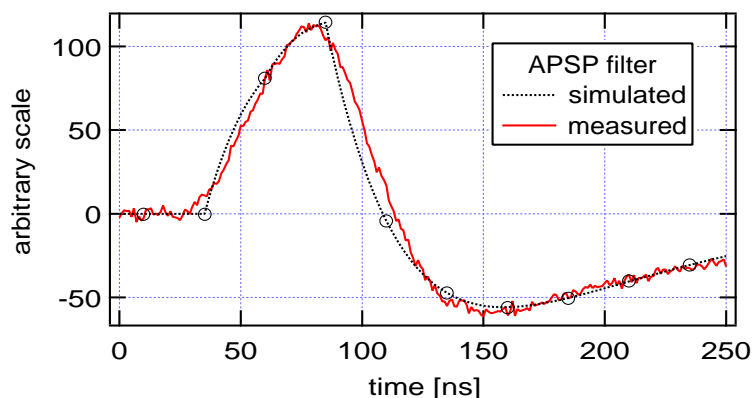

Figure 12. Impulse response of the APSP filter in the APVM chip

Acknowledgments

References

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