Performance study of a MWPC prototype for the LHCb Muon System with the ASDQ chip

LHCb Technical Note

Issue: 1

Revision: 1

Reference: LHCb Muon 00-062
Created: 13th July 2000
Last modified: 8th August 2000

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LHCb Technical Note 00-062
Revision: 1
Issue: 1
Last modified: 8th August 2000

Abstract

We report results from a beam test evaluating the front-end electronics for Multi-Wire-Proportional-Chambers (MWPCs) for the LHCb Muon System. The ASDQ chip with an adaption fulfils the requirements for the detectors in the entire Muon System. A time resolution of 3.2 ns at an operating voltage 3.15 kV was achieved with the gas mixture Ar(40%)CO_2(50%)CF_4(10%), translating into an efficiency of 99.5% for a 20 ns time window. An efficiency of more than 95% in a 20 ns time window is obtained for voltages above 2.95kV for all types of pads studied. Hence, the efficiency plateau is about 500 Volts.

Document Status Sheet

Table 1 Document Status Sheet

1. Document Title: Performance study of a MWPC prototype for the Muon System with the ASDQ chip			
2. Document Reference Number: LHCb 00-062			
3. Issue	**4. Revision**	**5. Date**	**6. Reason for change**
1	1	8 August 2000	First version

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1 Introduction

The LHCb Muon System is described in the LHCb Technical Proposal [1]. The L0 Muon Trigger of LHCb requires a coincidence of hits in all five muon stations within a certain spatial granularity. Therefore each station is required to have an efficiency >99%. In order to achieve this, a logical OR of two independent double gap chambers is foreseen in each muon station. High single layer efficiency within a time window of 20 ns can be translated to a timing requirement for a single chamber of less than 3.5 ns (RMS).

The double gap chambers are Multi-Wire-Proportional-Chambers (MWPC) with a wire pitch of 1.5 mm and 5 mm total gas gap. The required granularity is achieved by ORing signals from several wires (Wire-Pad) or by reading signals from segmented cathodes (Cathode-Pad). The detector capacitances range from a few pF to 200 pF. The expected rates per channel range from a few Hz to 800 kHz.

In this note we report test-beam results obtained from a double gap chamber prototype, developed at PNPI., that was operated in the X7 beam at the CERN SPS. The main focus of the test was the evaluation of the front-end electronics. We tested an adaption of the ASDQ chip (called ASDQ++) for different chamber parameters and particle rates that one can expect in LHCb.

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2 Chamber prototype

The wire chamber prototype we used is described in detail in [2]. It is a double gap MWPC with a sensitive area of 16×24cm^2 and a symmetric gas gap (cathode-to-wire distance) equal to 2.5mm.

The chamber was filled with the gas mixture *Ar(40%)/CO_2(50%)/CF_4(10%)*. Fig.1 shows a simplified view of the chamber together with the front-end electronics connected to both Wire-Pad and Cathode-Pad. The anode wires of 30 μm in diameter are oriented along the short side of the chamber. The wire pitch is 1.5mm. Wires were grouped in 8 separate Wire pads (W1-W8): 4 pads of 4×16cm^2 size and 4 pads of 2×16cm^2 size. The chamber has also 8 Cathode pads, 4 pads (C1A-C4A, C1B-C4B) of 4×8cm^2 size and 4 pads (C5A-C8A, C5B-C8B) of 2×8cm^2 size (see Fig.2). High voltage was connected to each Wire-Pad separately via a *2.7 MΩ* resistor. Cathode 1 was used as detector ground.

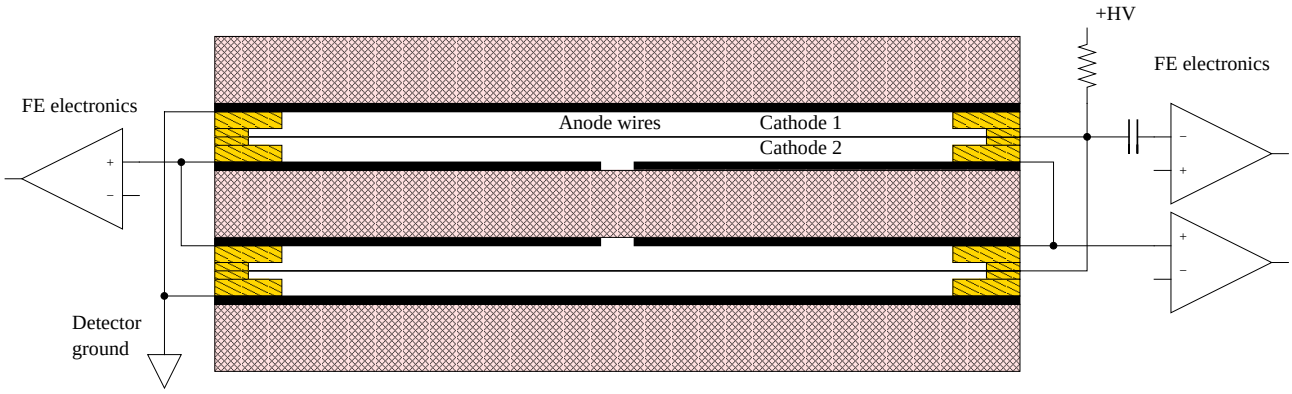

Fig.1. Schematic view of the double gap MWPC with the front-end electronics connected to the pads.

Table 1 presents the capacitance of various pads to the detector ground (C_{det}) of the MWPC prototype tested.

Table 1. Detector capacitance of various pads without (C_{det}) and with front-end board ($C_{det\ tot}$).

Pad size (cm^2)	C_{det} (pF)	$C_{det\text{-}tot}$ (pF)
Wire-Pad 4×16	≈100	≈115
Wire-Pad 2×16	≈60	≈80
Cathode-Pad 4×8	≈60	≈80
Cathode-Pad 2×8	≈40	≈60

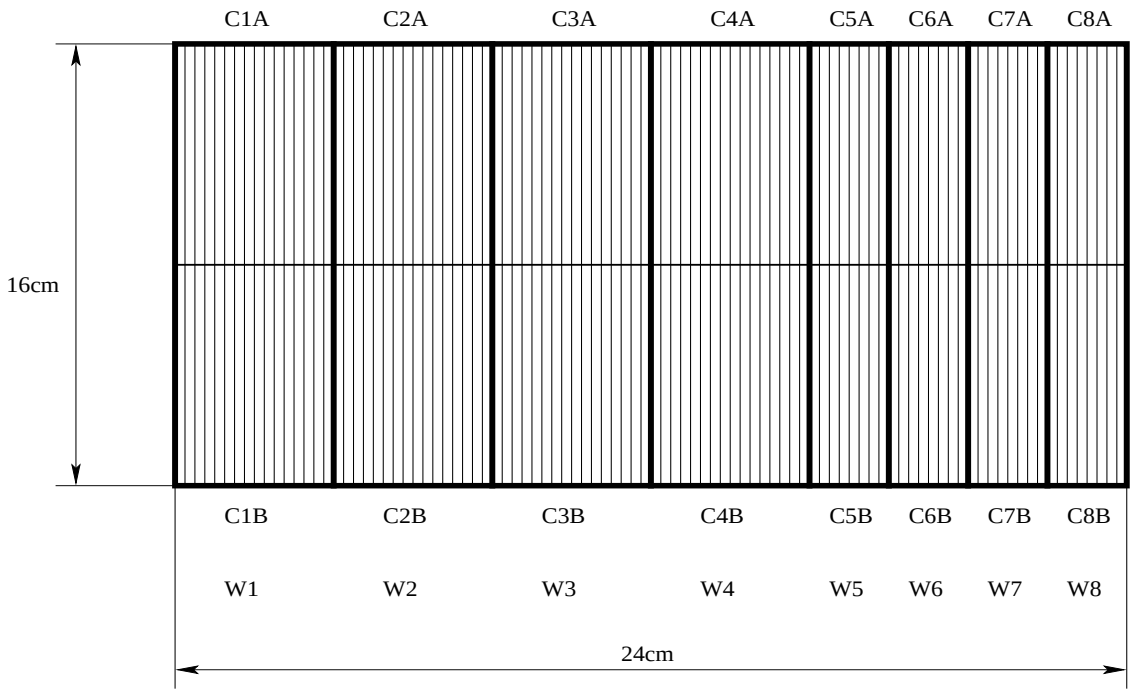

Fig.2. Wire-Pad and Cathode-Pad structure of the MWPC prototype.

O*nly the active area is shown.*

The total detector capacitance $C_{det\ tot}$ determines the serial noise of the front-end electronics and therefore the time resolution of the chamber. The detector capacitance and cross capacitance between pads are defined by the granularity and can not be changed in the given design. The cross capacitance between pads together with the input impedance of the amplifier determine the crosstalk in the system. To reduce crosstalk effects the input resistance of the amplifier must be as low as possible. Calculations show [3] that in order to achieve the required time resolution at reasonably low gas gain, the front-end electronics must have short peaking time (T_{peak}= 8-10ns) and low ENC (Equivalent Noise Charge <1fC, RMS) for a detector capacitance from a few pF to 200 pF.

The high rates in some of the Muon System regions (≈800 kHz/Pad) require in addition well optimized tail cancellation and baseline restoration circuits as well as a radiation hard technology. In order to minimize the inefficiency due to signal pile-up the signal pulse-width has to be as short as possible.

Below we present results obtained with the ASDQ chip, which was adapted to satisfy the requirements of the entire LHCb Muon System.

3 The ASDQ chip

The ASDQ is employed as a front-end chip of the Central Outer Tracker (COT) of the upgraded detector CDF-II at Fermilab [4]. It detects signals from drift cells, *3* meters in length, operating at a gas gain of about 2×10^4 with an $Ar/C_2H_6/CF_4$ gas mixture. The wires are terminated with R_T=300 Ω and the chip is operated at rather low threshold of about 2 fC without excessive noise count. In these conditions the ENC≈0.5fC (RMS) [4].

The ASDQ chip (currently available from the manufacturer MAXIM) is a further development of the known ASD-8 and ASDBLR chips [4, 5]. It has been implemented in the MAXIM analog bipolar process on a monolithic silicon substrate (*5.4mm×3.9mm*). Like the ASDBLR chip, it provides 8 channels of amplifier, shaper, baseline restorer, discriminator and output driver. Its shaping includes detector ion-tail cancellation well compatible with the $Ar/CO_2/CF_4$ gas mixture. The ASDQ chip is optimized for CF_4 tail cancellation and has no Xe option in contrast to ASDBLR. The baseline restorer eliminates threshold shifts that would occur at high hit rates (up to 20 MHz). A double pulse resolution study indicates that a second hit can be seen when it is separated from the first one by ≈50 ns. The impulse response of the ASDQ chip can be characterized by the peaking time of $T_{peak}\approx 8$ *ns* (C_{det}=0). The sensitivity of the chip *≈12.5 mV/fC* at C_{det}=0.

The chip has new features compared to the ASDBLR. It can provide measurements of the charge deposited by a particle (*dE/dx),* indicated with letter 'Q' in the title. The charge is encoded into the width of the pulse from the discriminator output. The feature can be enabled or disabled by an external digital level. There is a built-in calibration circuit which provides (separately for even and odd channels) the signal similar to one from the sense wire.

The power consumption is about *40 mW* per channel. The chip has been packaged in 64-pin flat package (PQFP) with the dimensions *12mm×12mm* and pin pitch *0.5mm*.

The ASDQ chip is radiation tolerant to several MRAD and *~10^{14} neutrons/cm^2*. The post-radiation measurements made on the ASD-8 and ASDBLR indicate suitable operation of these chips to several MRad and to doses of *3×10^{13} neutrons/cm^2* [4, 5].

In Fig.3 the simplified schematic of the ASDQ preamplifier is shown. There are two identical preamplifiers in each channel, which provide a DC balanced input to the differential shaper. Excellent common mode noise rejection is achieved in this way. This also allows negative (wire) and positive (cathode) read-out. The common emitter transistor Q1 provides high current gain of approximately β≈100 and a voltage gain of $\approx g_{m1}r_{e2}$, which in magnitude is close to unity. The common base transistor Q2 provides a voltage gain $\approx R_c/r_{e2}$. Therefore the total voltage gain of the circuit is $A \approx g_{m1}R_c$, which is equal to that of a single common emitter stage, but the bandwidth of Q1 is maximized. Both Q1 and Q2 exhibit wideband operation.

The cascoded Common Emitter – Common Base configuration of the ASDQ preamplifier has a rise time of *1.5ns* and an approximate gain of *2.5 mV/fC*. Ideally, as shown in Fig.3, an impulse

charge Q_{in} would be fully integrated onto C_f, resulting in an output voltage $V_{out}=Q_{in}/C_f$. In reality, however, the impulse sensitivity of the preamplifier (charge-to-voltage gain) is $1/C_{fx}$. Hence $V_{out}=Q_{in}/C_{fx}\approx C_f+C_{det}/A$, where $C_{fx} > C_f$, $C_{fx}= C_f+C_\pi+2C_{cb}+C_{det}/A$. A is the open loop gain ($A\approx100$, $g_m\approx15$ *mA/V at* $I_{e1}=0.4mA$) and C_π and C_{cb} refer to the base-emitter and the base-collector capacitance in the Q1 transistor. One can find from this considerations that at $C_{det}\approx40pF$ the output amplitude will be equal to half of the value at $C_{det}=0$. As a result, the detector capacitance can not exceed *40 pF*.

At low frequency the input impedance of the preamplifier shown in Fig.3 can be defined as $R_{inL}\approx R_f/A$. At high frequency (above $1/R_fC_f$) it depends on C_{det}, $R_{inH} \approx C_0 / g_mC_{fx}$. In the ASDQ chip C_0 was tuned to satisfy the requirement $R_{inL}\approx R_{inH}$. At this condition $R_{in}\approx280$ *Ohm* .

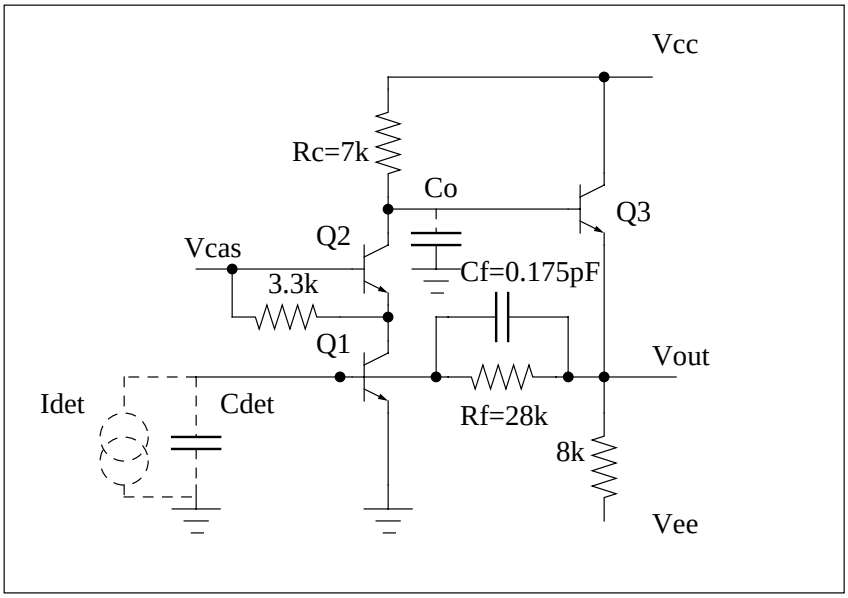

Fig.3. The ASDQ preamplifier schematic.

There are two identical preamplifiers in each channel, which provide a DC balanced input to the differential shaper. Excellent common mode noise rejection is achieved this way. This also allows negative (wire) and positive (cathode) read-out.

We can conclude that the ASDQ chip has many nice features, but very limited range of C_{det} and rather high R_{in}.

3.1 The ASDQ++

The simple modification shown in Fig.4 avoids both disadvantages. A common base transistor connected either to input *InA* of the ASDQ chip (in the case of wire read-out) or *InB* (cathode read-out) drastically improves the system. The input impedance can be reduced by an order of magnitude and is constant in a wide frequency range ($R_{in}=1/g_m \approx 25$ *Ohm at* $I_e=1$ *mA*). The detector capacitance can be extended by an order of magnitude, as shown in Fig.5. Both features are achieved without disturbance of the main characteristics of the ASDQ chip, i.e. its high performance at high rates, excellent pulse shaping (see Fig.6) and many other features.

We refer to the modified version as ASDQ++.

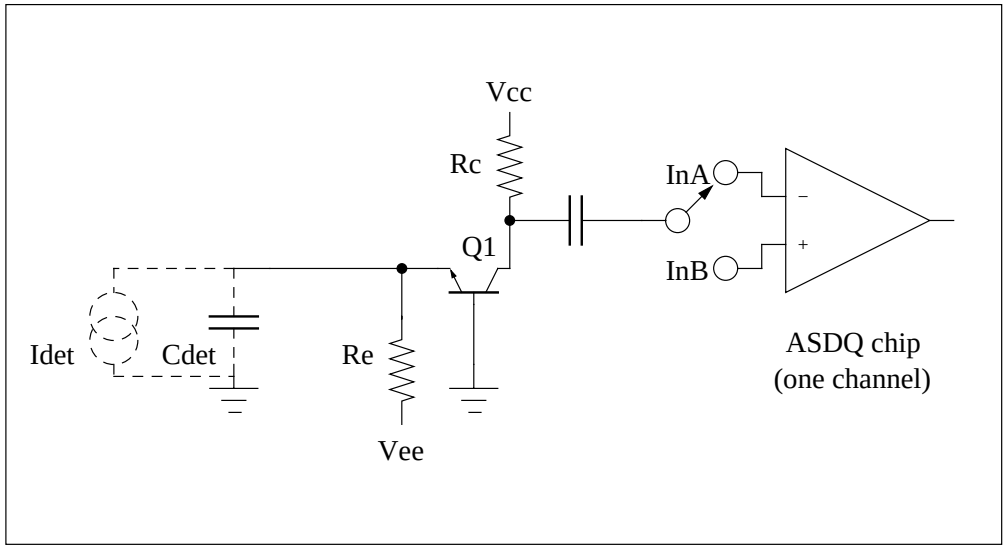

Fig.4. The modified schematic ASDQ++.

A common base transistor connected either to input InA of the ASDQ chip (in the case of wire read-out) or InB (cathode read-out) drastically improves the system. The input impedance can be reduced by an order of magnitude. The detector capacitance can be extended by an order of magnitude.

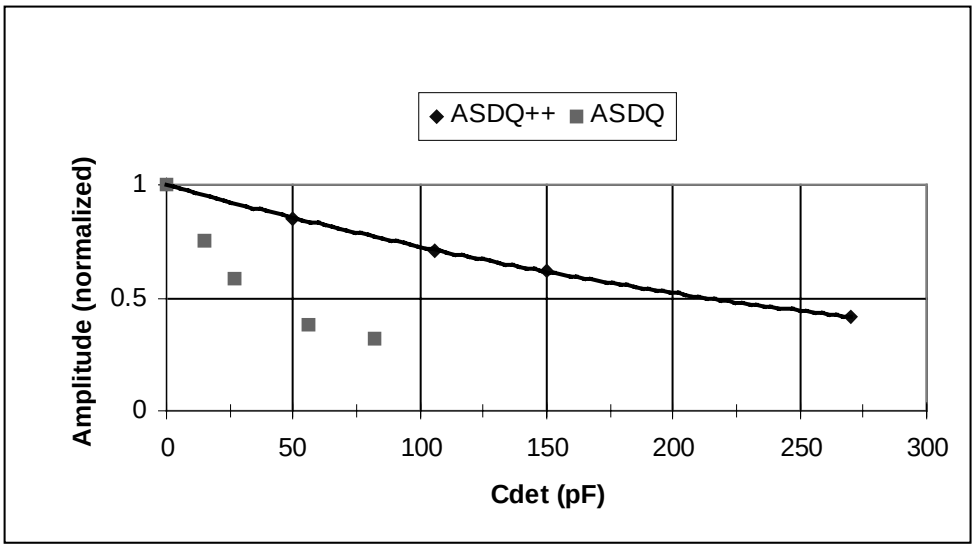

Fig.5. Dependence of the amplitude on C_{det} (measurements).

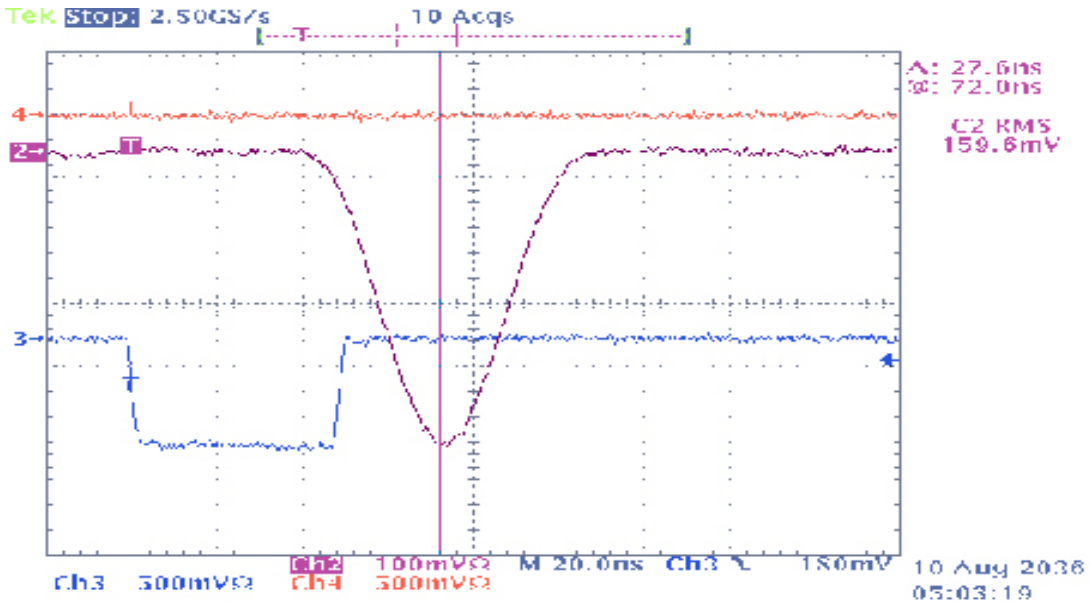

Fig.6. An example of signals recorded by scope with the ASDQ++ from minimum ionizing particles (120 GeV/c pions). *We find 27.6 ns collection time and 50ns dead time.*

3.2 Noise considerations

Fig.7 shows the Equivalent Noise Charge (RMS) versus detector capacitance for the ASDQ++. As expected, the measured noise is linear with the capacitance, and found to be:

$$ENC_{ASDQ++} = 1740 \text{ electrons} + 37 \text{ electrons/pF},$$

while for the ASDQ it is 1190 electrons +70 electrons/pF [4]. As one can see, at large C_{det} the parallel noise can be neglected and the serial component dominates. Better results in the case of ASDQ++ are obtained due to much lower base resistance r_{BB} of the first transistor compared to the integrated one. We have used BFR93A at emitter current $I_e \approx 1$mA. The modified scheme has longer T_{peak} (about 10 ns) due to the additional integration, which however also reduces the slope.

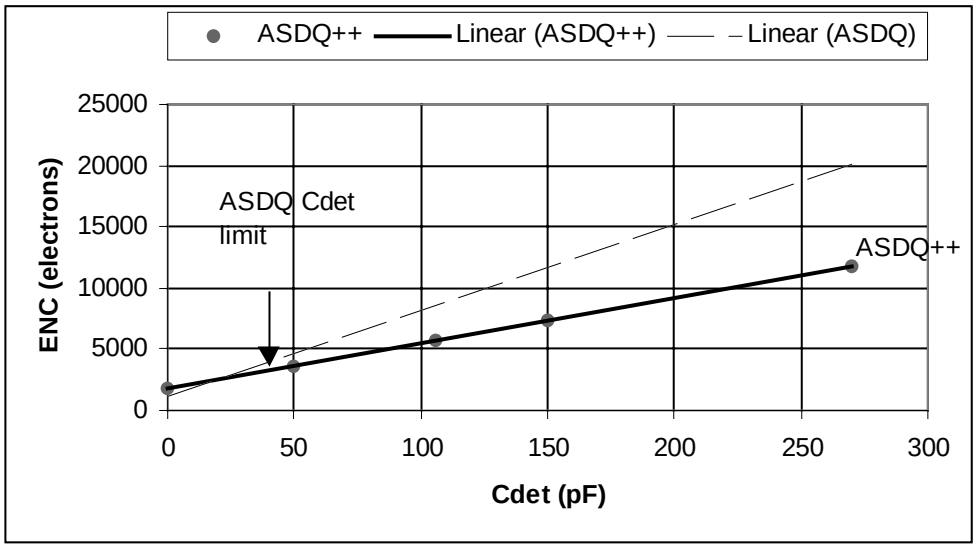

Fig.7. Equivalent Noise Charge versus detector capacitance.

4 Measurements

4.1 Experimental set-up

Measurements have been carried out at the CERN SPS, using the *120 GeV/c* negative pion beam X7. The experimental set-up is shown in Fig.8. The beam size was about *1cm* in the horizontal direction and *2cm* in the vertical one. To change the rate we used collimators. For triggering we used two scintillation counters: S1 (*15cm×15cm*) and S2 (*20cm×20cm*). In some measurements a small counter S3 with a width perpendicular to the beam of *1.8mm* (thickness *1cm*, length *5cm*) was used to improve the localisation of particles and to eliminate trigger dead time effects.

The coincidence of two or three counters within a 10 *ns* window provided the trigger signal. A hodoscope with 8 vertical and 8 horizontal scintillators (1×8 cm^2 each) provided a measurement of the beam position.

Constant-fraction discriminators were used for *S1* and *S2* to reduce the influence of the trigger signal time jitter to the time resolution measurements.

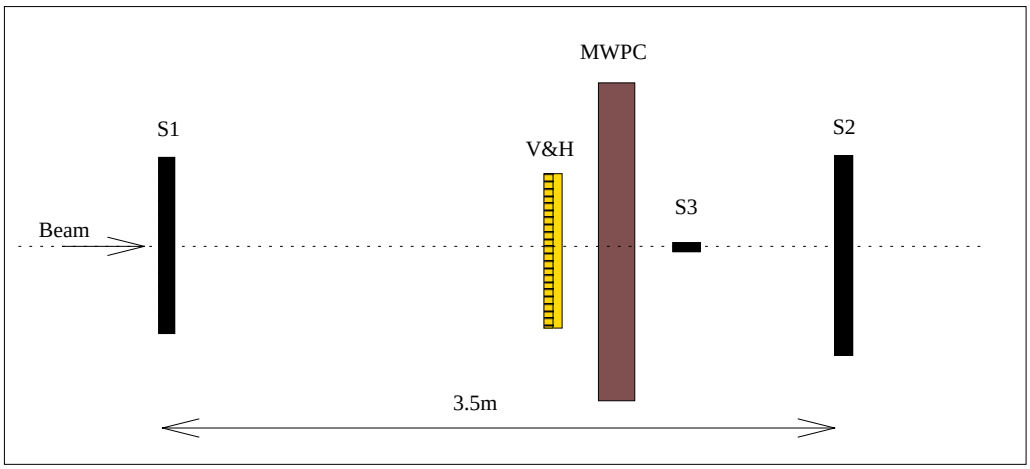

Fig.8. Experimental set-up.

4.2 Data Acquisition System

The Data Acquisition System (DAQ) is based on the CASCADE software package [6]. It reads the data from a VME front-end stage by means of a RIO processor (*CES, type 8061*) which was linked via Ethernet to a HP workstation.

Two types of interrupts were transmitted via a CORBO module (*CES, type 8047*):

- INT1 (Event type 1), at the end of a time gate of 1sec in duration. It was used for rate measurements and synchronized to the beam spill.
- INT2 (Event type 2), at each moment of the trigger signal arrival. It was used for time and charge measurements.

The following information was recorded by the DAQ:

- Time and amplitude of the signals from S1 and S2.
- Time of the signals from all hodoscope scintillators.
- Time of the signals from the MWPC equipped with ASDQ chip.
- Amplitude of the signals from channel 8 of the ASDQ chips.
- Scaler information, which was recorded twice: ones during the beam spill and ones in-between beam spills, in order to measure noise counts. For both cases a gate of *1 sec* was used to get the rate directly in Hz.

Multihit TDCs with time bins of *1ns* (*LeCroy type 1176, 16-channel, 16-bit*) were used for the time measurements. The Trigger signal was sent to the TDC as a Common Stop. In this mode of operation the TDC records up to 16 hits within a time of *64 μs* before the stop.

The ADCs (*LeCroy type 1182, 8-channel, 12-bit*) measured the charge in a gate set to *60 ns*. The ADC resolution is 50fC.

The digital signals sent to TDC were fanned out and sent to Scalers (*LeCroy type 1151, 100 MHz, 16-ch., 32-bit*).

5 Timing Measurements

The off-line event selection was done similar to [2]. The events were selected with several cuts applied to the raw data:

- *Shower rejection (Cut1).* Large amplitudes in the ADC spectra from the S1 and S2 counters were rejected: ADC (S1)<1300, ADC (S2)<1800.

- *Hodoscope selection (Cut2).* There should be exactly one in-time hit in both the H-plane and the V-plane of the hodoscope (coincidence between one vertical with one horizontal hodoscope counter). This helps to kill further the showers in the beam. A certain combination of the hodoscope counters could be selected to define a beam spot inside the pad.

The events passing *Cut1* and *Cut2* were used to calculate the efficiency and time resolution of the MWPC.

As examples, Fig.9 and Fig.10 show the ADC and TDC histograms from a Cathode-Pad C8A ($2\times8cm^2$). The center of the pad was positioned in the beam. The measurements were performed at HV=3.15 kV (Fig.9), corresponding to a gas gain of $\approx1\times10^5$, and HV=3.25kV (Fig.10) with approximately two times higher gas gain. The pedestal in the ADC spectrum is positioned in the channel 250 (not shown). The empty bins in the region below channel 500 demonstrates high efficiency in the ADC-channel (99.9%). The time resolution in the TDC spectrum between 200 and 300 channels was found to be 3.14 *ns* (RMS) and 2.46 ns (Sigma) at HV=3.15kV with the efficiency of 99.9%, 99.8% and 98.7% in the time windows of 25 ns, 20 ns and 15 ns. At HV=3.25kV the results are better, as expected for higher gas gain. Note that the ADC and TDC spectra measured at HV=3.15 kV for the Wire-Pad are quite similar to the ones measured at 3.25 kV for the Cathode Pad due to the 2 times larger induced signal.

Fig.11 shows the TDC histogram in which one can see the typical dead time of the channel. It was measured at high rate, about 500 kHz/pad. The width of the dead zone is equal to ≈50 ns and is in good agreement to the digital signal duration measured with the scope, as shown in Fig.6.

Threshold scan results for the ASDQ and ASDQ++ are shown in Fig.12. Measurements were done for a Cathode-Pad of $2\times8cm^2$ (C_{det}=40pF) at low rate (6-7 kHz/cm^2). One can conclude that both options give similar results at thresholds around 250-300mV (the operating point), but the ASDQ is even better at lower thresholds. It can be explained by the additional integration of the input signal with the ASDQ++.

A systematic study of the wire chamber performance was done for all types of pads shown in Fig.2. The efficiency and time resolution versus high voltage for the Cathode-Pad $2\times8cm^2$ (C_{det}=40pF) is presented in Fig.13. The ASDQ and ASDQ++ options one can compare at this detector capacitance (see Fig.26). For the higher detector capacitance (Cathode-Pad $4\times8cm^2$ and Wire pads) the measurements were performed with ASDQ++ only, see Fig.14, Fig15 and Fig.16.

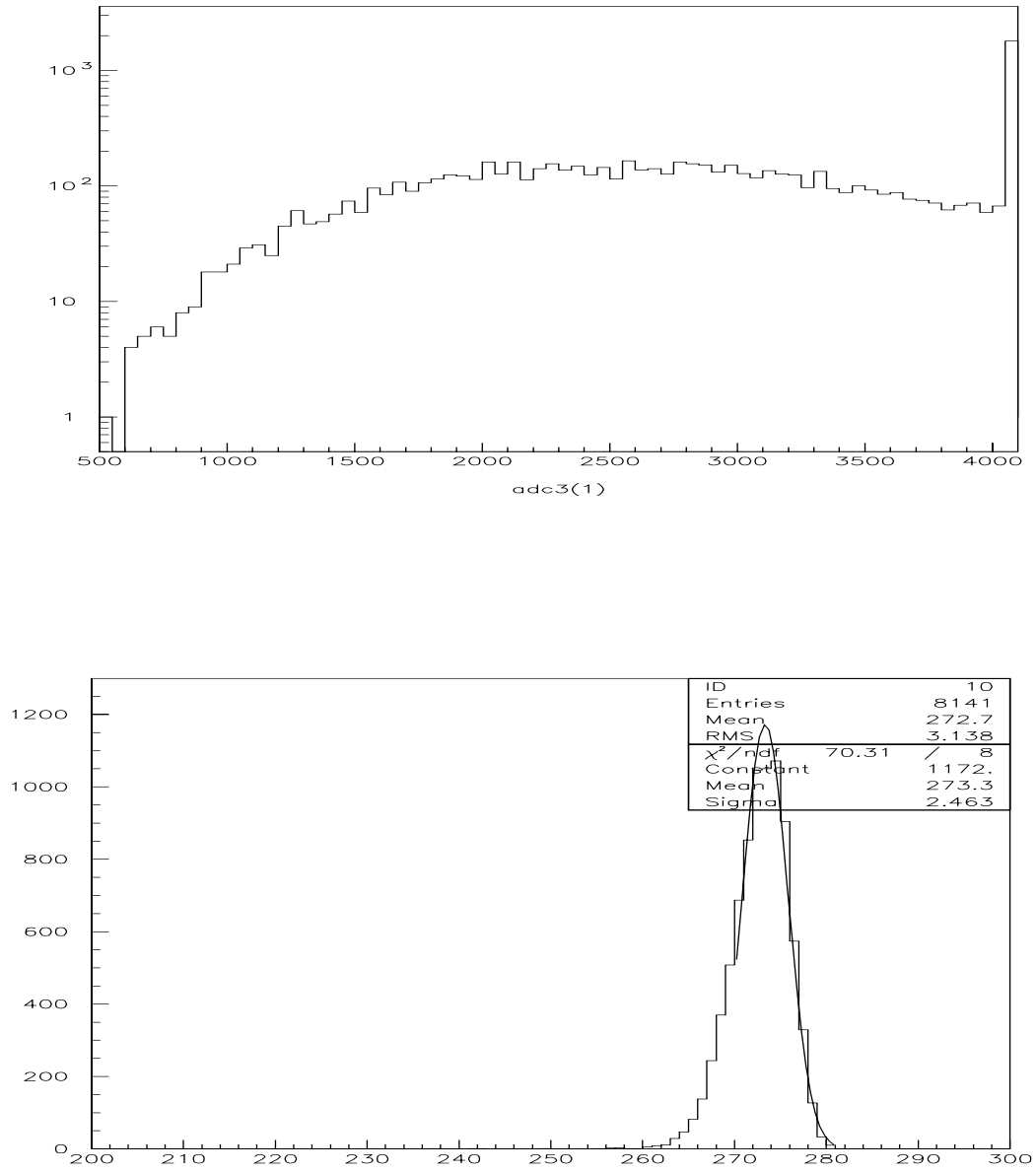

Fig.9. ADC (top) and TDC (bottom) spectra measured at HV=3.15kV.

Gas mixture Ar(40%)/CO_2(50%)/CF_4(10%), Gas gain ≈1×10^5, ASDQ++ Th=250mV, Cathode-Pad 2×8 cm^2.

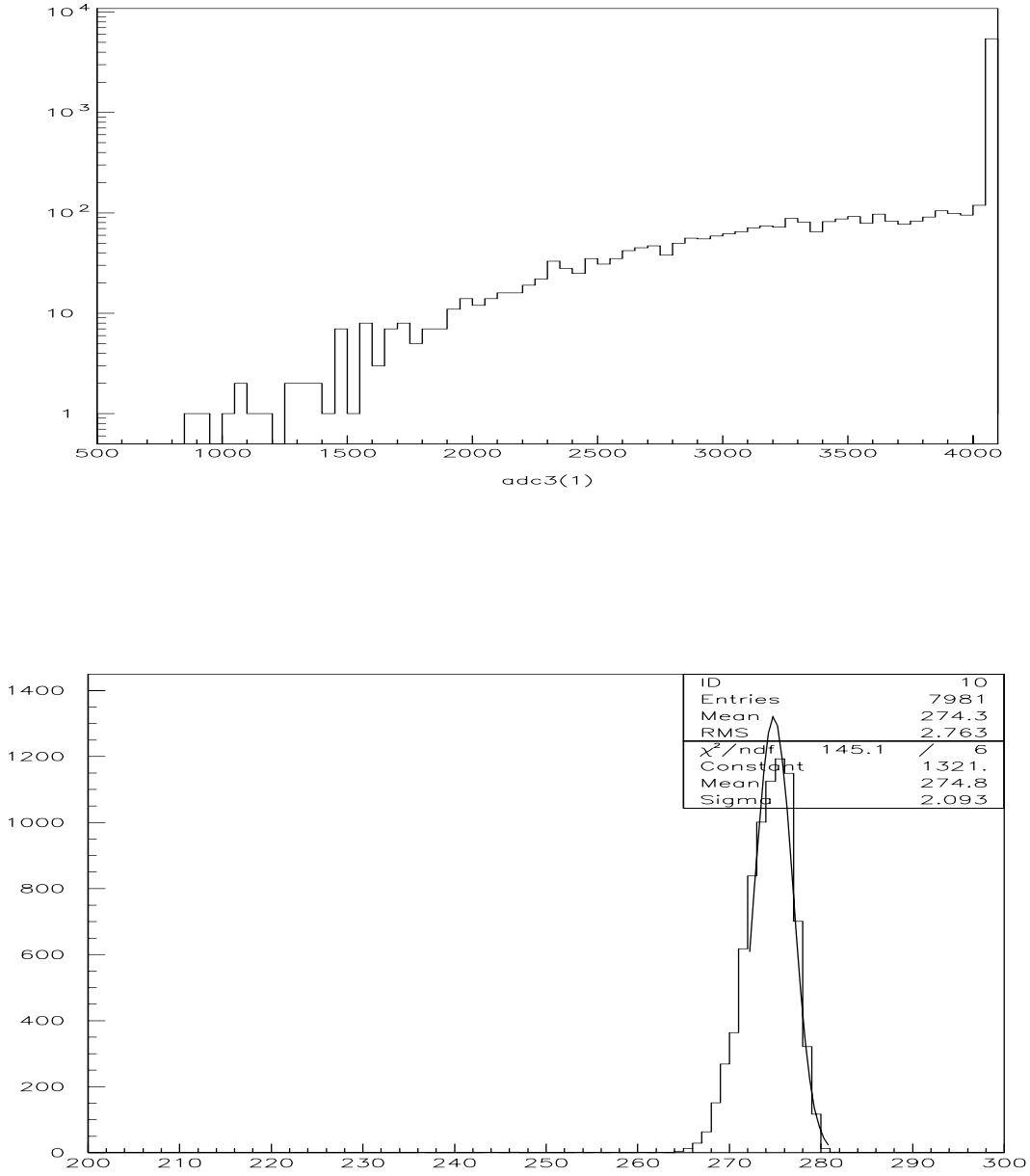

Fig.10. ADC (top) and TDC (bottom) spectra at HV=3.25kV (approximately two times higher gas gain).

We find similar ADC and TDC spectra for the Wire-Pad at HV=3.15kV and the Cathode-Pad at 3.25kV.

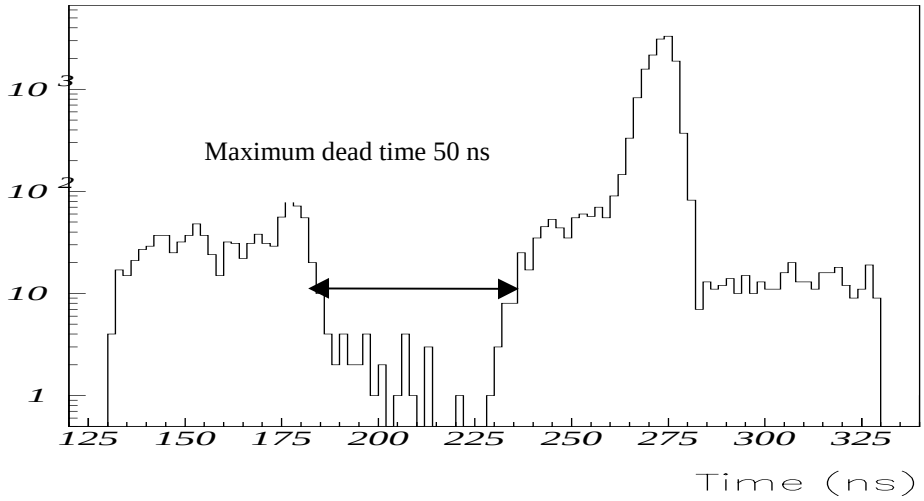

Fig.11. TDC histogram on a logarithmic scale obtained at high rate (*≈500 kHz/pad*) showing the dead time of the channel.

Time direction from right to left. The maximum width of the dead zone in the spectrum after the TDC peak is 50 ns which is in a good agreement with the digital signal duration given by the scope, see Fig.6.

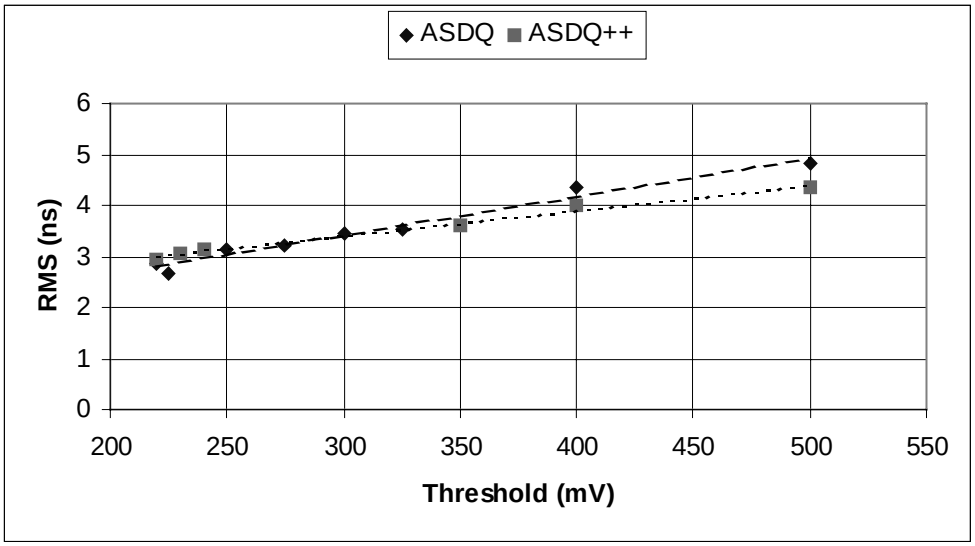

Fig.12. Threshold scan results obtained for ASDQ and ASDQ++.

Measurements have been made at low rate with the ASDQ chip for Cathode pad 2×8cm^2 (C_{det}=40pF) and with ASDQ++ for Cathode pad 4×8cm^2 (C_{det}=60pF). One can conclude that both curves are similar especially at thresholds around 250mV (operating point).

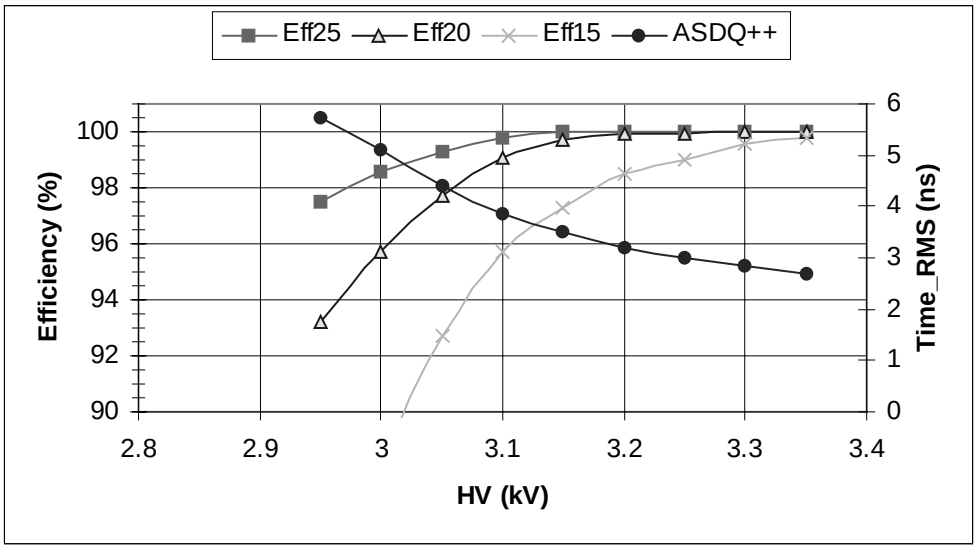

Fig.13. Efficiency in time windows of 25, 20, 15 ns and time resolution for a 2×8cm^2 Cathode-Pad. *ASDQ++ Th=250mV.*

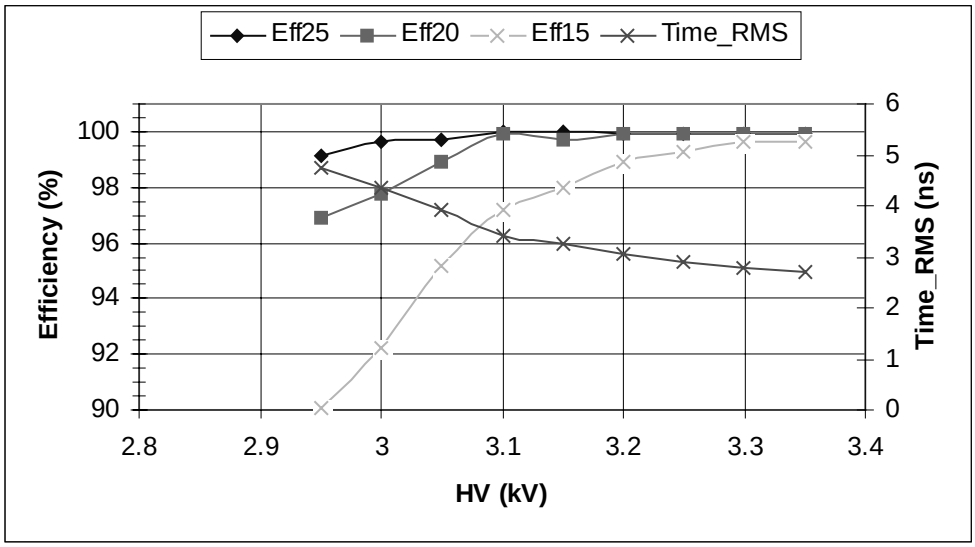

Fig.14. Efficiency in various time windows and time resolution for a 4×8cm^2 Cathode-Pad. *ASDQ++ Th=250mV.*

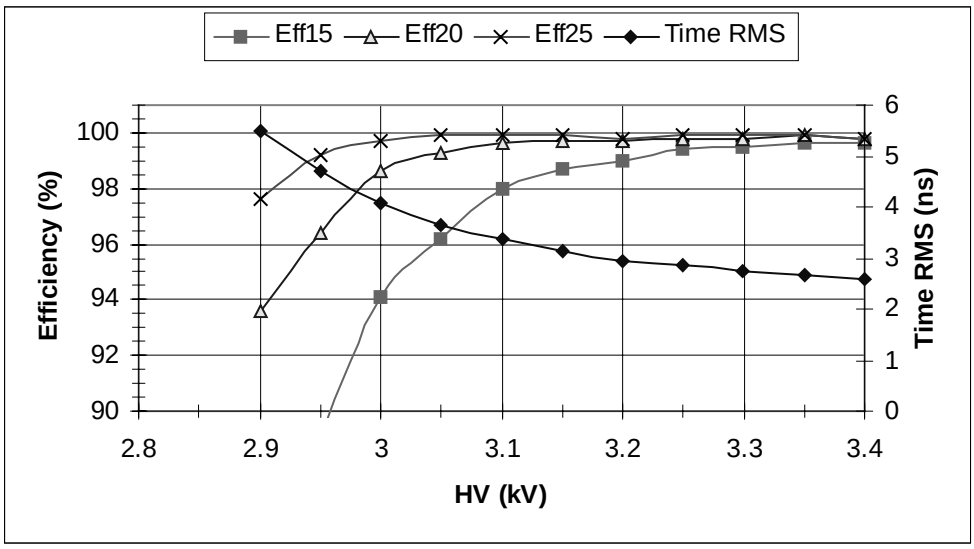

Fig.15. Efficiency in various time windows and time resolution and for a $2\times16cm^2$ Wire-Pad. *ASDQ++Th=300mV.*

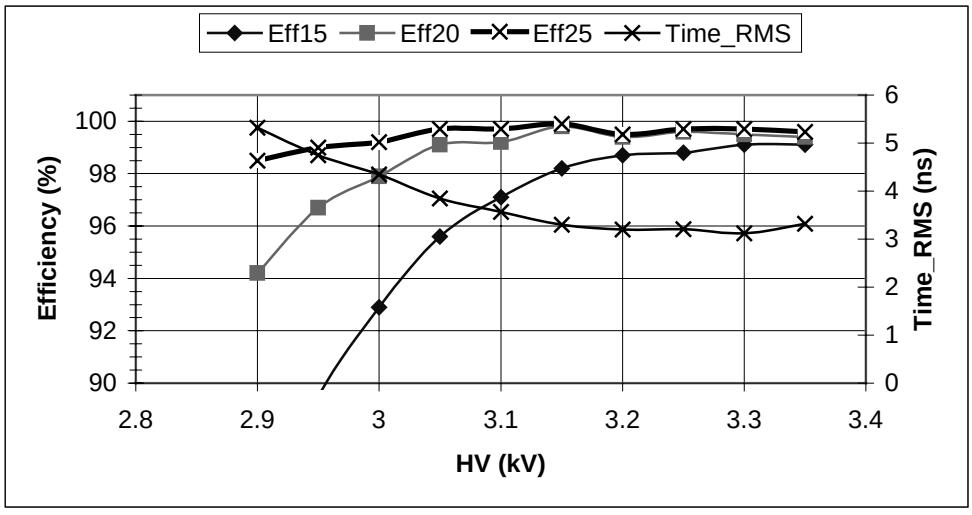

Fig.16. Efficiency in various time windows and time resolution for a $4\times16cm^2$ Wire-Pad. *ASDQ++Th=300mV.*

One can conclude from these measurements that an efficiency of more than 95% in a 20 ns time window is obtained for HV above 2.95 kV for all types of pads studied. Hence, the plateau length is ≈500 V. In a special set of measurements the detector capacitance of the Cathode pad $2\times8cm^2$ was artificially increased to 250 pF. This leads to an efficiency plateau in a 20 ns time window reduced by about 150 V, starting at 3.1 kV.

6 Crosstalk Measurements

Fig.17 shows the Cathode-Pad to Cathode-Pad ($4\times8cm^2$) crosstalk versus high voltage. Similar measurements were performed for the Wire-Pad to Wire-Pad ($4\times16cm^2$) crosstalk, as shown in Fig.18. The crosstalk has been defined as the ratio of hit counts on adjacent pads ($i\pm1$) to hit counts on the central one (i) where the beam was positioned. As one can see from Fig.17, at HV=3.15kV (operating point), the crosstalk is less than 5% which is acceptable. It is lower on the Wire pads with respect to Cathode pads, as expected due to the smaller cross capacitance.

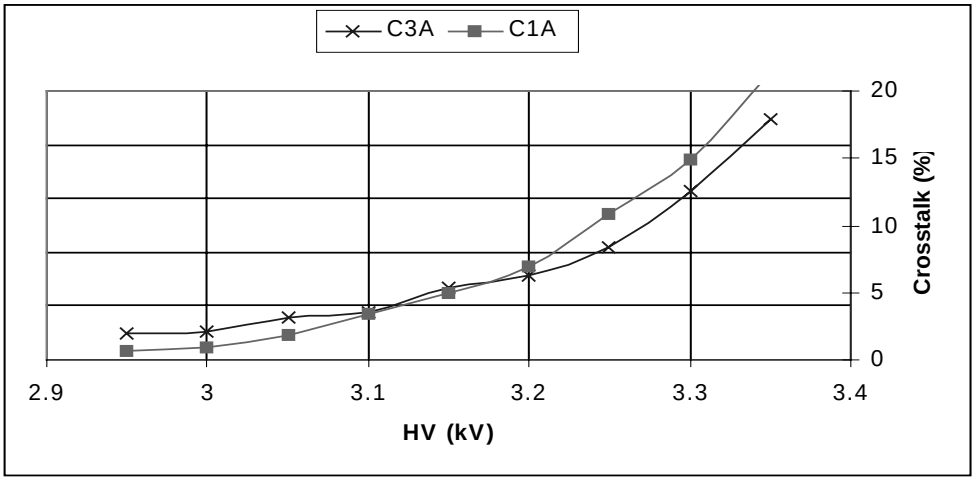

Fig.17. Crosstalk Cathode-Pad to Cathode-Pad.

The beam was positioned in C2A. ASDQ++Th=250mV.

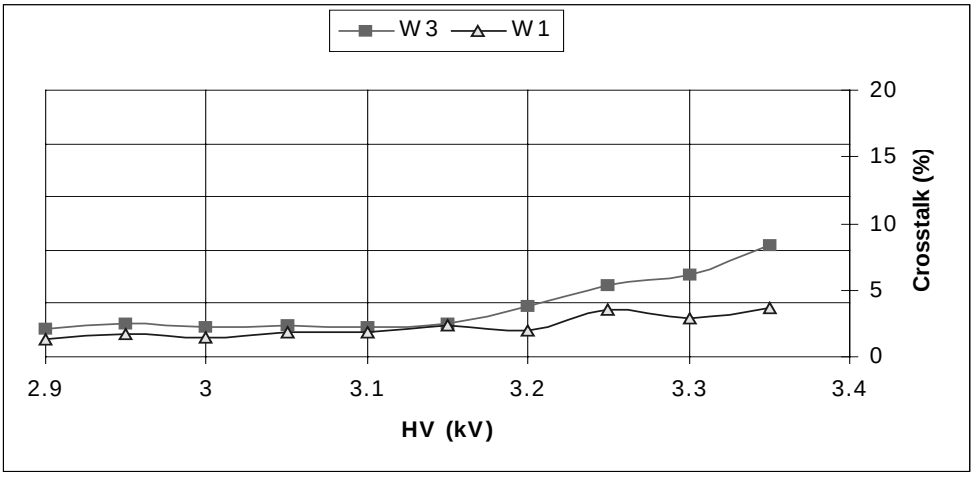

Fig.18. Crosstalk Wire-Pad to Wire-Pad.

The beam was positioned in W2. ASDQ++Th=300mV.

The cluster size is defined here as the mean number of fired pads for a incident beam position. The mean value, over all incident positions and at operational voltage 3.15 kV, obtained for Cathode-Pad is equal to 1.06 and for Wire-Pad to 1.04. In Fig. 19 the dependence of the cluster size versus high voltage is presented. During these measurements the beam incident point is at the center of a pad.

Using the small counter S3 (see Fig. 8) in coincidence with S1 and S2, we have carried out a scan across Cathode Pads (2x8 cm^2). Fig. 20 shows the cluster size evolution during the scan. As one can see, there is a maximun when the beam is passing between the pads. The width of this `bump' is related to the gas gap of the chamber.

Fig. 21 shows that the 20 ns time window efficiency is reduced to the level of 98% and the time resolution (RMS) reach 4 ns when the beam is passing between the pads. The width of the `bump' correspont to the width of the S3 counter (1.8 mm).

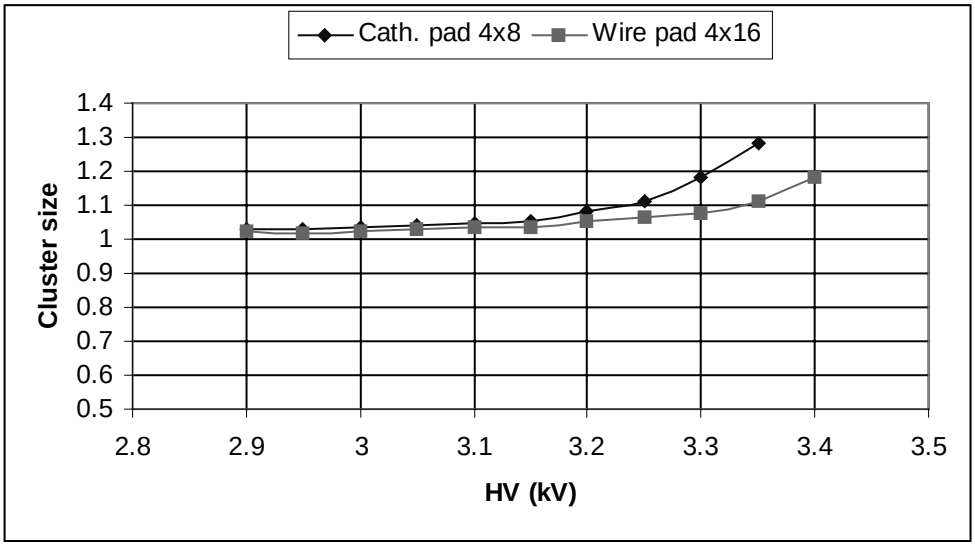

Fig.19. Cluster size mean value versus high voltage measured for both Cathode (4×8 cm^2) and Wire pads (4×16 cm^2).

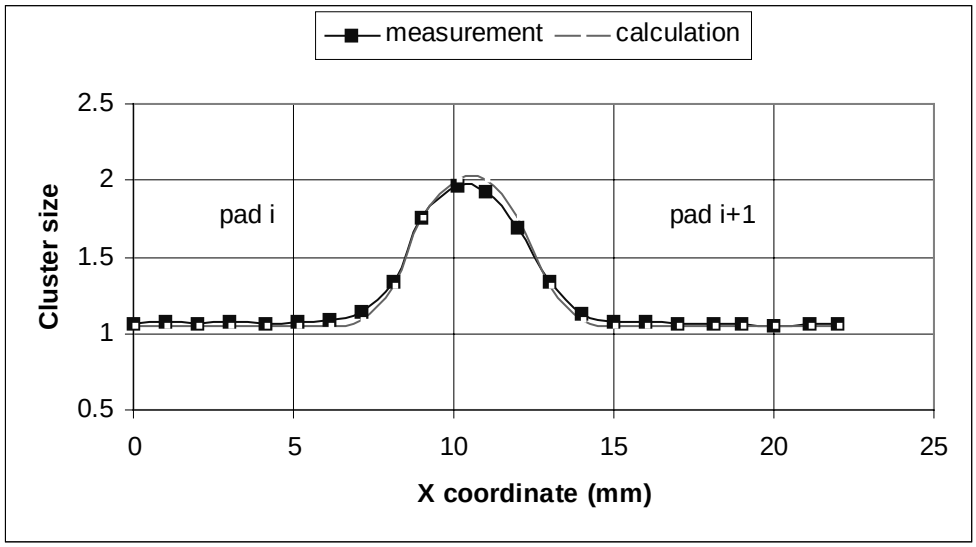

Fig.20. Cluster size versus position across Cathode pads (2×8 cm^2).

The calculation is performed for the threshold corresponding to 4 primary electrons. ASDQ++Th=250mV. The width of the 'bump' is related to the gas gap of the chamber.

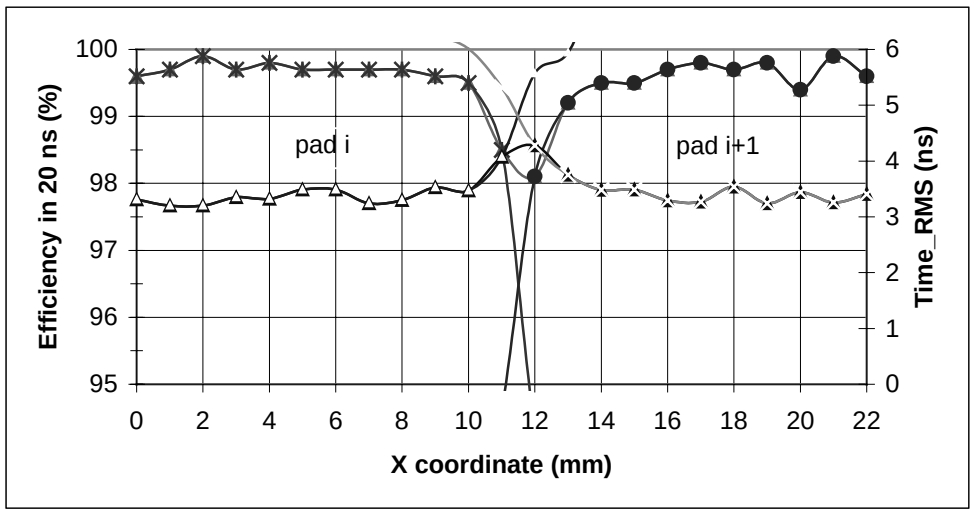

Fig.21. Efficiency in a 20 ns time window and time resolution (RMS) of the MWPC measured across Cathode pads (2×8 cm^2).

The efficiency is reduced to the level of 98% and the Time_RMS is increased from 3 to 4 ns. The width of the 'bump' corresponds to the width of the counter S3 (1.8 mm).

7 High Rate Measurements

The performance of the chamber was studied at various beam intensities (rates) from a few *kHz/cm^2* to *100 kHz/cm^2*, which was the maximum achieved for the beam line X7. However, it was enough to get rates of *500-600 kHz/pad (channel)*. As expected, with high rates one can find reduction of the efficiency due to signal overlap. Fig. 22 shows the efficiency reduction on the level of 0.3% per *100 kHz/pad* in a 25 ns time window and of 0.4% in a 20 ns time window. Fig.22 also shows that the time resolution is stable with rate. The fit gives a constant time resolution of 2.74 ns (Sigma) for all TDC spectra measured for the wire-pad of 2×16 cm^2 at various rates.

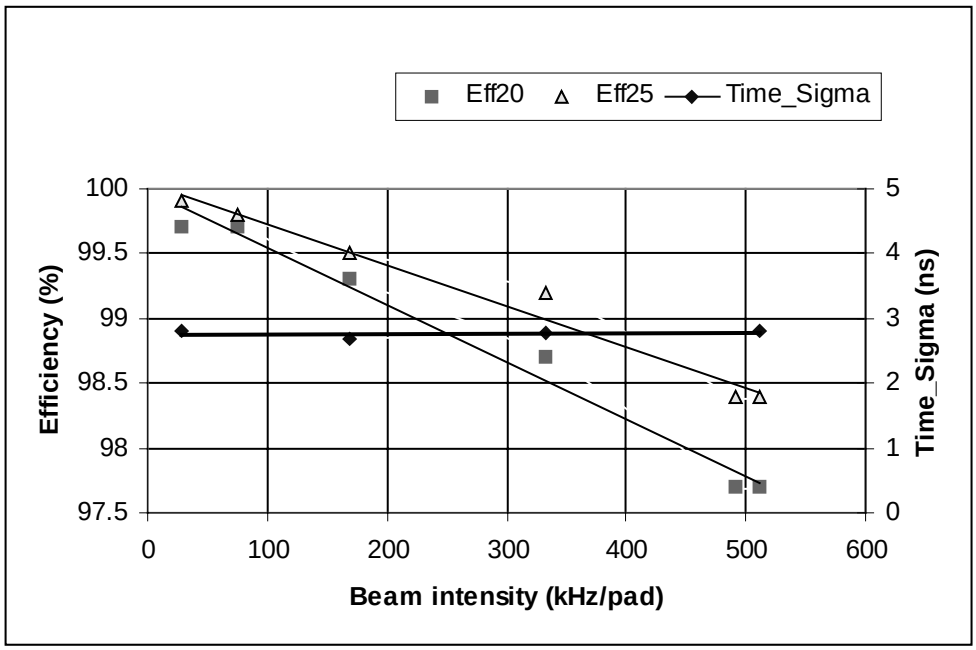

Fig.22. Rate dependence of time resolution and efficiency in 20ns and 25ns time windows.

HV=3.15 kV. ASDQ++ Th=300mV. The result of the linear fit gives an efficiency reduction on the level of 0.3% per each 100 kHz/pad in a 25 ns time window and of 0.4% in a 20 ns time window. The time resolution is stable with rate. The fit gives a constant Sigma=2.74 ns for all TDC spectra measured for the Wire-Pad 2×16 cm^2 at various rates.

8 Comparison with other Amplifiers

At present we have accumulated data with four types of front-end electronics: SONY [7], PNPI [2], ASDQ (without modification) and ASDQ++. Their performance on the same MWPC with very similar gas mixtures is compared below.

Fig.23 shows the time resolution versus high voltage measured with the SONY chip for a Cathode pad of 4×8 cm^2 size. The chamber was filled with *Ar(40%)CO_2(45%)CF_4(15%)*. As one can see, the results are worse compared to ASDQ++ even at very low thresholds of the SONY chip. Another drawback of the SONY chip is the higher input resistance of about 100 Ohm (together with spark protection resistors), large deadtime (up to 160ns) and limited radiation tolerance (100 kRad).

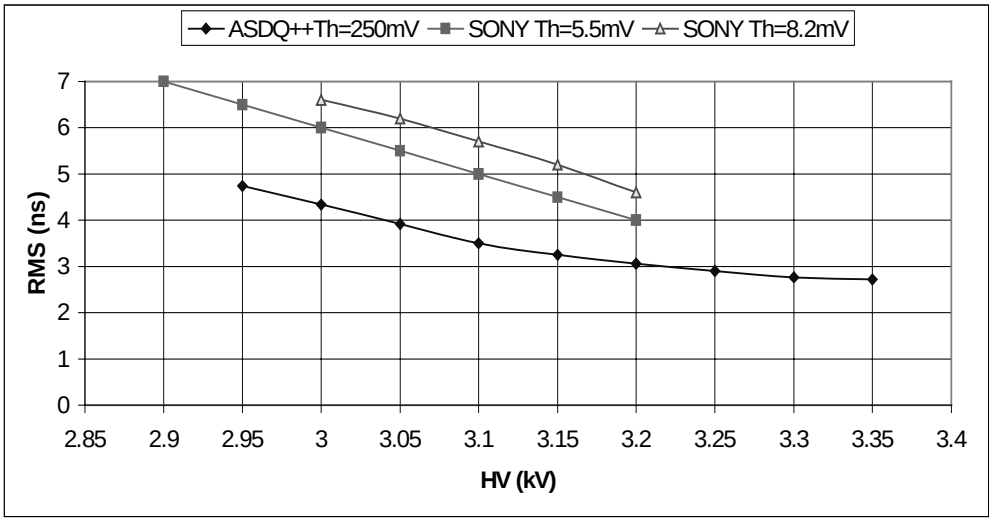

Fig.23. Time resolution comparison for two chips, SONY and ASDQ++. *The gas mixtures: Ar(40%)CO2((45%)CF4(15%) in the case of SONY and Ar(40%)CO_2(40%)CF_4(10%) in the case ASDQ++.*

Many results were obtained with the PNPI front-end electronics. It is an amplifier constructed with discrete components. A standard discriminator (*LeCroy, type 4416*) has been used for measurements with this amplifier. Fig.24 shows the time resolution versus high voltage for the PNPI (Th=40mV) and ASDQ++ electronics (Th=250mV) for the same chamber and the same Cathode pad (4×8 cm^2). The gas mixture was *Ar(40%)CO_2(50%)CF_4(10%)* in both cases. As one can see, the results are very close at HV=3.15 kV (operating point) and differ a bit around this point. It can be explained by the difference in the peaking time. The systematic shift is compared in Fig.25. One can conclude that both curves are quite similar.

In Fig.26 efficiencies in a 20 ns time window are compared for various front-end solutions: PNPI, ASDQ and ASDQ++. One can conclude that the results obtained for cathode-pads 4×8 cm^2 are very similar. However, as shown in Fig 27 and Fig.28, Cathode-Pad to Cathode-Pad crosstalks are quite different. The ASDQ++ results obtained at Th=250 mV are better compared to the PNPI

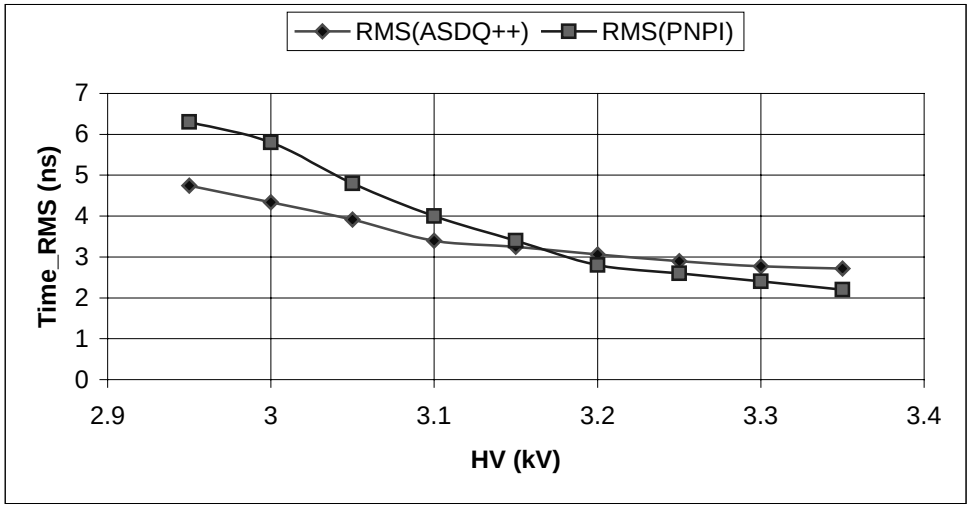

Fig.24. Time resolution comparison for PNPI front-end amplifier and ASDQ++.

PNPI Th=40mV, ASDQ++Th=250mV. The gas mixture in both cases: Ar(40%)CO_2(50%)CF_4(10%).

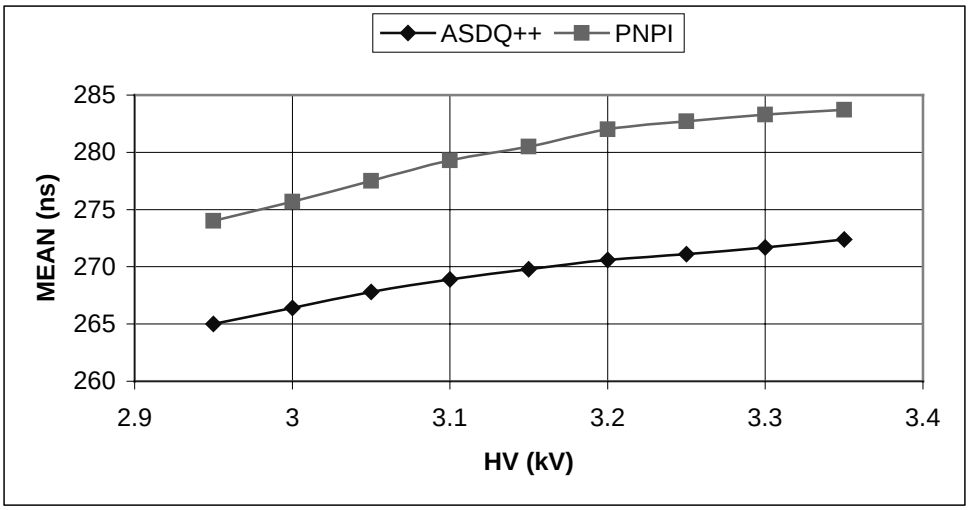

Fig.25. Systematic time shift comparison for PNPI front-end amplifier and ASDQ++.

PNPI Th=40mV, ASDQ++Th=250mV. The gas mixture in both cases: Ar(40%)CO_2(50%)CF_4(10%).

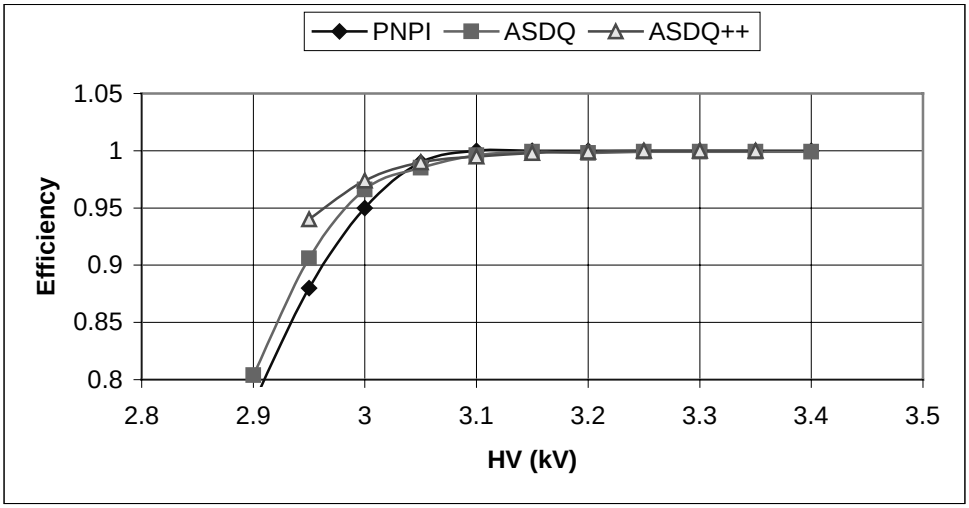

Fig.26. Efficiency in a 20 ns time window comparison for various front-end solutions.

Cathode pad 2×8 cm^2. The gas mixture in all cases: $Ar(40\%)CO_2(50\%)CF_4(10\%)$.

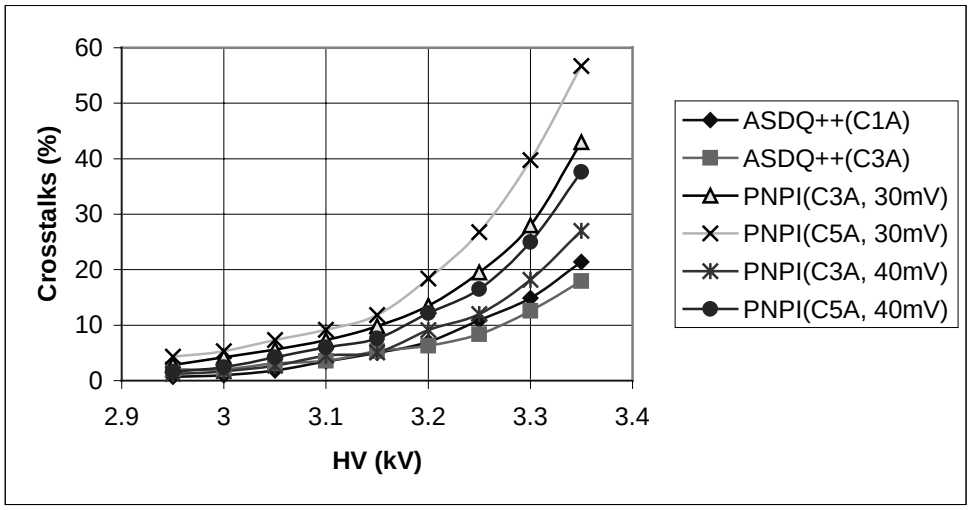

Fig.27. Cathode-Pad to Cathode-Pad crosstalk comparison for PNPI front-end amplifier and ASDQ++.

PNPI Th=30mV and Th=40mV, ASDQ++ Th=250mV.
Cathode pads 4×8 cm^2.

results at Th=30mV and still better for a higher threshold of 40mV.

Fig.28 illustrates the crosstalk comparison between ASDQ and ASDQ++ solutions. As was expected, crosstalk at high input impedance is rather high.

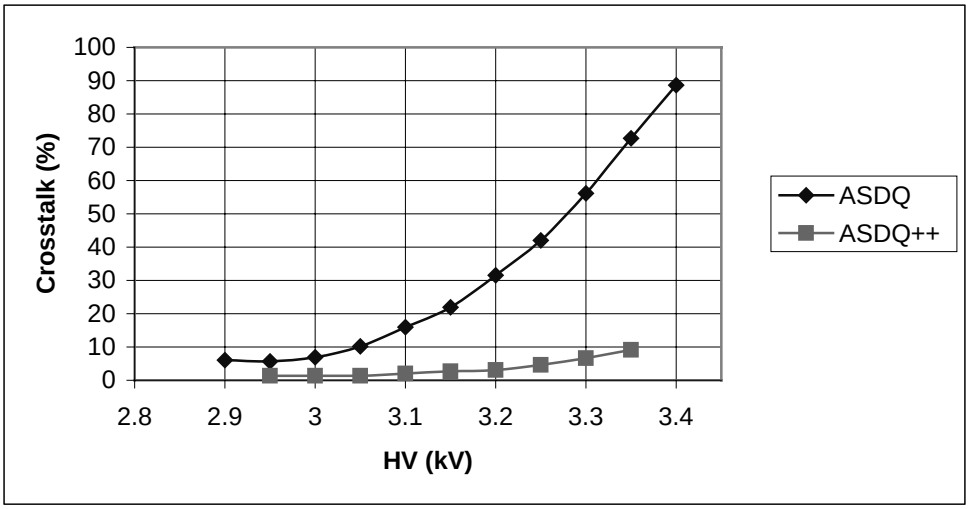

Fig.28. Cathode-Pad to Cathode-Pad crosstalk comparison for ASDQ and ASDQ++. *Cathode pads 2×8 cm*^{2}.

9 Conclusion

The ASDQ chip is well adapted for the wire chambers with the Ar/CO2/CF4 gas mixture and 30um wire diameter. The peaking time of about 8 ns, ion tail cancellation and baseline restoration result in an average dead time of 50ns. Although the timing behaviour is excellent, the application of the ASDQ chip is limited by the large input impedance (280 Ohm) and the limited range of detector capacitance (<40pF).

As shown in this report, all these problems can be solved with a common base transistor at the input of the ASDQ. A total input impedance of about 50 Ohm (25 Ohm input resistance of the common base transistor together with the two spark protection resistors of 10 Ohm each), ENC of about 1.6 fC at C_{det}=200 pF and sensitivity loss of 50% at C_{det}=200 pF were achieved. This makes it possible to use the ASDQ chip in the entire LHCb Muon System.

Measurements on a MWPC prototype with Cathode pads ($C_{det\text{-}tot}$=80 pF) and Wire pads ($C_{det\text{-}tot}$=115 pF) showed an efficiency of 95% in a 20 ns time window for a voltage ≈2.95 kV. The plateau extends up to 3.45 kV. The working point is 3.15 kV where we find a time resolution of 3.2 ns and an efficiency of ≈99% even in a 15 ns time window.

The crosstalk is bellow 5% at the HV working point, although the Cathode-Pad to Cathode-Pad capacitance in this MWPC prototype is rather high and can still be reduced in the next design.

The time resolution was measured to be constant up to rates of 100 kHz/cm^2 and 500-kHz/channel. The inefficiency due to signal pileup is 0.3(0.4)% per100 kHz for a 25(20) ns time window, as expected for an average pulse-width of 50 ns.

The crosstalk and cluster size on the boarder of two cathode pads are well in agreement with simulations.

Acknowledgements

We would like to thank M.Newcomer for many discussions and for providing the ASDQ chip for these measurements. We express our gratitude to B.Bochin for the MWPC prototype costruction, A.Lai and D.Marras for their help on the board design, V.Suvorov for his help on the gas mixture. We wish also to thank A.Vorobyov and H.J.Hilke for many useful discussions and suggestions.

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