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Custom Integrated Front-End Circuit for the CMS Electromagnetic Calorimeter

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Custom Integrated Front-End Circuit for the CMS Electromagnetic Calorimeter

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Abstract

A wide dynamic range multi-gain transimpedance amplifier custom integrated circuit has been developed for the readout of avalanche photodiode and vacuum phototriode in the CMS electromagnetic calorimeter for LHC experiment. The 92 db input dynamic range is divided into four ranges of 12 bits each in order to provide 40 MHz analog sampled data to a 12 bits ADC. This concept, which has been integrated in rad-hard full complementary bipolar technology, will be described. Experimental results obtained in lab and under irradiation will be presented along with test strategy being used for mass production.

I. INTRODUCTION

The readout chain of the CMS crystal calorimeter requires to cover a wide dynamic range (92dB) of signals to be digitized each 25 ns. Such calorimeter does not need a signal over noise ratio as high as the dynamic range for high energy signals [1]. In addition, the maximum resolution of present ADC for such sampling rate is often limited to 12 bits. The technique used in our case, for taking into account the requirement that the ADC resolution must not impair the performance of the system, is a linear multi-gain switching circuit. Such architecture has been recently integrated on a single chip in a full complementary bipolar technology.

This circuit, originally designed for the $PbWO_4$ crystal electromagnetic calorimeter of CMS for the LHC experiment, consist of a low noise transimpedance amplifier , matched to a pair of avalanche photodiode (APD), followed by a four ranges sampler and multiplexer, running at 40 MHz. In addition, temperature and photodetector leakage current readout circuitry is also included on chip, to monitor the state of the detector.

This paper is organized as follows. In Section II, the principle of operation of this circuit is described. Detailed description of some critical blocks are presented in Section III while chip layout is discussed in Section IV. Section V is devoted to experimental results obtained. Finally some concluding remarks will be given in Section VI.

II. SYSTEM OVERVIEW.

The block diagram of the circuit, named Floating Point PreAmplifier (FPPA), is depicted in Figure 1. The transimpedance amplifier is the first active electronic element of this circuit which has to convert the current coming from a pair of APDs into a shaped voltage with a high precision (low noise) and a dynamic range of 92dB. Following the preamplifier are four gain stages, with gains 1, 5, 9 and 33. The gain stages have clamps to prevent saturation. The four channels sampler and multiplexer, which selects the gains and multiplexes them to an ADC, follows the gain stages. It consists of a series of analog switches, comparators and digital logic. Directly after the gain, analog switches are used to form a sample/hold amplifier. Comparators on the three highest gain stages along with digital logic determine which gain stage has the largest, non-saturated signal and multiplex that signal to the ADC via the output buffer. The digital logic also outputs a code indicating which gain range was used. Each 25 ns, the circuit provides analog sampled data covering the whole input dynamic range of 92 dB with a precision of 12 bits. In other words, when switched in range 33, the noise coming from the APD and the preamplifier dominates compared to the value of the ADC quantum while when switched in range 1, the quantization noise of the ADC dominates. For normal data taking, the circuit operates in automatic mode and samples the waveform as described above. In addition, a "force" mode is foreseen to select any of the four ranges, especially for gain calibration procedure. Theses modes are selected by four unlatched digital lines.

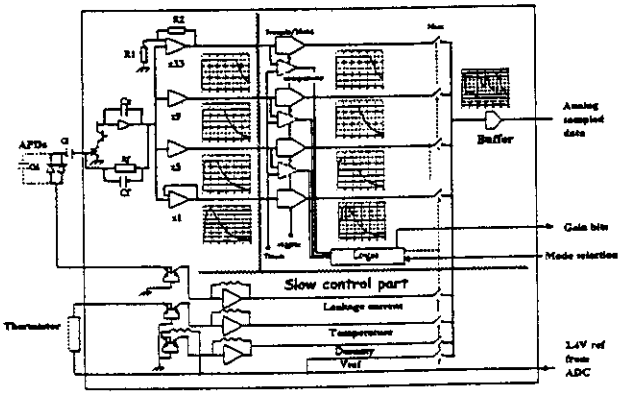

Figure 1: Block diagram of the FPPA.

Two auxiliary inputs allow the readout of an external temperature sensor and photodetector leakage current. The temperature input is matched for a 100kΩ at 25°C thermistor. A high value resistance was chosen to reduce self heating. An internal dummy channel is used to control the baseline voltage variation during operation under irradiation. The current readout circuitry monitor and convert the leakage current of the APDs from 100 nA to 20 µA into a voltage. In addition, the internally buffered and distributed voltage coming from the ADC reference voltage is also monitored. Four additional

switches have been added to multiplex the slow control data to the main output and are selected by a dedicated "force" mode.

III. CIRCUIT DESCRIPTION.

This section focuses on detailed circuit descriptions of the sensitive parts of the design linked to the performance needed. This concerns particularly the preamplifier, the gain stages and the slow control readout chain.

A. Preamplifier and gain stages.

The simplified schematic of the preamplifier and gain stages is shown in Figure 2. The preamplifier converts the photocurrent into a voltage waveform to be sampled. The linear transimpedance amplifier topology was used instead of the charge amplifier due to its good capability to process signals for high dynamic range applications [2], and also for saving power dissipation because it does not require additional pulse shaping circuits behind. As seen from the schematic, the passive R_fC_f -network associated with the compensation capacitance C_c, along with the detector capacitance C_d and the resistance R_1 of the input stage performs the $(RC)^2$ shaping of the output pulse; therefore no additional shaping stage is needed. The shaping time constant has been fixed to τ=40ns [3].

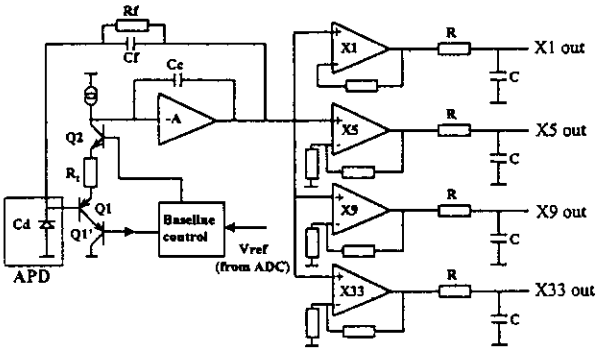

Figure 2: Simplified schematic of the preamplifier and gain stages.

The full scale input charge of 60 pC, corresponding to a 1.5 TeV event in a crystal, gives an output pulse of 2V. The source capacitance is equal to 200 pF, cable capacitance included. Detailed shaping calculations could be found in [3]. The inverting amplifier, labeled A, is a modified bipolar version of the CMOS source-coupled class AB amplifier proposed in [4].

The increase of the base current of Q_1, due to irradiation, also increase the voltage drop across R_f and therefore decrease the output DC operating point of the preamplifier. A baseline control circuitry has been added to prevent DC voltage shift during operation. It consists of a transresistance amplifier which tracks a copy version of the input transistor base current trough Q_1, and adjust the base voltage of Q_2, keeping constant the output DC voltage.

The input PNP transistor was chosen to have a low base resistor value (rbb') and the highest current gain β. The main sources of noise of the preamplifier come from the feedback resistor R_f, the base current of the input PNP transistor and the metal resistor R_1. The noise contribution of the collector current I_c of Q_1 is negligible compared to the one of R_1. The equivalent noise charge referred to the input is given by:

$$ENC^2 = \left(\frac{2qI_C}{\beta} + \frac{4kT}{R_f}\right)\tau + \frac{4kTR_1}{\tau}(C_d + C_f)^2 \qquad (1)$$

where τ is the shaping time constant, C_f and C_d are respectively the feedback and detector capacitance. The total simulated output noise is 55 μV rms which gives an ENC of 10000 electrons.

The preamplifier output pulse is sampled each 25 ns by subsequent S/H stages. In normal operation, the peak sample P_k and its two neighbors will be summed to reconstruct the energy deposited in crystals. The P_{k-1} sample, situated 25 ns before the peak, belongs to the rising part of the shaped voltage, where its derivative dv/dt and therefore the current in the compensation capacitance C_c are the highest. The exponential nature of the bipolar transistor could cause pulse shape distortion. A way of evaluating this change in shape versus the input charge is to study the variation of the P_{k-1}/P_k ratio. In theory, this ratio should remain constant over the whole dynamic. Detailed calculations showed that 1% change of this ratio adds 0.5 ns to the reconstructed timing error and 0.2% to 0.5% to the summed non linearity error, which remains acceptable in our case. Care has been taken in the design of the preamplifier input stage. A metal resistor is inserted between the emitter of Q_1 and Q_2. Simulation indicates that the variation of the P_{k-1}/P_k ratio is closed to 1% when the transconductance gm of Q_1 and Q_2 is seven times more than $1/R_1$.

Monte Carlo simulations have been performed on the preamplifier. A set of 50 iterations, reflecting the lot to lot process variations along with on chip mismatches, was done on the peaking time spread. The Figure 3 shows the results obtained. As a result, a 10 ns peaking time spread is observed between lots and chips will be sorted during production. In addition, the peaking time is correlated only to the absolute value of R_1.

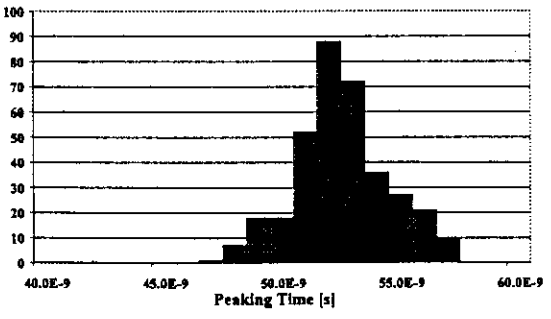

Figure 3: Peaking time spread (Monte-Carlo simulation).

The gain stages, connected directly in parallel to the output of the preamplifier, consist of closed loop current feedback amplifiers [5] followed by simple RC filters, with a time constant much lower than the preamplifier shaping time constant. Each amplifier has a clamping circuit to prevent saturation and long recovering time for high level signals. The gains are fixed by the ratios of internal matched metal resistors

which have low thermal coefficients and are radiation resistant.

In normal operation, analog sampled data provided to the ADC could belong to different ranges, depending on the input charge, coming from the photodetector. Therefore, the bandwidths of gain stages have to be close to each other in order to have a P_{k-1}/P_k ratio variation much lower than 1% when reconstructing the signal. The design strategy used to overcome this problem is to have a high closed loop bandwidth (250 MHz) for the amplifiers followed by matched RC filters which have a typical bandwidth of 30 MHz. Simulation indicates that the bandwidth mismatch between ranges has to be lower than 3% in order to have a P_{k1}/P_k ratio variation lower than 1%. Matching data on passive components, provided by the foundry are much better than our needs.

B. Sample/Hold and Multiplexer Stages.

The schematic of the switch used in sample/hold and multiplexer stages is shown in Figure 4. In order to benefit from the high performance of NPN and PNP transistor, a symmetrical switched emitter follower architecture was employed to realize both functions. Digital controlled differential pairs turn on and off unity gain emitter followers, every 25 ns. A non-linearity of 2.6 10^{-5}% is achieved for signal swing equals to power supply rails minus 5V. In addition, clamping transistors were incorporated to improve speed.

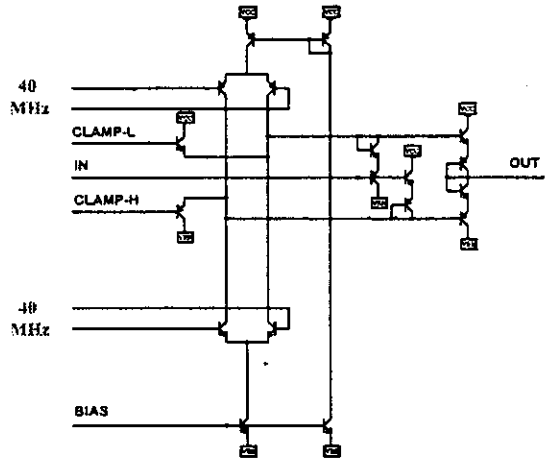

Figure 4: Sample/Hold and multiplexer schematic.

Monte Carlo simulation has been performed to determine the integral non linearity spread of the S/H stage. The results obtained are shown in Figure 5. As the 12 bit ADC, connected at the output of the chip, requires a 1V swing within a 1.9-2.9 voltage range and is DC coupled, an on-chip buffer following the multiplexer stage, was designed. In order to preserve the signal integrity, the output buffer achieve a non-linearity of 0.1%, as well as a bandwidth of 300 MHz, and an output noise of 50 µV rms. Moreover, a division by two function and a 2mA sinking capability in quiescent condition is necessary to convert the 2V to 1V signal swing and to drive the ADC load.

DC voltage shift and division by two is accomplished by three identical current feedback amplifiers and metal resistor bridge.

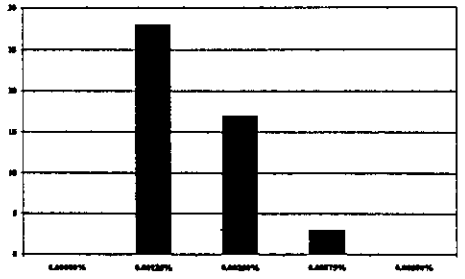

Figure 5: Distribution of the integral non linearity of S/H stage.

C. Temperature and Leakage Current Readout Blocks.

Irradiation and temperature produce an increase of APDs leakage current up to 10 µA after 2 MRad and with a temperature sensitivity of 10%/°C at 18°C and must be monitored by a specific readout chain. The simplified schematic is depicted in Figure 6.

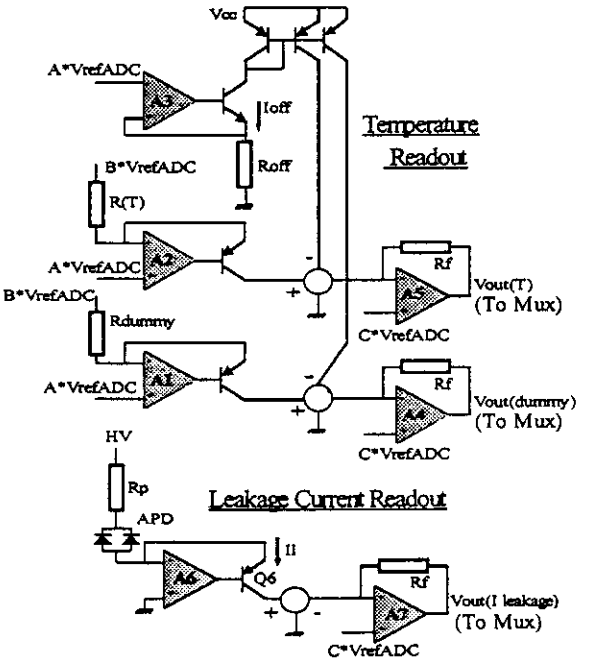

Figure 6: Simplified schematic of the temperature and leakage current readout chain.

1) Leakage Current Readout.

The circuit consists of two operational tansconductance amplifiers (OTA). A6 convey the leakage current I_l through transistor Q_6 and stabilizes the APD anode voltage to ground. After inverting I_l with a current mirror, the second OTA A7 operates as a transimpedance amplifier. It converts the leakage current into a voltage. Output voltage increases from C^*V_{refADC} to 2.5V as soon as leakage current increases. The full scale input current is 20 µA and the precision is 1%. These two OTAs are low input bias current and are also used for the

temperature readout. Monte Carlo simulation over 50 iterations gives an absolute anode voltage between −10 mV and 8 mV and 1% of integral non-linearity.

2) Temperature Readout.

For measuring the APD and crystal temperature, a discrete negative temperature coefficient thermistor is used. One must detect a variation of 0.1°C over a range of 20°C. The current through the thermistor is first monitored by the OTA A2, inverted and then referenced to the current corresponding to 5°C (I_{off}), generated by A3 and R_{off}. A current to voltage conversion using the OTA A5 as a transimpedance amplifier. The output voltage is given by the following expression:

$$V_{out}(T) = V_{refADC}\left[\frac{R_f}{R(T)}B + C - R_f A\left(\frac{1}{R_{off}} + \frac{1}{R(T)}\right)\right] \quad (2)$$

Digital code N after an analog to digital conversion over n=12 bits becomes:

$$N = 2^n\left[\frac{R_f}{R(T)}B + C - R_f A\left(\frac{1}{R_{off}} + \frac{1}{R(T)}\right)\right] \quad (3)$$

This expression indicates that the digital value is independent of the ADC voltage reference. A dummy channel connected to an internal metal resistor was also implemented to be able to distinguish if an output voltage variation comes from a change of temperature or from irradiation effect on the readout chain. Monte Carlo simulation gives less than 0.12% of integral non linearity. Under irradiation, the base current of bipolar transistors increase while the collector current remain constant. This effect is more important for small collector current. Therefore, a specific symmetrical OTA with compensated input bias current was used [6].

IV. Chip Layout.

The layout of the chip is shown in Figure 7. Care was taken during the floorplan design phase because of the mixed mode nature of this circuit.

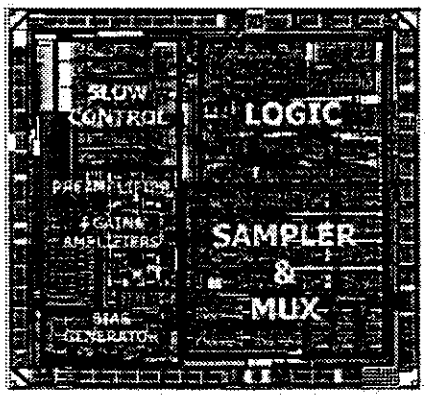

Figure 7: Chip layout.

Sensitive analog parts and digital block are individually surrounded by a dielectric trench for reducing crosstalk. The core cell is surrounded by bond pads protected against electrostatic discharges (ESD). On chip transient clamps prevent ESD damages on analog and digital supplies lines. For preamplifier and APD leakage current inputs, which are very sensitive to noise and diode leakage current, a special ESD protection scheme was used. The die area is 25 mm^2.

V. Experimental Results.

Prototypes were extensively tested in lab and under 64 MeV protons beam irradiations. The test setup used consists of a Tektronix CSA803C signal analyzer, a Picopulse high dynamic range pulse generator along with a dedicated test board with independent digital and analog supplies. Some experimental results are presented. The Figure 8 shows the output analog sampled signal in normal mode superimposed with the output signal in track mode (S/H circuit in sample mode) corresponding to a 1 pC input charge.

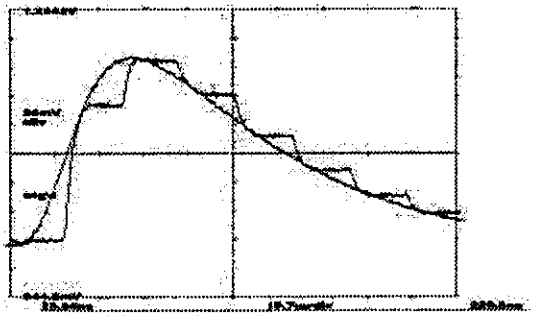

Figure 8: Output signal for 1pC input charge.

An Integral non linearity of 0.15% ±0.05% was measured at the output of the circuit, running at 40 MHz, on the four samples around the peak. Figure 9 shows the output in automatic mode for an input charge of 4.5 pC. The circuit change from range 33 to range 9 and then to range 33. A switching time between ranges of 9 ns has been measured.

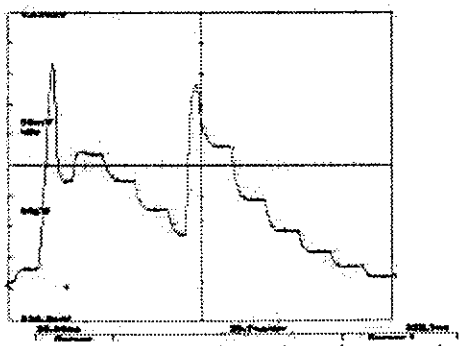

Figure 9: Output signal for 4.5 pC input charge in automatic mode.

An equivalent noise charge of 10500 electrons was measured on range 33, with a source capacitance of 200 pF and 40 MHz clocks applied on the circuit.

Dynamic measurements were performed on circuits under 64 MeV proton irradiation. A total dose of 10^{13} protons/cm^2 was applied. A change of preamplifier gain of 0.3% was observed while no change in shape, by measuring the P_{k-1}/P_k ratio, occurs.

Mass production of 80000 working chips implies automated tests. Static and dynamic tests performed on chips has been foreseen. In order to determine which parameters are

relevant and have to be measured during mass production, a test workbench is being designed. This system uses a DSP and allows a wide amount of tests to be performed. A PC computer connected to it stores the data to be processed and sorted afterwards.

VI. CONCLUSION.

The design goal of integrating a linear switched multi range transimpedance amplifier which can perform a 12 bit precision signal operation and covering 92 dB of dynamic range has been achieved. Crucial key parameters as constant bandwidth between ranges, noise, precision, speed were studied to obtain a reliable design. Experimental tests performed in lab and under irradiation assess the performance of the circuit. This chip will equip the barrel and the endcap part of the CMS electromagnetic calorimeter, by changing the metal mask while keeping the same silicon front-end. A 4'' wafer run is now being processed and mass production will start next year.

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