DESIGN AND IMPLEMENTATION OF THE HIGH PERFORMANCE THYRATRON DRIVER*

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Abstract

To meet high performance injection requirment, the extraction and injection kicker of the booster synchrotron of SRRC must be working in accordance with the injection frequency. If the operating timing of the extraction and injection kicker deviates too much from the booster master timing clock, the injection efficiency will be deteriorated. To prevent this situation to occur, the jitter of thyration driver of extraction and injection kicker related to that of the master timing clock must be small than +/- 1ns. A new thyration driver was designed using high performance Power MOSFET. The new thyration driver is capable of producing very small phase jitter and fast rise time. Results and measured performance will be presented in this paper.

1 INTRODUCTION

Thyratron is a switching device which can with stands very high voltage (tens of kilo Volts) did conducts high current (several hundred Amperes). To achieve this high-voltage, high current switching capability, a robust Thyratron Driver is required. The performance of the Thyratron driver has great influence on the Thyratron tube's switching characteristics and its lifetime. Three major driver features will strongly effect the switching performance. They are (1) Trigger Jitter (2) Trigger output delay time (3) Trigger rise time. In this paper a novel Thyratron driver topology is proposed and fabricated for daily operation. The driver circuit not only exhibits smaller trigger jitter but also reducedtrigger output delay time. This Thyratron driver has been installed in the injection and Extraction Kicker of the Booster Ring at SRRC. But also is proven to be very robust over time.

2 DESIGN PRINCIPLE

The major requirement of the Thratron driver is to deliver high quality trigger pulsed with adequate voltage and current to turn on the Thyration tube. To meet these requirements, selection of fast switching Power MosFET with small C_{iss} and Q_g (the gate input capacitor of MosFET) Characteristics and Power MosFET drivers are the two most important factors. With careful design the Thyratron driver would meet the specification of trigger output pulse's rise time less than 30ns and jitter be less than +/- 1nS.

The smaller the C_{iss} and Q_g the faster the turn on and off time of the Power MosFET and hence a sharper trigger output pulse rise time can be largely reduced by increasing the output current driver capability of the Power MosFET driver. Except the rise-time and jitter issue, trigger input and output signal isolation is also important factor to be considered in this design.

High-speed opto-isolator is employed to prove necessary isolation between the TTL -level input trigger signal from the control unit and the high voltage signal. So that these two sub-circuit systems will not interact with each other and hence improve the jitter performance of trigger output.

Because of the fast rise time of the trigger pulse, oscillation of the might occur due to the parasitic capacitance and inductance in the circuit. To overcome this, RDC snubber circuit was deployed in the Poewer MosFET output stage.

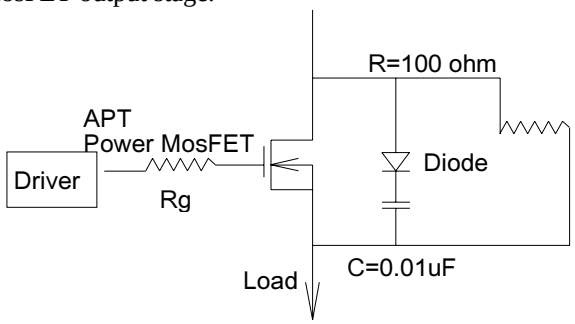

Figure 1. The Snubber circuit of the SRRC-1000.

3 TESTING AND RESULT

After finishing the overall circuit design the SRRC-1000 prototype was built and installed into booster ring's extraction kicker system to measure its output performance.

The trigger output waveform of the extraction kicker with SRRC-1000 as trigger driver is in figure 2, figure 3. They Show the zoom-in view of portion of rising pulse to demonstrate the rise time of the trigger output. It can be calculated from figure 3 that the rise time is

$$\text{Calculated Rise Time} = \frac{287V}{19.7ns} = 14.56\text{V/ns}$$

Important Data of SRRC-1000 are listed below:

1. Optocoupler Delay Time: 50ns
2. Driver Delay Time: 35ns
3. Total Delay Time: 130ns
4. High Voltage Rise Time: 84ns
5. Jitter: ±0.2ns
6. Driver Peak Current: 18 Amp

SRRC-1000 Working in Extraction Kicker

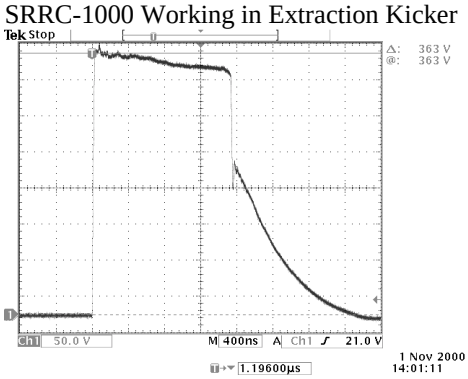

Figure 2: Output Voltage Waveform (On Line Loading).

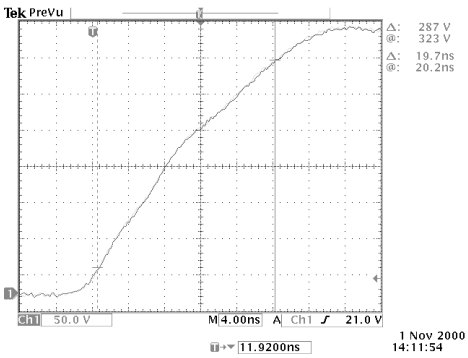

Figure 3: Output Voltage Rise Time: 19.7ns (On Line Loading).

The rise time and slew rate of the output waveform the SRRC-1000 driver to the Thyratron Grid 2 Gate is shown in Figure 4. Figure5 illustrates the jitter performance of SRRC-1000 Trigger output pulse.

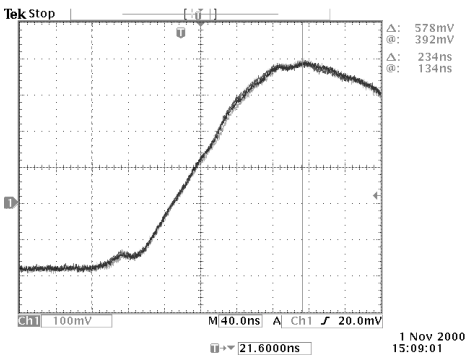

Figure 4: Thyratron Grid 2 Input Voltage Rise Time: 578V/234ns.
SRRC-1000 (Scale: 1V=1000V).

The measured jitter is about +/-0.2nS, which is far less than the +/-1nS specification.

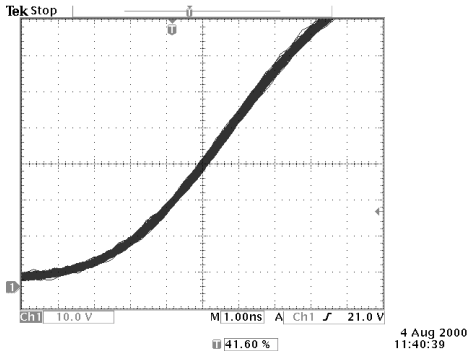

Figure 5: The jitter of the Output waveform, Rg = 1.67 ohm Jitter: ±0.2ns.

The SRRC-1000 driver board and the assembly of the final driver system are illustrated in Figure 6 to Figure 8 respectively.

Figure 6: SRRC-1000 Circuit Board.

Figure 7: Internal arrangement of SRRC-1000 System.

Figure 8: Picture of SRRC-1000 Thyrotron trigger system.

4. CONCLUSION

In this paper, a rigid Thyratron driver circuit is developed and deployed in daily operation. The SRRC-1000 driver boards have been fully tested and proven to be successful in supplying the adequate trigger pules, which are used to drive the Thyratron tubes both injection and extraction kicker system in the booster ring at SRRC.

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