HIGH SPEED DIGITAL SIGNAL PROCESSING ELECTRONICS FOR THE TLS LONGITUDINAL FEEDBACK SYSTEM

M. S. Yeh, K. T. Hsu, C. H. Kuo, W. K. Lau, J. F. Lee, H. J. Tsai, SRRC, Hsinchu, Taiwan

Abstract

A high-speed digital signal processing system is being built for feedback control of bunch phase in the TLS storage ring. It consists of (1) an analog-to-digital converter plus demultiplexer (ADC/DEMUX) unit (2) a digital filters (DIFI) array and (3) a digital-to-analog converter plus multiplexer (DAC/MUX) unit. The ADC/DEMUX unit has a fast ADC that digitizes the discrete signal of bunch phases. The data are then down-sampled and distributed to the slower DSP chips in the DIFI array via communication ports. The DIFI array performs digital filtering such that phase error of each bunch is extracted. In the DAC/MUX, processed data from DIFI array are collected and organized in a proper sequence (there is a buffer that hold the output data for number of turns if higher loop gain is required). This stream of data is then converted back to analog signal for bunch phase correction. Design and construction issues of this system are reported.

1 INTRODUCTION

A bunch-by-bunch longitudinal feedback system based on parallel digital signal processing techniques is being built for TLS storage ring. One of the technological challenges is to implement a high-speed digital signal processing system at a peak data processing rate of 500 MB/s. It performs simple but fast digital filtering for extraction of phase error information from each of the 200 bunches. With these data, an adequate correction signal is constructed for feedback. This system consists of three parts. They are the ADC/DEMUX unit, the DIFI array and the DAC/MUX unit. The ADC/DEMUX unit has a 500 MHz 8-bits ADC that digitizes the discrete signal of bunch phases. The data are then down-sampled by a factor of 18 and distributed via communication ports to 60 MHz C44 processors that run at a lower speed. The DIFI array performs simple but fast digital filtering (e.g. n-taps FIR filters) such that phase errors of each bunch are extracted. In the DAC/MUX, processed data from DIFI array are collected and organized at right sequence This stream of data is then converted back to analog signal by a 12 bits fast DAC for bunch phase correction. Section 2 describes the ADC/DEMUX unit that has been built and tested successfully. Section 4 describes the evaluation test of using C44 as processing elements in the DIFI array. It has been discussed that whether one should includes hold buffers in the DAC/MUX unit. Section 3 describes a modified version of DAC/MUX having hold-buffers for loop gain enhancement. A summary of recent progress and possibility of using processing elements other than DSP chips are discussed in the last section.

2 THE ADC/DEMUX UNIT

This ADC/DEMUX unit digitizes, down-samples and distributes the discrete signal of bunch phases. Recently, this unit has already been fabricated and tested (Figure 1). Some preliminary beam observations have been performed with it [1].

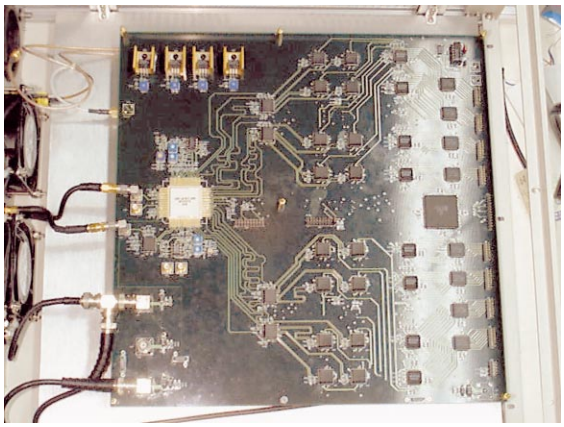

Figure 1: The ADC/DEMUX unit has been built and tested successfully

2.1 Fast ADC

The ADC we employed is the 500 Msps 8-bits MAX101A produced by MAXIM. It has two 250 MHz ECL signal outputs that are 180° out of phase.

2.2 Demultiplexer

Each channel of the 250 MHz ECL output from MAX101A is then demultiplexed into four channels by using the MC100E445 serial to parallel converter. To each channel, data rate is therefore slowed down by a factor of four (i.e. 62.5 Mbytes/s). To keep the demultiplexed ECL signal from each channels in synchronous with each other. Propagation delays have to be carefully controlled during circuit board layout. Data in ECL logic are converted into TTL logic before they are stored in first-in-first (FIFO) memories.

2.3 Down-Sampling and Interface Control

Down sampling and data transfer from FIFO memories to the C44 processors via communication ports are control by a single CPLD chip which is programmed in house. It takes the advantage of in-system-programmability that

control logic may change from time to time during prototyping. For example, down-sampling factor can easily be changed without changing the layout of the circuit. Note that the down sampling factor was set at 18.

2.4 Circuit Board Layout and Fabrications

The work of PCB layout is complicated by the mixed signals running at high speed require impedance control, skew control and avoid cross talks between signals. There are the four signal layers and eight power/ground layers so that interference between layers can be avoided.

3 THE DAC/MUX UNIT

The multiplexer in the DAC/MUX unit receives data from the C44 processors (also via communication ports) that represent filtered phase errors and reorganize in a proper sequence. And they are converted back to analog signal by a fast DAC and send to the modulator of the 1.0-1.25 GHz rf system. Hold buffers are also implemented to allow repeated kicks for higher loop gain. Figure 2 shows a functional block diagram of this unit. PCB layout of this unit is in progress.

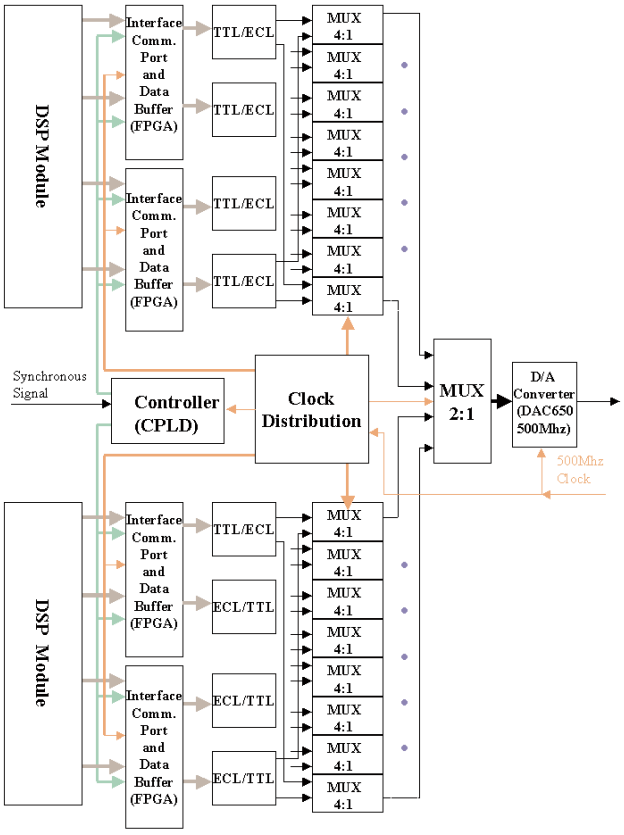

Figure 2: Functional Block Diagram of the DAC/MUX Unit

3.1 Fast DAC

The fast 12 bits DAC we used is the Burr-Brown DAC650 running at 500 MHz (only 8 bits are used). A prototype PCB was made to test the performance of this chip. The result is quite satifatory.

3.2 Multiplexer

Multiplexer is just the reverse of the demultiplexer in the ADC/DEMUX unit.

3.3 Hold Buffer and Interface Control

According to the results from feedback loop simulation [2]. It is desirable to have data buffers that allow repeated kicks for many turns. Data buffer have been implemented by field programmable gate array (FPGA). Again, interface between C44 processors and data buffer in multiplexer is controlled by CPLD.

4 THE DIFI ARRAY

The DIFI array is a system of VME DSP modules and each module has a number of DSP chips. The number of chips modules and number of chips per modules depend on the type of processors and commercial DSP modules we choose as long as the communication ports are provided for data transfer. The possible candidates of processors are chips of the TI C4X and C6X series. We reported here the evaluation test we have done with the C44 processors. The C6201 processor is another possibility and is under studied. The software structure of the system consist of a algorithm for DIFI and to provide raw data for beam diagnostic purposes and is reported elsewhere [3].

4.1 Evaluation Test with C44 Processor

Using C44 processors in the DIFI array is being tested. Data transfer between individual C44 and external circuits via communication ports are satisfactory. The processing speed per modules depends on both the hardware and software architecture of the module. Global on-board memory is essential.

4.2 Possibility of using the C6201Processor

Rapid development in DSP technology provides a wide range in processor selection. Modules with high speed C6201 fixed point processor are now commercially available. The use of these processors in the system allows a sophisticated controller design for better feedback loop performance. Possibility of the option is under consideration.

5 DISCUSSION

The unique design of the ADC/DEMUX and DAC/MUX units provides flexibility in choosing commercially available DSP modules provided that the communication ports exist. This capability is ideal for system upgrade to a more sophisticated controller design. The ADC/DEMUX unit has been built and tested. DAC/MUX unit is being built and will be tested in the near future. Possibility of using FPGA as processing elements is in the list of further studies.

6 REFERENCES

[1] W. K. Lau et al, "Progress of the Longitudinal Feedback System and Associated Beam Observations in TLS", these proceedings.
[2] W. K. Lau et al., "Analysis of the TLS Longitudinal Feedback System" these proceedings
[3] C. H. Kuo et al., " Integrated Software Environment of Longitudinal Feedback System for TLS" these proceedings.