

A DIGITAL QUENCH DETECTION SYSTEM FOR SUPERCONDUCTING MAGNETS*

D.F. Orris⁺, S. Feher, M.J. Lamm, J. Nogiec, S. Sharonov, M. Tartaglia, J. Tompkins, FNAL, Batavia, IL

Abstract

A system has been developed for digitally detecting superconducting magnet quenches in real time. This system has been fully tested and is completely integrated into a Vertical Magnet Test Facility (VMTF)[1] at FNAL. The digital technique used for this system relies on the application of digital signal processing (DSP) algorithms running on a native Motorola PowerPC VME processor. The performance of this digital system has been shown to be superior to the analog technology typically used for quench detection; *i.e.*, it detects resistive voltages reliably at low thresholds with minimum delay and is a more flexible system.

1 INTRODUCTION

The quench management system for VMTF has two primary components: The quench logic hardware, and the quench detection system. The quench logic hardware controls the power supplies, the dump, and the heater power supplies, while the quench detection system provides the quench trigger event for initiating the magnet protection and data logging sequences.

A digital quench detection system was developed for this purpose. Multiple quench threshold values can be set for special purpose triggers, the channel configuration is programmable, it can perform digital balancing, and is controlled through a GUI. The system design will be discussed, followed by the methods of filter design, system optimization, and software operation.

2 DIGITAL QUENCH DETECTION SYSTEM DESIGN

A number of analog voltage tap signals from the magnet are converted to digital signals by passing them through an anti-aliasing filter before conversion by an ADC, which are then are digitally processed by the CPU. These modules reside together along with the other quench management hardware in the same VME crate for fast communication.

The important parameters for the real time digital quench detection (DQD) system design include the CPU load, the ADC performance specifications, the anti-aliasing filter response, and the digital filter specifications.

2.1 The ADC Specifications

The ADC used for this system is a 16-Bit, 8-channel (expandable to 256 channels), successive approximation device with built-in sample-and-hold. Each channel has a differential input with a range of $\pm 10V$. The input amplifiers are instrumentation quality with four programmable gains for each channel. The maximum aggregate conversion rate is 409.6 kHz.

A VxWorks driver was written for this ADC in order to provide a means for streaming the data to the processor. The method of streaming the data to the VME processor was optimized in order to reduce the CPU load associated with filtering. Flexible control over sampling, decimating, and filtering was provided.

2.2 Anti-Aliasing Filter Parameters

Since the ADC chosen for this system is a sample-and-hold device, an anti-aliasing input filter was necessary. An 8-Channel, 5th-order, zero-error, Bessel filter was built for this purpose. The chosen cut-off frequency was 1KHz, and the noise rejection in the stop band was measured at 60dB, though the critical folding frequency actually occurs at $\sim 9KHz$ (see Fig. 1).

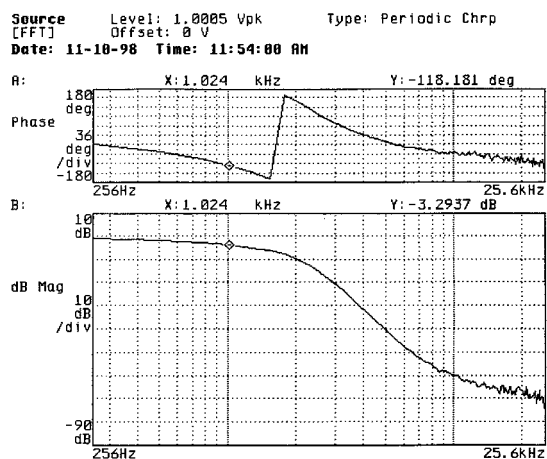


Figure 1: Bessel Filter Test Results

A primary concern in the design of this system was to minimize the total group delay of the signals used for

* Work supported by the United States Department of Energy

⁺ orris@fnal.gov

making the digital quench decision. A larger group delay will result in a longer delay of the event that causes the power supply to ramp down after a quench. The net effect of this delay will be to increase the probability of damaging the magnet under test due to high voltage to ground, or from excess ohmic heating.

Since eight separate Bessel filters were implemented, one for each ADC input channel, the cut-off frequency was chosen high enough so that filter matching was not an issue and the group delay is kept to a minimum. The group delay of these filters was measured at 0.23msec.

2.3 FIR Filter Design Requirements

The dominant source of noise across the magnet coil is generated by the power supply. It can be seen from Fig. 2 that 720Hz is the primary noise component measured in the VMTF system, though there are several other nontrivial components as well.

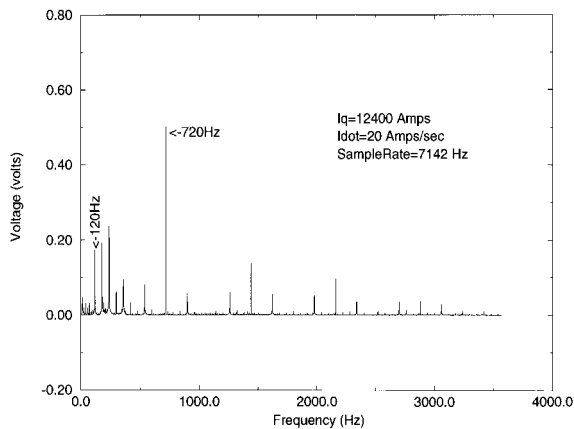


Figure 2: FFT of the Unfiltered Whole Coil Signal

There are two particular concerns with 720Hz noise: One, this frequency is not attenuated much by the Bessel filter; and two, residual bucked noise can occur due to small phase differences between two bucked channels.

Since 720Hz should be the only noise component produced by the power supply, action should be taken to attenuate it. The presence of any other noise should be removed at the source.

A digital filter with a cut-off frequency low enough to provide adequate 720Hz attenuation was implemented. Since the same digital filter would process all eight ADC signals, all group delays would be exactly matched.

A FIR filter was implemented for this reason. An IIR filter was considered because the group delay can be very small. However, the inherent stability of the FIR filter made it more attractive -- a spike produced on a coil due to the discharge of a strip heater could produce a false quench trigger if the filter was to become unstable.

The requirements of the FIR filter include the following: One, attenuate 720Hz as much as possible; two,

keep the number of taps to a minimum; and three, minimize gain error and overshoot.

2.4 FIR Filter Performance Characteristics

The FIR filter taps were determined using the Parks-McClellan algorithm. The desired sample rate was from 12KHz to 18KHz, so in order to keep the total group delay down to ~ 1ms, forty taps or less was required.

Optimal design parameters were determined after successive tests on the filter using a step response. The design band edges used were from 0.0 to 0.0082189 and from 0.049565 to 0.5. The Band Gains were, Band 1 = 1.0 and Band 2 = 0.0, and the Weighting was, Pass band = 1.0 and Stop Band = 18.0. This optimisation resulted in a 40-tap FIR filter with no overshoot and a 0.0003% gain error. The attenuation in the Stop-Band region is 50dB (see Fig. 3).

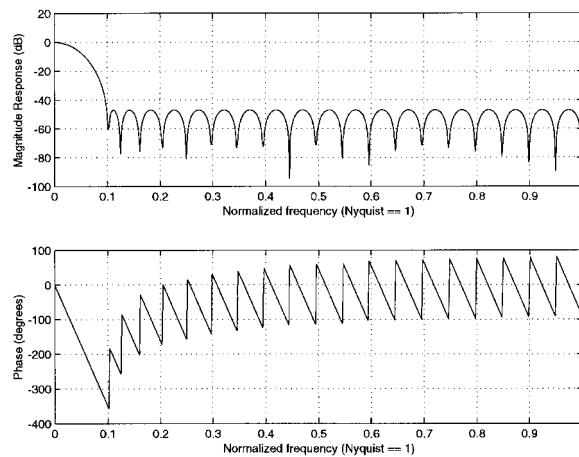


Figure 3: 40-Tap FIR Filter Response

2.5 Digital Quench Detection Processor

The processor used for this system is a Motorola PowerPC VME processor (MVME-1604-022). It is a 133MHz processor with 16Mbyte memory, and 256Kbytes of L2 cache.

This processor communicates with all the quench modules in the quench management system as well as with several other modules in our distributed processing environment. It performs the digital signal processing functions to the streamed ADC data, and it provides the quench management system with the required quench triggers. It performs filtering, digital bucking, threshold checking, trigger event generation, and balancing.

2.6 The Digital Quench Detection Program

The quench detection software was written in 'C' and runs under the VxWorks (real time) operating system. Since considerable care must be taken to guard against quench

decision delays, separate cyclic processes are run in parallel with very high priority. For example, the data is streamed from the ADC to the CPU in arrays sized to match the FIR filter tap size. The data contained in these arrays are sampled at some frequency >10KHz, but the arrays of data are sent to the CPU at some decimated frequency, which is set by the user.

The quench process also runs in parallel with a very high priority. This tight cyclic process waits for filtered data to arrive and then sends the hardware a heartbeat, which is required every 8.2msec. The quench process then performs the necessary functions leading up to a threshold decision and then returns to wait for more data from the ADC.

2.7 Digital Quench Detection Design Optimisation

Since the minimum sample rate of the ADC is dictated by the Nyquist criterion, a choice must be made for the attenuation magnitude of the alias-free dynamic range. For example, if the desired attenuation magnitude were 60dB, then its corresponding frequency of 9KHz would dictate a minimum ADC sample rate of 18KHz. A reasonable attenuation goal for this system was thought to be somewhere between 50dB to 60dB. This would dictate an ADC sample rate between 12KHz and 18KHz.

The final choice for the sample rate was 11,520Hz. Since the stop band response of the FIR filter is 50dB, there is little to be gained, with respect to the Bessel filter, from higher sample rates. Another good reason for this choice is that for this sampling rate, the second attenuation peak in the FIR filter response occurs at 720Hz (see Fig. 3), resulting in 78dB attenuation of this frequency (see Fig. 4).

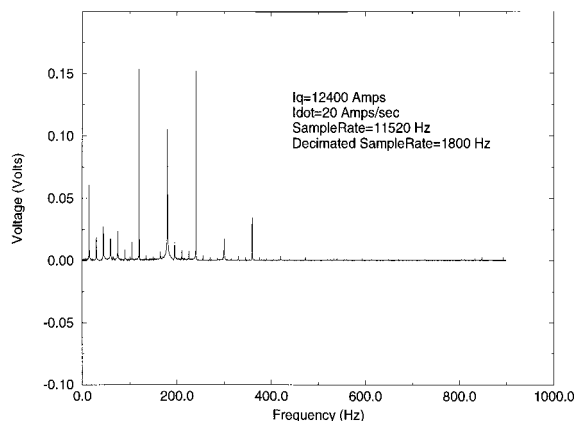


Figure 4: FFT of the Filtered Whole Coil Signal

In addition, 11,520Hz is a common multiple of 15Hz, which happens to be present in the power bus due to an external source -- the Booster Ring. Therefore, off-line filtering of 15Hz, and many of its harmonics, is made more efficient for off-line analysis.

The resulting group delay of the FIR filter associated with this sample rate is 1.6ms. Including the Bessel filter, the total group delay of the system is 1.83ms.

A decimated sample rate of 1800Hz was chosen based on the CPU load. Since the quench decision is based on this data rate, the time resolution is 0.56ms.

A typical plot of a real-time digitally detected quench is shown in Fig. 5. The peak noise spikes are ~15mV at a current of 12400Amps. This is good in comparison to the threshold setting of 300mV.

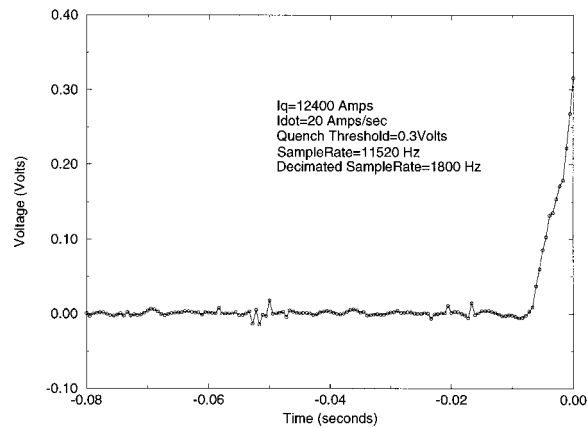


Figure 5: Real Time Quench Detect -- Bucked Half Coils

3 CONCLUSIONS

A Digital Quench Detection system was implemented using mostly commercially available components. By optimising this system to reject noise while minimising group delay, a successful method of digitally detecting quenches was accomplished.

The primary advantage to a digital quench system is its flexibility. For example, this system was easily coupled with a Software Quench Detection[2] system used to test High Temperature Superconducting Leads[3]. Also, since it is capable of generating multiple trigger events, other DAQ systems can be triggered at very low trigger thresholds for special magnet studies. This system has been in operation for two years and has an excellent performance history.

4 REFERENCES

- [1] M.J. Lamm *et al.*, "A New Facility to test Superconducting Accelerator Magnets", PAC'97, Vancouver, Canada, 1997
- [2] J.M. Nogiec *et al.*, "Architecture of HTS Leads Software Protection System", PAC'99, New York, USA, 1999
- [3] G. Citver *et al.*, "HTS Power Lead Test Results", PAC'99, New York, USA, 1999