Silicon DAQ based on FPDP and RACEway

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Abstract

DAQ for Si-detector of PHOBOS setup (RHIC) with Scalable Power for read out and Zero Suppression is described (see Fig.1). Data from VA-HDR chips with analog multiplexor, are digitized by FADC. Digital buffers are multiplexed by DMU modules at speed 100 MBytes/sec and transmitted through FPDP [1] and virtual extender of FPDP to fiber (FFI). At the receiver end (in counting house) data from fiber are distributed between a number of dedicated processors (in RACEway multiprocessor frame [2]) for Zero Suppression (ZS). After ZS data are concatenated and transmitted to Event Builder.

I. Introduction

Si detector on PHOBOS setup has about 120,000 channels. VA-HDR chips are used for analog readout. For Common Mode Noise (CMN) correction and Zero Suppression data buffers from digitization modules are transmitted to dedicated frame of processors. Expected event rate is of the order of 1 kHz, raw data size is 240 kB. For fast data transfer of unsuppressed data we are using Front Panel Data Port (ANSI/VITA-17 Standard)- synchronous data flow path that allows data to be transfered at high speed (160 Mbytes/sec) Fig.2.

FPDP cable could be connected to RINT module (input module in FPDP standard, for RACEway) directly, if distance is short. For data transfer from 2 crates filled by DMUs (Fig. 3) to the counting house we are using virtual extender of FPDP to optical link (FFI modules). The same modules sitting in RACEway crate convert data from serial format back to parallel 32 bit. Data in RACEway are handled by processors and after that zero suppressed buffers are transmitted to Event Builder.

II. Front end part

The front end part of DAQ is based on custom designed modules. Readout of VA-HDR chips and digitization is provided by FEC modules. Each FEC can digitize data from up to 6144 channels, parallel in 8 chains. FEC module sends data to DMU module by Twinax cable (about 15 m @ 25 Mbytes/sec) using G-link serial connection. FEC and DMU modules are connected by slow flat cable for control. DMU has FIFO for data and fast FPDP interface. After receiving data from FECs, DMUs are requested in sequential multiplexing mode for data transfer from the FIFO to common "bus" - FPDP cable. MDC module (Fig. 4) provides muster function in a crate filled by DMU modules. It also checks the length and parity of individual buffer and add the status information at the end of each buffer. Data from 2 crates sitting near the setup are converted from FPDP to serial optical link (G-link) format and back, by custom FFI modules . They are working at 100 Mbytes/sec speed. On Fig. 5 timing for ZS system with 2 optical links and 10 PPCs is shown.

III. RACEway real - time multicomputer

To handle a lot of data in real-time we are using scalable RACEway architecture in VME. RACEway is an ANSI/VITA standard for high performance switched communication in real-time systems. The RACE Series real time multicmputers provide from two to thousands of integrated compute nodes. RACE systems implement the RACEway real-time system interconnect. RACEway Interlink provides fast (up to 160 Mbytes/sec) point to point interconnection. The RACEway interconnect and RACE compute nodes form the building blocks of RACE computer systems. Each node is a compact computer with a processor, memory, and a RACEway network interface that delivers computational performance previously available only from supercomputers.

We have number of motherboards with I/O and PPC-750 processors. Data from FFI are received by RINT input modules and then distributed between processors. Code for CMN correction and Zero Suppression is written in C. Number of processors in system could be easily changed.

IV. References

1. http://www.fpdp.com

2. http://www.mc.com

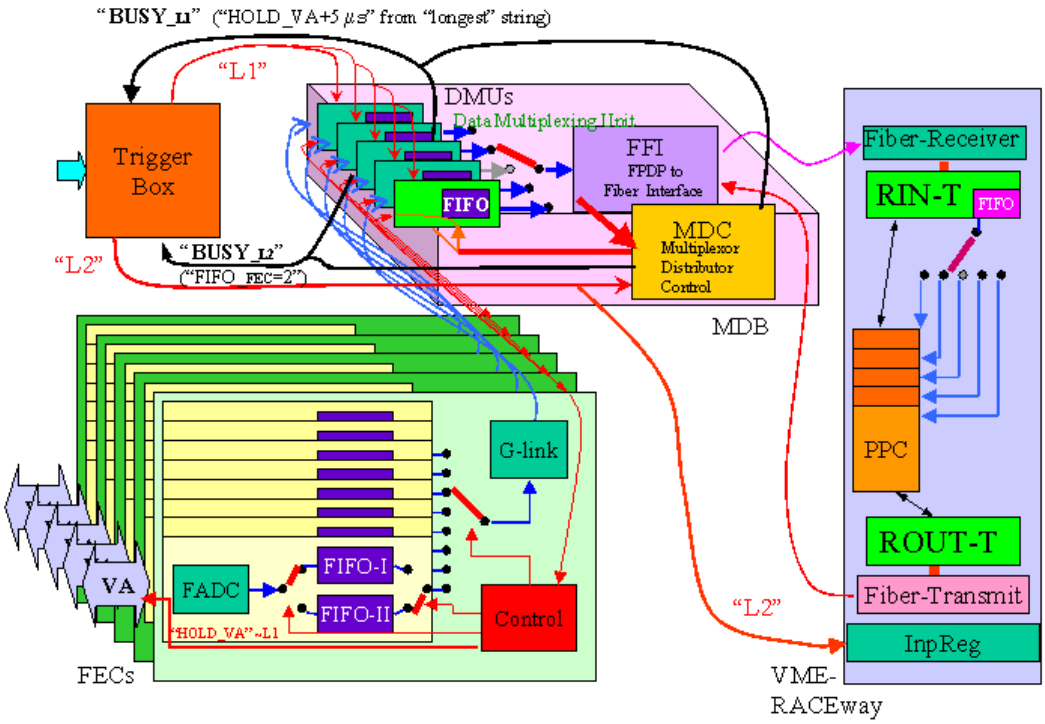

Figure 1: Block diagram of Si part of DAQ.

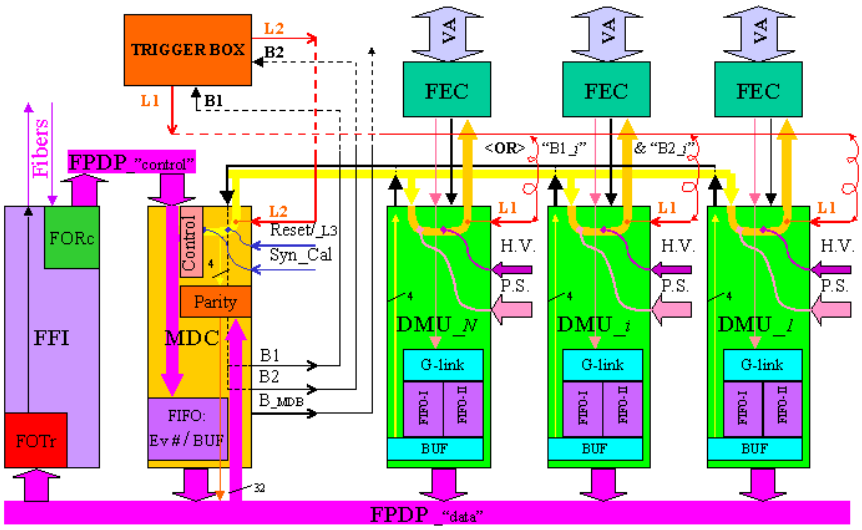

Figure 2: Two FPDP cables are used for data transfer and control.

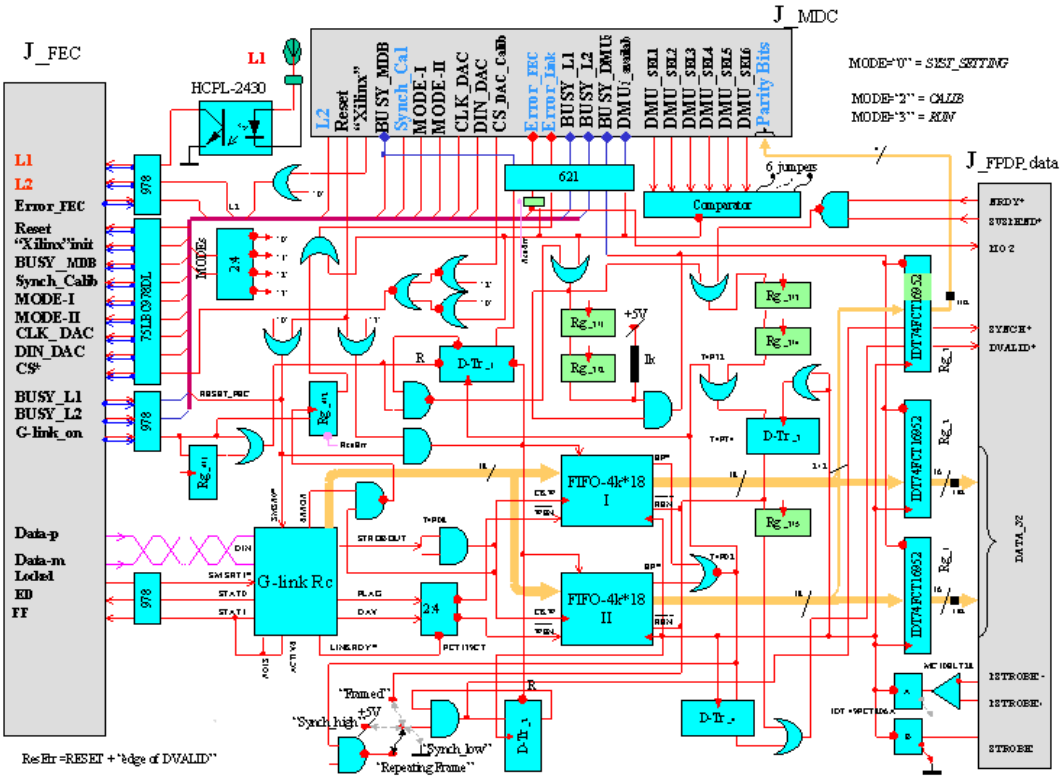

Figure 3: Functional block diagram of DMU module.

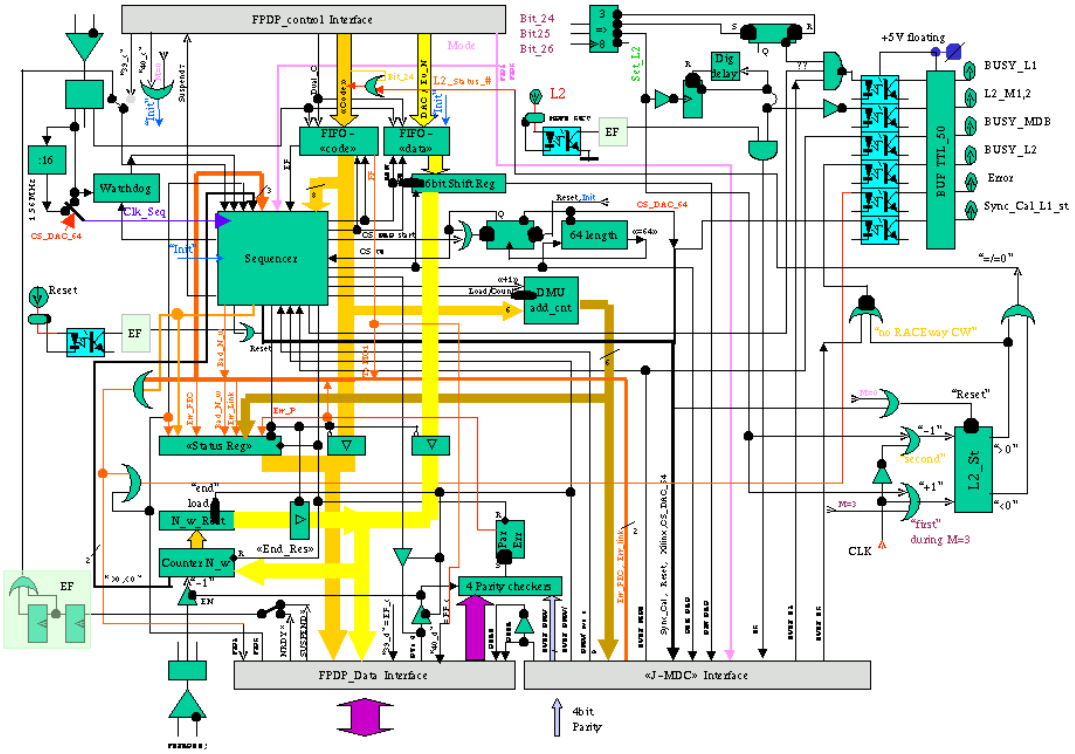

Figure 4: Block diagram of MDC module.

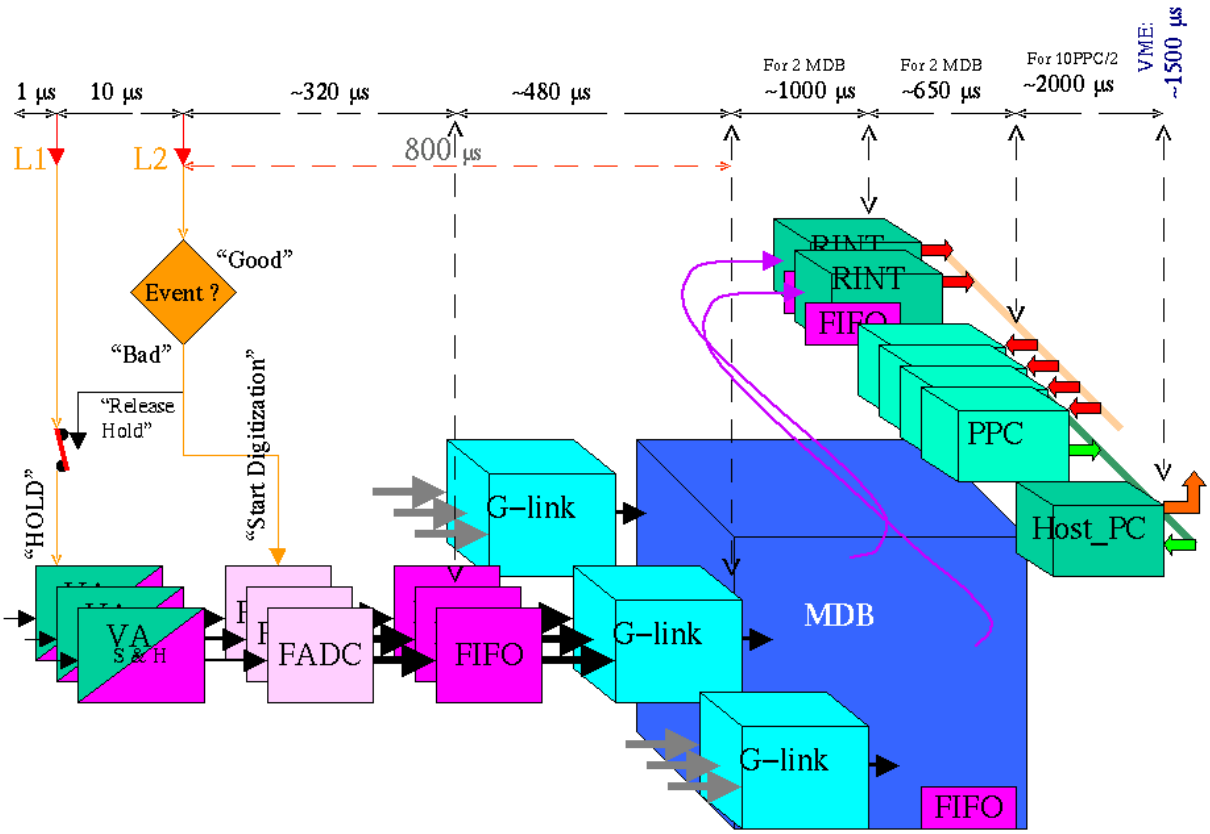

Figure 5: Timing for 60,000 channels and 10 PPCs.