The ATLAS Liquid Argon Calorimeters Read Out Drivers (ROD).

PRAST Julie, for the ATLAS Liquid Argon Collaboration.

LAPP, BP 110, Annecy le Vieux, France
Julie.prast@lapp.in2p3.fr

Abstract

The Read Out Drivers (ROD), which are described here, are part of the electronics of the ATLAS Liquid Argon Calorimeters. A ROD module receives triggered data from 256 calorimeter cells. It calculates precise energy and timing of the calorimeters signals from discrete time samples. It also performs monitoring and formats data for the next element in the electronic chain.

To assess the feasibility of the project, the ATLAS LAr collaboration has decided to make a ROD demonstrator. The project consists in the construction of a motherboard, into which can be plugged up to 4 daughterboard processing units (PU). The architecture of the PU is based around a Digital Signal Processor (DSP). Currently 3 PU have been designed, two based on an integer DSP and the other on a floating point processor.

First prototypes were produced at the beginning of the year. They show very encouraging results. However to improve performance, new prototypes with more powerful DSP, will be studied.

I. OVERALL PRESENTATION

A. *The ROD modules in the electronics chain*

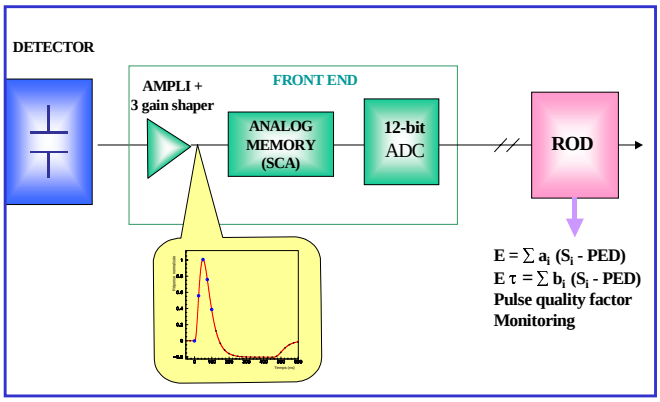

Figure 1 : The upstream electronics chain of the ATLAS Liquid Argon Calorimeter

During hadron beams collisions, produced particles create a current in the calorimeter electrodes. At the output of the detector, the signal is amplified, shaped, sampled and stored in an analog pipeline memory, waiting for the level one accept decision. Data are then digitized by a 12-bit ADC and sent on optical links towards the 800 ROD modules, where they are processed.

B. *The ROD modules goals*

A single ROD module receives data from 2 Front End Boards (FEB), consisting of typically 5 time samples from 256 channels (cf figure 1). Data arrive at the frequency of the LHC (40 MHz). Processors in the module calculate the energy E and time τ (relative to the current bunch crossing time) from the digitized samples, along with a pulse quality factor χ^2, which indicates how closely the samples follow the known waveform. These energy and time calculations are done using optimal filtering [3] [4]:

$$E = \sum a_i \, (S_i - PED)$$
$$E\,\tau = \sum b_i * (S_i - PED)$$

The pulse quality factor is a normal chi squared calculation:

$$\chi^2 = \sum ((S_i - PED) - E.\, g_i)^2$$

where S_i are the digitized samples, a_i and b_i the weights, which are channel dependant. The quantity g_i is the expected normalized waveform and PED the pedestal.

The error on the energy is amplitude independent, whereas the error on the time varies inversely with the amplitude. For this reason, it only makes sense to calculate τ for those channels with E above some threshold value. Most of the data are constituted with minimum bias events. Thus, most of the hit cells have low energy. There are very few cells for which τ, and χ^2 are calculated. Simulations show that this fraction *f* of high energy cells is around 10 %.

The ROD module processors perform also monitoring of quantities related to detector performance. To monitor the data flow, some histograms should be filled. These histograms concern quantities as parity errors, channels gain, baseline monitoring and for channels above some threshold values amplitude, time and quality of fit. For this set of histograms, a minimum memory of 130 kB is required, which corresponds to an emptying frequency of 0.2 Hz.

During calibration runs, charges of various amplitudes are injected in the electronics chain. The ROD modules compute first and second moments and send data to a local processor, which then calculates calibration constants for each channel of that module.

The ROD modules will be housed in a Readout Crate, which will be a 9U VME crate with a dedicated host processor. The ROD system will consist of about 800 modules, each of which services 256 calorimeter channels.

C. Design considerations

The maximum Level 1 trigger rate for ATLAS is 100 kHz. So, the processor must be able to treat an event in an average of 10 µs.

The processing time per event depends of the energy of the cells. There can be considerable fluctuations from event to event and some high energy event can need more than 10 µs to be processed. As a consequence, a significant amount of buffering is required to keep dead time to a minimum.

For the ROD design, our preference is to use a commercial programmable processor. A natural choice is Digital Signal Processors (DSP), because they present a very efficient calculation power for that kind of algorithm and a high I/O bandwidth.

The design of the ROD demonstrator started in the middle of 1999. The final prototype will be frozen at the end of 2001. The production is foreseen in 2002, followed by boards installation in 2004.

II. THE ROD DEMONSTRATOR

In order to demonstrate capabilities of various DSP candidates and to understand more clearly design issues, the ATLAS LAr collaboration has decided to build a ROD demonstrator. The project involves the construction of a motherboard in the 9U VME 64x format, into which can be plugged up to 4 daughterboard processing units (PU).These PU are small daughterboard (85 * 185 mm) containing one or more DSP and will be used to process calorimeter data.

Currently, 3 PU have been designed, one based on a floating point DSP (the Hammerhead 21160 from Analog Devices) and two others based on an integer DSP (the TMS 320C6202 from Texas Instrument).

A. The motherboard design

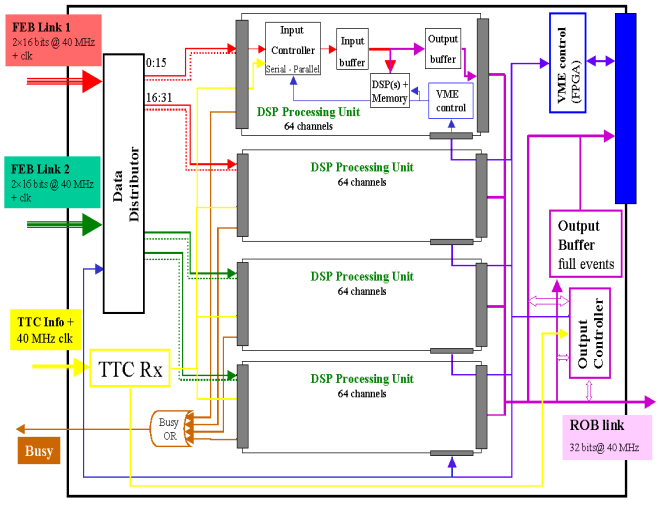

Figure 2 : The ROD demonstrator motherboard design.

Figure 2 shows the ROD demonstrator motherboard designed by the University of Geneva, Switzerland. The motherboard is a full size 9U VME module, able to carry 4 PU. It allows I/O connections with FEB and ROB (Read Out Buffer). An input is also provided for the timing and trigger information (TTC signal). The motherboard also allows the control of the PU and contains a VME interface. Through this VME interface, the CPU crate can communicate with the ROD modules. For tests purposes, the VME interface can also be used to inject and read data.

B. The Analog Devices processing unit design

1. The Analog devices PU description

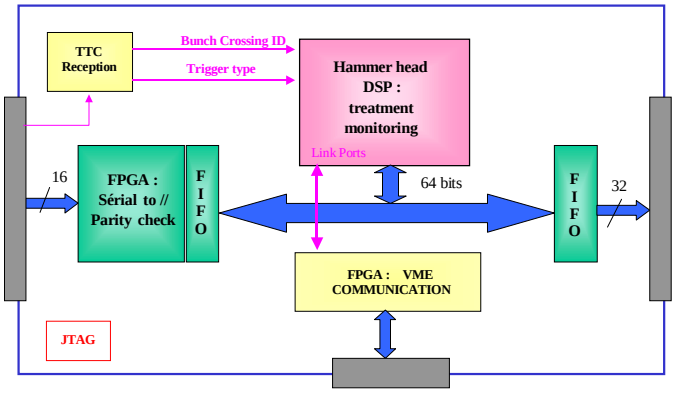

Figure 3 : The Analog Devices PU block diagram

Figure 3 shows the Analog Devices PU (PU 1) designed by the LAPP of Annecy, France. Input data (64 channels) arrive from the FEB at 40 MHz in a 16-bit series format. They enter a programmable component, which parallelizes them and looks for errors such as parity or format. The data are then sent to the DSP. The DSP is a processor specialized in signal treatment. The 100 MHz 21160 DSP was chosen, because it is nowadays the floating point processor that seems to present the best performance. For the ATLAS experiment, we count on a more powerful DSP, such as the TigerSharc from Analog Devices.

When the data are treated by the DSP, they are written into an output FIFO before being read by the motherboard. The PU also contains a VME interface, which allows the DSP boot, histogram reading and the spying of the DSP.

2. The Hammerhead DSP architecture

The Hammerhead DSP is a 32-bit fixed or floating point 100 MHz DSP. The computational unit is made of 2 processing elements (PE) that support Single Instruction Multi Data (SIMD). In this architecture, a single instruction is issued to both PE. When executing this instruction, each PE operates on different data.

Each PE includes an arithmetic and logic unit (ALU), a multiplier accumulator (MAC), a barrel shifter and 32 data registers. The ADSP 21160 has also 4 Mbit of on-chip dual-ported SRAM memory and an integrated I/O processor, which allows non intrusive DMA on six 8-bit link ports, 2 serial ports and a 64-bit external bus. Furthermore, multiple internal busses eliminate bottlenecks. Figure 4 page 5, shows the Hammerhead DSP architecture.

C. The Texas Instrument processing unit design

1. The Texas Instrument PU description

Two processing units are designed around the TMS 320C6202 250 MHz DSP from Texas Instrument. One is designed by Nevis Laboratories, Columbia University, USA (PU 2) and the other is designed by the CCPM of Marseille, France (PU 3). The architecture of these two PU is quite similar. The main difference between these two designs is that the PU 2 has a dual port memory between the input FPGA and the DSP, to buffer data.

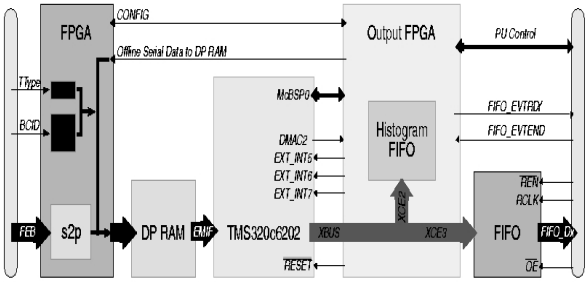

Figure 5 : Block diagram of PU 2.

Figure 5 shows the design of PU 2. The input data are reformatted and decoded into the input FPGA. They are then written into a 128 Kbytes dual port memory, before being read by the DSP. The controller FPGA is the VME interface between the PU and the motherboard. It is also used as a FIFO for histograms.

2. The Texas Instrument DSP architecture

The TMS320C6202 DSP is a fixed point 250 MHz DSP. It is based on the very-long-instruction-word (VLIW) architecture. The processor has 32 32-bit general registers and eight *independent* functional units. The eight functional units provide six 32-bit ALU and two 16-bit multipliers. The DSP also includes 1 Mbit of on-chip memory. It provides two 32-bit external buses and 3 serial ports to communicate with the peripherals. Figure 6 page 5, shows the 6202 architecture.

III. FIRST RESULTS OF THE ROD DEMONSTRATOR

A. Hardware results.

A motherboard prototype has been produced in April. It is almost completely tested and functions correctly. The three PU are now available. The PU 1 has been produced in February. As the first PU available, it was used to test the motherboard. The motherboard is currently under test with the 2 other processing units. A second version of the motherboard will be soon available and will be distributed to the participating institutions. The main difficulty for the motherboard was to handle signal reflection, since very long 40 MHz bus are used.

The hardware tests of the PU consist mainly in the verification of the input FPGA (parallelization and check of the FEB data) and the test of the whole communications of the DSP with its peripherals (input DMA, output DMA towards the output FIFO, output of the histograms to the controller of the crate, test of the VME interface, boot of the DSP, etc …).

Table1 : Summary of the ROD demonstrator results

	DSP	freq DSP	Floating point	Hardware	Software (assembly)
Mother board				Tested and working	Ready (C language)
PU 1	ADSP 21160	100 MHz	Yes	Tested and working	Complete. Under optimization
PU 2	TMS 320C 6202	250 MHz	No	Under test	E, τ, χ^2 optimized. Histo to be done
PU 3	TMS 320C 6202	250 MHz	No	Under test	Complete. Under optimization

The tested Analog Devices PU (PU 1) works correctly on the motherboard. FEB data can be injected, treated and sent to the ROB at the frequency of the LHC. No blocking hardware issues were noticed, the design withstands the event rate of 100 kHz with no loss of event. The Texas Instrument PU are currently under testing. They also show very encouraging results. Table 1 summarizes the progress of the ROD project.

One of the main hardware difficulties for the PU is the use of ball grid array (BGA) packages. The distance between 2 pins can be very small, as in the case of PU 3, where 0.8 mm BGA are used. In that case, routing and soldering steps are very delicate and need very advanced tools.

B. Software results.

Since the software of the motherboard is not time critical, it was written in C language, which allows flexibility and an easy maintenance. This is not possible for the processing units, which must treat events in less than 10 µs to meet the ATLAS bandwidth requirement. The PU DSP must be programmed in their specific assembly language.

The PU software consists mainly in the calculation of the energy E for all the channels and the calculation of τ and χ^2 for a fraction *f* of high energy cells (cf § I.B). It consists also in the management of data in memory and the elaboration of histograms. PU 1 and PU 3 software are complete and must be optimized. In the case of the PU 2, the calculation part of the software (E, τ, χ^2) is fully optimized, but histograms implementation must be done.

Table 2 : Summary of the ROD software progress for 64 channels calculation.

	PU 2	**PU 1**
E, τ, χ^2, f= 100 %	3.4 µs	-
E, τ, χ^2, f= 100 % Histo, output format	~ 2750 cycles ⇔ 11 µs	-
E, τ, χ^2, f= 10 % Histo, output format	-	~ 990 cycles ⇔ 9.9 µs.
Precision on the energy	$2^{-16} = 10^{-5}$	$5\ 10^{-6}$

Table 2 summarizes the ROD software progress. Experimental results on PU 3 are not yet available, but simulations indicate that processing times of approximately 10 µs are feasible.

In PU 2, E, τ and χ^2 are calculated for all 64 channels regardless of amplitude. That calculation is done in 3.4 µs. This is an important result, as the approach, which is different from PU 1 and PU 3, eliminates branching, which is inefficient for a DSP, is eliminated.

Since the Analog Devices Hammerhead DSP is a 100 MHz SIMD processor (cf § II.B.2), this approach is not possible, as regards to its architecture and frequency. The PU 1 can only treat a fraction *f* of 10% of high energy cells, but which is likely to be sufficient (cf § I B) and has the advantage of reducing the size of output data.

The energy calculation is very precise. The precision on the energy reaches 10^{-5} with the integer DSP and $5\ 10^{-6}$ with the floating point DSP. No precision on energy is lost in the ROD modules. The precision in the determination of both E and τ is dominated by ADC quantization, since the system of digitization consists in 12 bits ADC operating on 3 gain scales.

IV. CONCLUSION

We described the technical requirements of the Read Out Driver for the liquid argon calorimeters in ATLAS and presented the architecture of the demonstrator boards. First ROD prototypes show very encouraging results for both investigated DSPs. They demonstrate the absence of blocking issues and respect the ATLAS experiment bandwidth. They assess the feasibility of the project with currently available commercial DSPs, even if few others points must still be studied, as power consumption in the crates.

In the future, hardware tests must be finalized and the assembly DSP code must be optimized. Then, the LARG ROD final design have to be prepared. For that, more powerful DSP will be studied, such as the 150 MHz VLIW architecture floating point TigerSharc from Analog Devices or the 300 MHz fixed point TMS 320C6203 from Texas Instrument. With these new DSP and the techniques evolution, the possibility to double the system density by handling 128 channels instead of 64 in a single DSP, can be opened. Nevertheless, this option must be carefully studied, as it would imply significant changes on the hardware, as on the input FPGA of the PU or on the I/O connections of the motherboard.

V. REFERENCES

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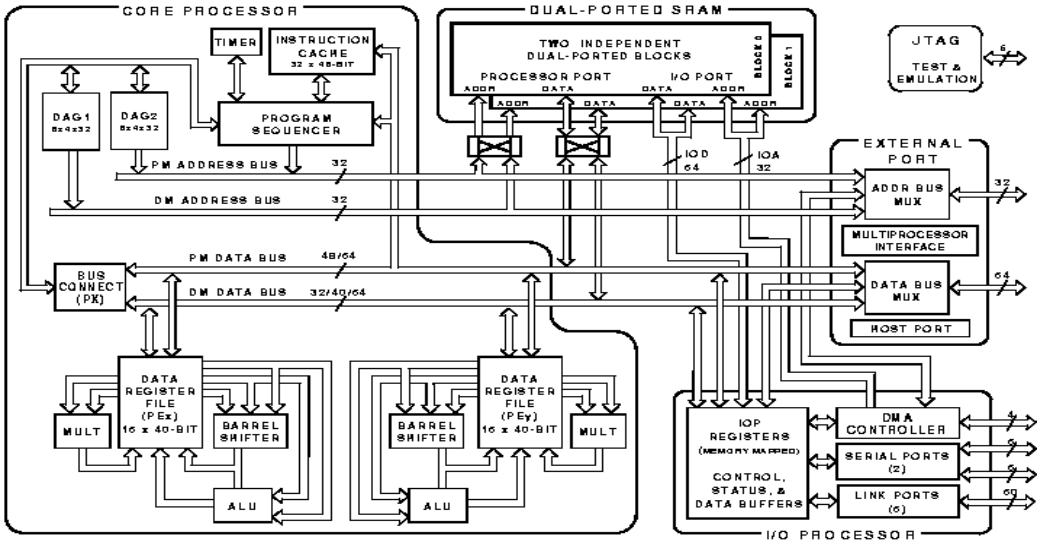

Figure 4 : The Hammerhead DSP architecture

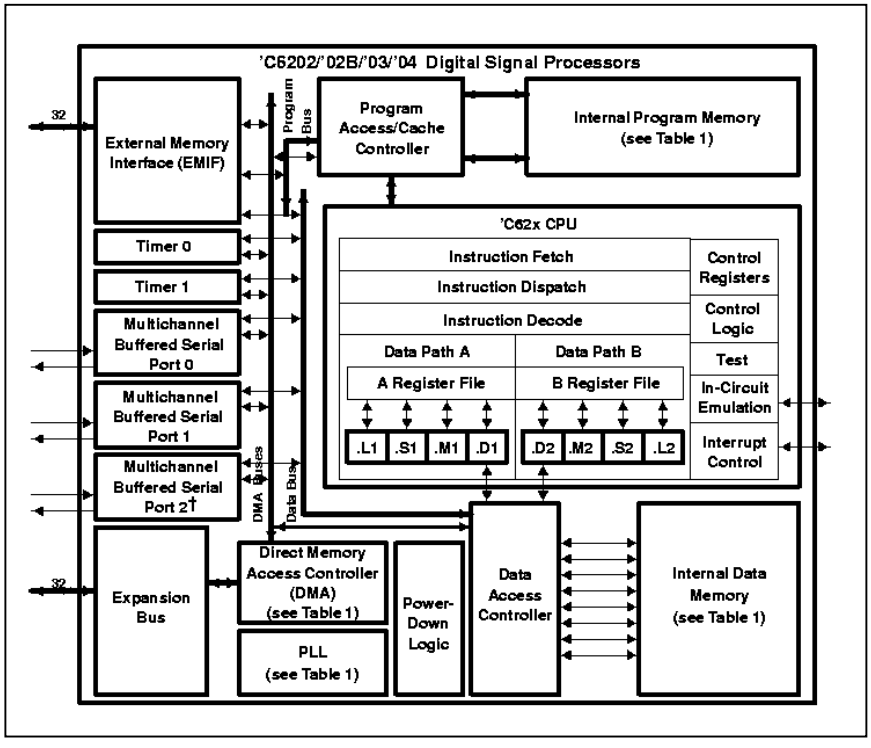

Figure 6 : The TMS 6202 DSP architecture