Performance of a 128 Channel Analogue Front-End Chip for Read-Out of Si Strip Detector Modules for LHC Experiments

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Abstract

We present a 128-channel analogue front-end chip, SCT128A-HC, for readout of silicon strip detectors employed in the inner tracking detectors of the LHC experiment. The chip is produced in the radiation hard DMILL technology. The architecture of the chip and critical design issues are discussed. The performance of the chip has been evaluated in details in the test bench and is presented in the paper. The chip is used to read out prototype analogue modules compatible in size, functionality and performance with the ATLAS SCT base line modules. Several full size detector modules equipped with SCT128A-HC chips has been built and tested successfully in the lab with β particles as well as in the test beam. The results concerning the signal-to-noise ratio, noise occupancy, efficiency and spatial resolution are presented. The radiation hardness issues are discussed.

I. INTRODUCTION

The LHC operating conditions present a very big challenge to the front-end electronics of Si trackers for experiments designed for high luminosity physics. Requirements on the front-electronics of Si strip detectors are very demanding. The readout has to be close to the Si sensor and therefore needs to be radiation hard up to doses of 10 Mrad and up to fluences of 3×10^{14} charged particles/cm^2 and 2×10^{14} neutrons/cm^2.

Due to a high occupancy expected for full luminosity operation the pulse shaping time has to be short. To avoid pile-up of events in single channels double pulse resolution has to be in the order of 50 ns. It is convenient to have a peaking time of the output pulse equivalent to the bunch crossing frequency of 40 MHz.

The noise performance is dictated by the most probable signal from a minimum ionising particle crossing a 300 μm thick Si sensor, which is 22500 charges. To obtain a good efficiency for track reconstruction and maintain at the same time a low noise occupancy a signal over noise ratio better than 15:1 is required. This is equivalent to a noise smaller than 1500 e$^-$ ENC.

The size of irreducible noise contributions, shot noise from leakage current in the irradiated Si sensor and base current in an irradiated bipolar junction transistor and preamplifier series noise, are determined by the chosen sensor element size. The sensor element size cannot be too small in order to limit the number of channels, and also cannot exceed a certain size to keep the detector capacitance low.

The three big LHC experiments, ATLAS, CMS and LHCb, which will have Si trackers, are considering detector geometries with strip length from 6 cm to 12 cm and strip pitches from 50 μm to 120 μm. The strip pitch is given by the required spatial resolution in the range of $\sigma = 5$ μm to $\sigma = 25$ μm.

In all cases data has to be stored in on-chip buffers for the duration of the level 1 trigger latency, which is around 3 μsec. This requires long pipelines with derandomising buffers. Data compression on-chip is desirable to facilitate the data transmission over optical links to the control room.

Several front-end architectures have been developed over the last 8 years for LHC experiments. Basically three different concepts have been pursued:

Full analogue readout with transmission of all data via analogue optical links to the external read-out processors for digitisation with flash ADCs. Examples for this architecture are the APV6 [1] chip and the APV-25 chip for the CMS tracker and the SCTA chip as back-up solution for the ATLAS tracker.

Analogue read-out with on-chip ADCs for each channel. This allows data sparsification on-chip and digital data transmission via digital optical links. An example is the AROW [2] chip which was developed as a possible read-out for the ATLAS Si tracker.

Binary readout architecture selects channels hit by a particle by means of a comparator in each channel. Individual thresholds on each channel allow to select hit channels by discriminating on the pulse height at the output of the shaper. A binary pipeline followed by a derandomising buffer and a data compression logic allow to transmit data only from hit channels via a digital optical link. There are two versions of binary front-ends (baseline for the ATLAS Si tracker) available. The CAFÉ-P front-end chip in bipolar technology (MAXIM process) together with the ABC pipeline chip, produced in radiation hard CMOS (Honeywell process) [3].

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Another version of this architecture, the ABCD2T chip, combines both front-end and pipeline functions on one chip produced in radiation hard BiCMOS technology (TEMIC DMILL process) [4].

Historically most collider experiments have so far used full analogue readout front-ends for Si trackers and vertex detectors. This method allows individual treatment of data in each channel with optimised and adaptable software and thereby the most detailed control and monitoring of the whole system. Analogue readout is to a large extent immune to external electromagnetic pickup (common mode) since common mode noise can be fully eliminated with simple and fast software. The price to pay for this safety is a heavier load on data transmission off the detector over optical links, both in bit rate and in the required number and quality of the links. Another advantage, at least in the case of the two options in DMILL technology developed for the ATLAS SCT, is a significantly lower power consumption of the SCT128A-HC chip compared with the ABCD2T chip [5]. The binary architecture, however, allows a more compact design and has the advantage of a much reduced data transfer rate with more chips using a single optical link.

In this paper the ATLAS back-up solution, the SCT128A-HC chip, will be described. Results from measurements of the performance of the chip will be presented. The performance of ananalogue prototype module consisting of two 6.4×6.3 cm^2 ATLAS baseline detectors read out by 6 SCT128A-HC chips, which has been tested with a Ru β-source and in a 100 GeV pion beam, will be discussed.

II. The SCT128A-HC Front-End Chip

The SCT128A-HC chip is an example of the analogue readout architecture for silicon strip detectors, which meets all basic requirements of the LHC experiments. The block diagram of the chip is shown in Fig. 1. The chip comprises five basic blocks: front-end amplifiers, analogue pipeline (ADB), control logic including the derandomizing FIFO, command decoder and output multiplexer.

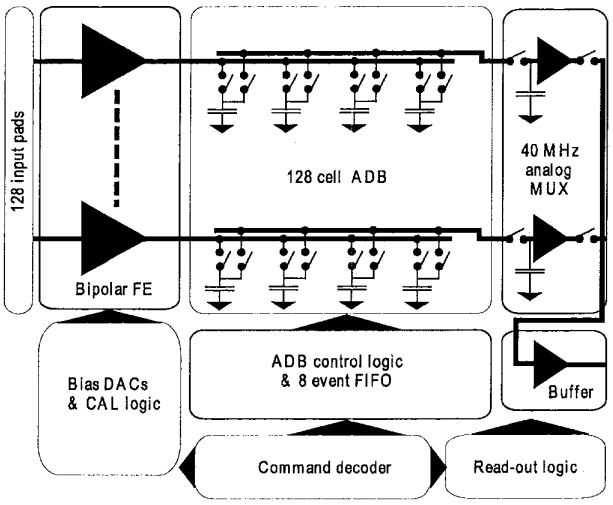

Figure 1: Block diagram of the SCTA128-HC chip.

The front-end is based on a fast transimpedance amplifier, using a bipolar input transistor, followed by an integrator providing a semi-gaussian shaping with a peaking time of 25 ns. The peak values are sampled at 40 MHz rate and stored in the 128-cell deep analogue pipeline. The derandomizing function is realised by means of an additional FIFO in which up to eight addresses of cells containing valid data can be stored. Upon receiving a trigger signal the data is read out through the fast 40 MHz analogue multiplexer.

The bias currents of the input transistor, integrator and readout amplifiers are controlled by 5-bit DACs. In order to improve the testability of the chip an internal calibration circuitry has been implemented. The circuitry allows to generate calibration pulses with the amplitudes controlled by an 8-bit DAC and the delay with respect to the clock phase controlled by an internal delay circuit. One of the four internal calibration lines can be selected by a 2-bit address. Communication with the chip is provided with the command decoder which controls all circuits mentioned above as well as the readout logic.

Fig. 2 shows the layout of the SCTA128A-HC chip. The front-end channels and the analogue pipeline are laid out with a pitch of 42 μm. Input bonding pads are laid out with 60 μm pitch. The bond pads for supply voltages and control signals are located on both sides of the chip. The die area is 7.9×8.0 mm^2 of which about 30% is occupied by the storage capacitors in the ADB.

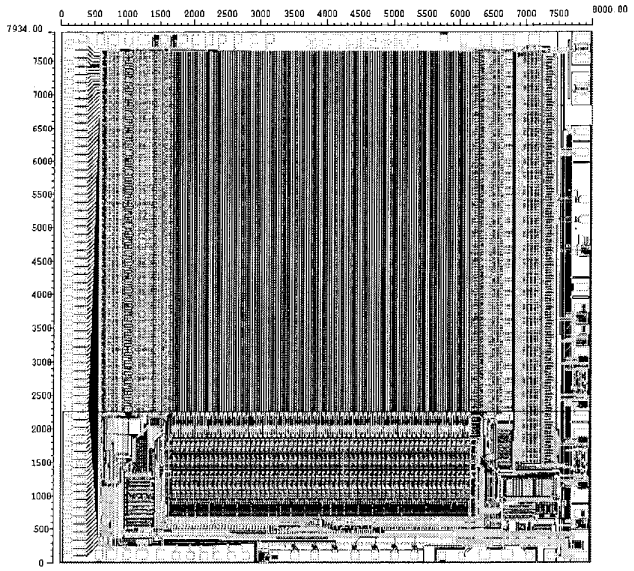

Figure 2: Layout of the SCT128A-HC chip.

A. Front-End Performance

The concept of the SCT128A-HC design is based on a fast front-end circuit providing the peaking time of 25 ns, which matches the sampling frequency of 40 MHz. This way, only one sample of the peak value for each pulse is stored in the ADB. The size and bias current of the input transistor was optimised for readout of relatively long silicon strips with a total capacitance up to 25 pF. The current in the input

transistor can be set by an internal DAC in the range between 50 μA and 300 μA.

The pulse shape at the output of the shaper can be reconstructed by scanning the delay of the calibration signal with respect to the clock phase so that a different time slice of the pulse is readout for each scan point. The internal delay register is built as a simple chain of inverters and it is not designed for an absolute delay value. For the present batch the conversion factor between the designed delay and the real delay is equal 1.2. Fig. 3 shows the result of one delay scan for a particular channel of the SCT128A-HC chip. The injected charge was 6 fC. The obtained peaking time matches very well the design value of 25 ns.

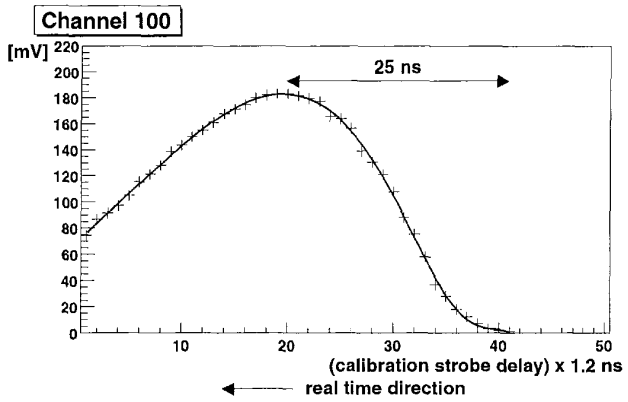

Figure 3: Pulse shape at the multiplexer output obtained from the delay scan. The injected charge was 6 fC.

For tracking applications there is no particularly demanding requirement with respect to the linearity. Nevertheless, the SCT128A-HC chip has been designed to provide a linear response up to 12 fC of the input charge. Fig. 4 shows the linearity measured for one channel. The average gain is 25.5 mV/fC while a typical spread of gain in 128 channels of one chip is 0.9 mV/fC rms, i.e. 3%. Although the uniformity of gain is not a very critical issue for the analogue architecture the obtained figure allows use of the chip without off-line correction.

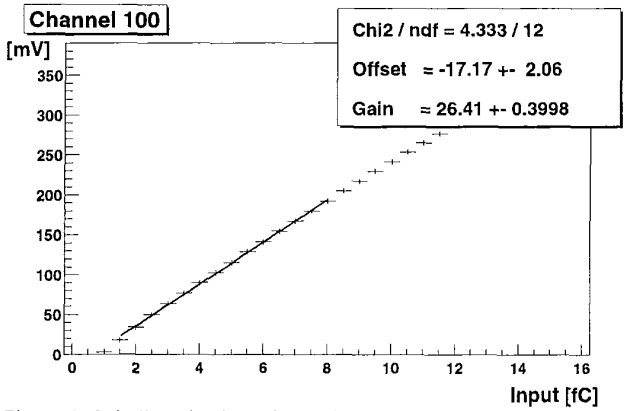

Figure 4: Gain linearity for a single channel.

The noise performance of the SCT128A-HC chip can be optimised according to the detector capacitance by choosing a proper value of the current in the input transistor. An example of noise measurements for three different values (100 μA, 160 μA and 200 μA) of the current in the input transistor is shown in Fig. 5. The noise measurements were taken for the chip operating at the clock frequency of 40 MHz. The noise was measured by random reading of cells of the pipeline so that the measured value includes cell-to-cell pedestal variation in the pipeline. The two groups of channels at the edges of the chip were connected to 6 cm long strips of the capacitance about 9.5 pF, while the inputs of the central part of the chip were left open. For the channels with open inputs one can notice dependence of noise on the base current in the input transistor. For the channels connected to strips the resulting noise is the sum of the parallel noise and the series noise, which vary in opposite directions with the bias current of the input transistor. As a result the noise is almost the same for quite different values of the current.

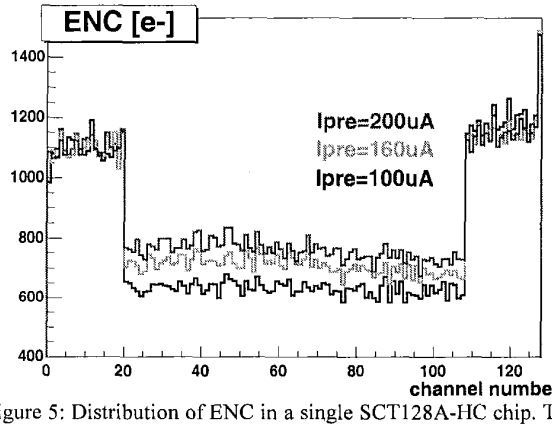

Figure 5: Distribution of ENC in a single SCT128A-HC chip. The 20 channels on each side were connected to the silicon strips.

From the data shown in Fig. 5 we obtain approximately the following noise figures:

ENC = 757 + 38 e^-/pF for 200 μA in the input transistor,
ENC = 707 + 43 e^-/pF for 160 μA in the input transistor,
ENC = 634 + 53 e^-/pF for 100 μA in the input transistor.

B. Analogue Pipeline Performance

Since the SCT128A-HC chip performs very simple voltage sampling where only analogue value is stored/retrieved from the pipeline, the pedestal spread between ADB cells contributes as an additional noise source. By varying the delay between reset signal (reset of the write/read pointer in the ADB) and the trigger sent to the chip one can obtain the pedestal map in the ADB. Fig. 6 shows the ADB pedestal map (128 cells × 128 channels) for one chip. From the presented figure one can extract the cell-to-cell pedestal variation as well as variation of the DC offset spread between channels.

The spread of the DC offsets between channels is in the range of 20 mV p-p while the spread of the pedestals along one channel of the ADB is in the range of 2 mV p-p. The distribution of the pedestals in one particular channel is shown in Fig. 7. The spread value of 0.4 mV rms has to be compared with the gain of 25 mV/fC which gives an additional contribution of 100 e^- rms to the noise generated in the front-

end. For a low bias current in the input transistor and a low detector capacitance the additional contribution is about 3% of the overall noise at the output. For higher detector capacitances and respectively higher currents in the input transistor, as required for optimisation of noise, this contribution becomes negligible.

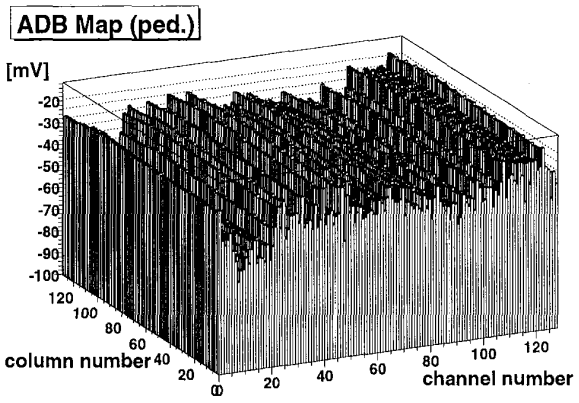

Figure 6: Map of the pedestals in the ADB.

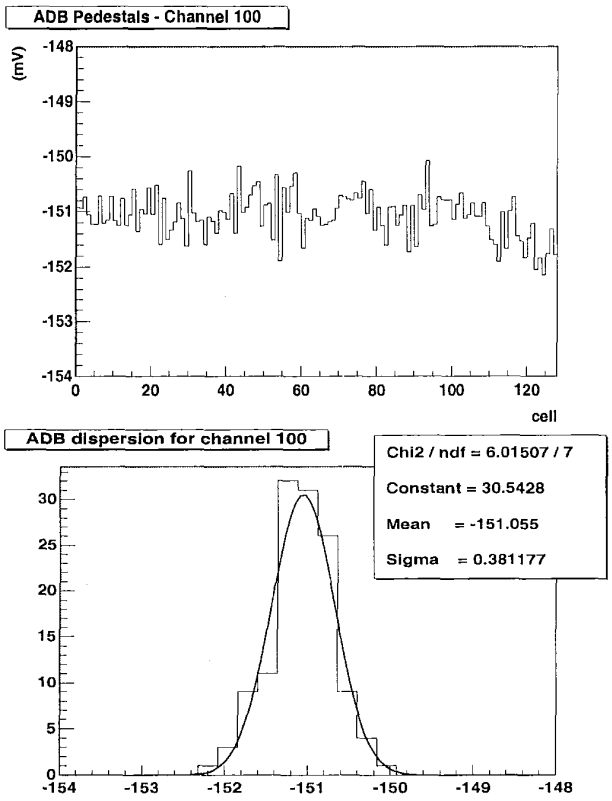

Figure 7: Pedestal distribution of 128 ADB cells in one particular channel.

C. Readout Protocol

The readout logic is designed in such a way that two 128-channel chips can be daisy chained and read out via one analogue link. Upon receiving a trigger signal the data is sent first from one chip while the second one connected to the same fibre waits for the appropriate number of clock cycles before sending the data. The data package from each chip consists of a 4-bit header, three analogue values which can be used for calibration of the optical links, 1-bit FIFO overflow flag, 4-bit BCO counter and 4-bit level-1 trigger counter. Fig. 8 shows a scope view of the read-out sequence at nominal readout speed of 40 MHz.

The 4-bit BCO counter and L1 counter contents returned by the chip can be used for synchronisation of each trigger with the physical data from the detector. In the case of overflow of the readout buffer the control logic issues an overflow bit which is bundled with the physical data. After detection of the overflow error the chip should be reset by means of the soft-reset command.

The maximum clock rate of the multiplexer and the readout circuit is the same as the rate of sampling the data, i.e. 40 MHz. The chips can be read out with a lower rate (40 MHz divided by 2, 4 or 8) which is programmable. All communication with the chip i.e.:
- sending the level 1 triggers,
- sending the software reset,
- loading the DACs,
- issuing the internal calibration pulses
- programming the speed of the output MUX

is executed via a fast 40 MHz serial interface.

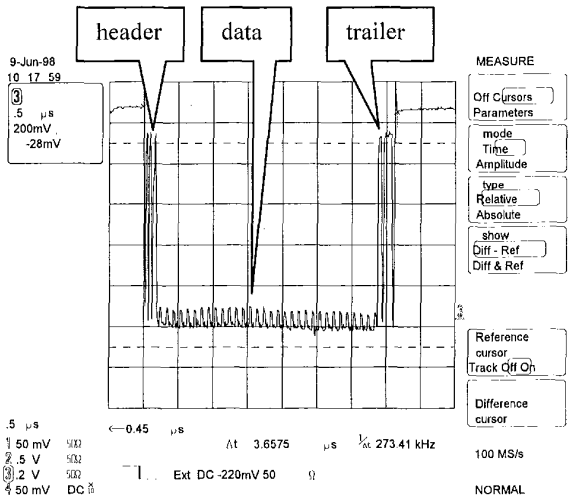

Figure 8: Response of the chip to a 4 fC calibration signal injected in every fourth channel.

III. Si Strip Detector Module

A. The ATLAS Si Strip Sensors

The microstrip silicon sensors for the ATLAS experiment are single sided 285 μm thick detectors with highly p-doped implant strips in a high resistivity (2-10 kΩcm) n-type substrate. The implanted strips are AC coupled to Al read-out strips via a silicon dioxide / silicon nitride layer. The coupling capacitance is of the order of 20 pF/cm. The strips are biased from a common bias line through polysilicon resistors of

1.25 MΩ. The pitch of the detector is 80 μm. The total interstrip capacitance (one strip to all neighbours) is about 1.1 pF/cm at 150 V bias voltage, which together with the capacitance to the back plane gives about 18 pF load capacitance at the input of the amplifier for 12.8 cm long strips.

B. The SCTA Module

The module consists of two daisy chained Si strip sensors and six SCT128A-HC chips. The chips are mounted on a ceramic hybrid connected to the sensors in the end-tap configuration. The pitch adapter needed to match the strip pitch of 80 μm and the pitch of input pads on the chip, which is 60 μm, is integrated on the hybrid. In order to evaluate the noise performance of the chips as a function of the input capacitive load three chips were connected to 6 cm long strips and three other chips were connected to 12 cm long strips. The photo of the module is shown if Fig. 9.

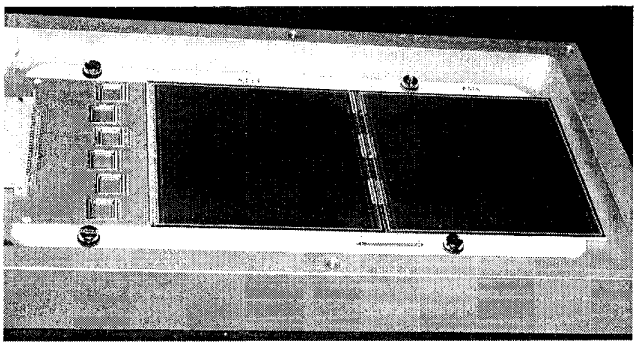

Figure 9: Photo of the 12 cm module with 6 SCTA128A-HC chips.

C. Test Beam Results

The module was tested in 100 GeV pion beam at the SPS accelerator at CERN. The test beam set-up included a high precision telescope consisting of four planes of silicon strip detectors which provide the track position with resolution of the order of 2 μm in both co-ordinates perpendicular to the tracks. An example of residual distribution for one of the telescope detectors is shown in Fig. 10.

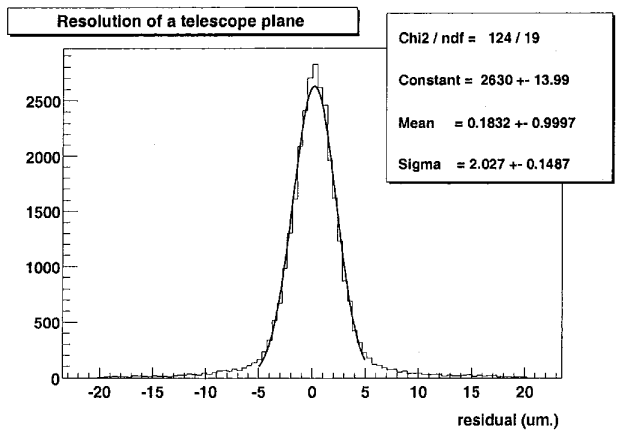

Figure 10: Spatial resolution of the Si telescope.

For the analysis of the beam test data first a set of events is processed in order to obtain the pedestals, the electronic noise and the calibration factors for the readout flash ADC card. Then, a search for clusters is performed, selecting strips having signals higher than 4 times their noise. Any neighbouring strips with a signal over noise figure exceeding a value of 3 are added into the cluster definition.

The signal over noise distributions for the cluster signals for 6 cm strips region and for 12 cm strips region are shown in Fig. 11 and Fig. 12 respectively. The most probable values of the signal-to-noise ratio are 26 and 18 for 6 cm and 12 cm region respectively. These values are largely sufficient to provide a high particle detection efficiency while keeping the noise occupancy well below ATLAS requirements.

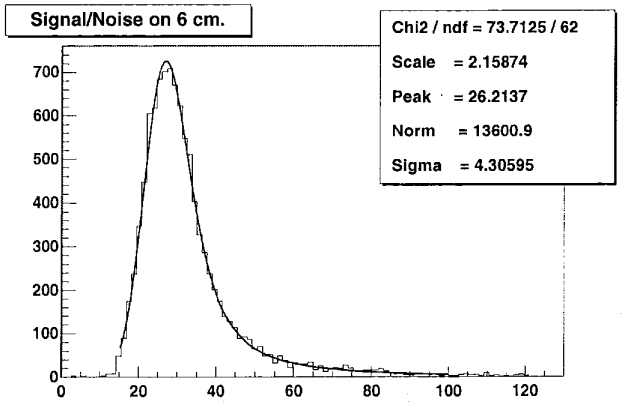

Figure 11: Signal-to-noise distribution for 6 cm strips region.

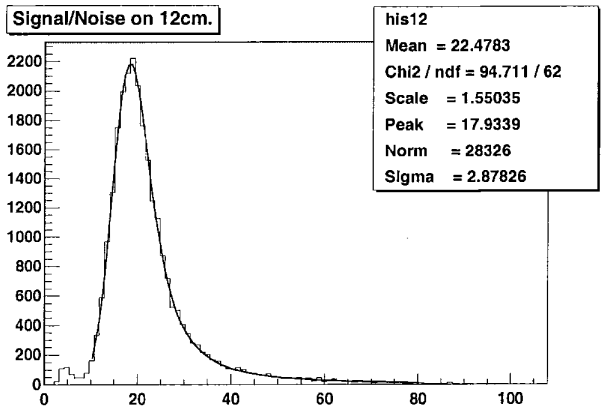

Figure 12: Signal-to-noise distribution for 12 cm strips region.

For the given strip pitch of 80 μm in the ATLAS-SCT detectors and perpendicular tracks most of the events result in single strip hits. For those events the spatial resolution is expected to be like for a binary system, i.e. pitch/sqrt(12). For double strip hits one gets a significant improvement of the spatial resolution by weighting the reconstructed position with signal amplitudes at two neighbouring strips. In our test we had about 85% of events with single strip hits and 15% with double strip hits. The distributions of residuals are shown in Fig. 13 separately for the double and single strip hits. The spatial resolutions are 3.0 μm and 21.4 μm respectively. Given

a relatively small fraction of double strip hits in our test the overall spatial resolution is determined by the single strip hits. In the experiment, however, the fraction of double strip hits is expected to be much higher due to inclined tracks and effects of the magnetic field which results in additional smearing of the charge collected in the detector.

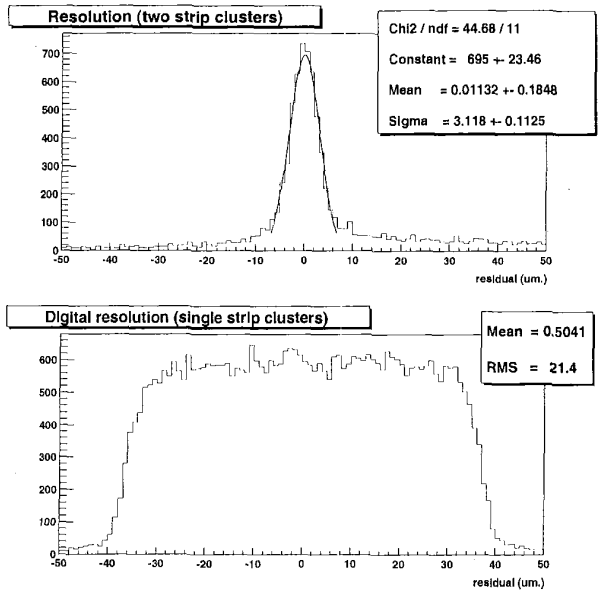

Figure 13: Distributions of residuals for double strip hits and single strip hits.

Another important module parameter measured in the test beam was the track efficiency. For each track reconstructed in the telescope, we search for a signal in the tested module in the region –200 μm +200 μm around the projected track position. For each reconstructed track we search also for any signal outside the track region and this signal are counted for noise occupancy. The efficiency and noise occupancy depend on the criteria we apply for the signal definition. Fig. 14 shows the noise occupancy vs efficiency for the cuts on the cluster signal of 7σ, 6σ, 5σ, 4σ, 3σ consecutively, where σ is the rms value of noise.

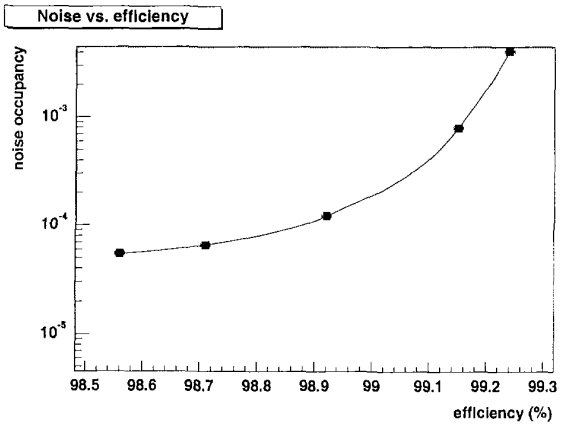

Figure 14: Efficiency versus noise occupancy for cuts on the signal equal to 7σ, 6σ, 5σ, 4σ, 3σ consecutively.

IV. Performance of the Module With the Optical Link.

An optical link for transmission of data from the SCT128A-HC chip using VCSELs is under development. Available optical power and bandwidth present no problems. The total system frequency response from the VCSEL driver to receiver output is flat up to 100 MHz. Fig. 15 shows the DC transfer characteristic of VCSEL current versus received PIN diode current.

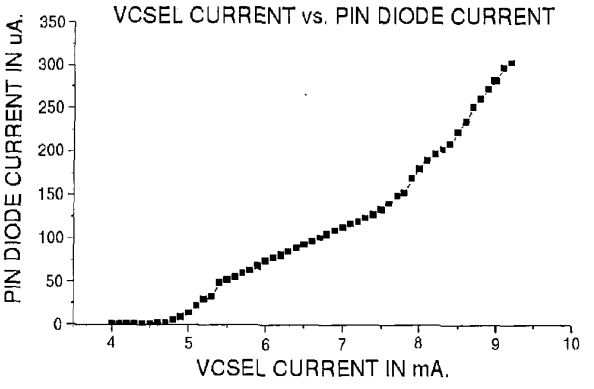

Figure 15: VCSEL characteristic.

The threshold is observed to be at 4.8 mA and the transfer characteristic is far from linear due to mode shifts in the excitation of the laser. However, there is a linear region over a sufficiently large dynamic range. The linearity of these devices is expected to improve with further development. At present one could consider to preselect VCSELs with overlapping linear regions by wafer pre-screening. The linear region is expanded in Fig 16.

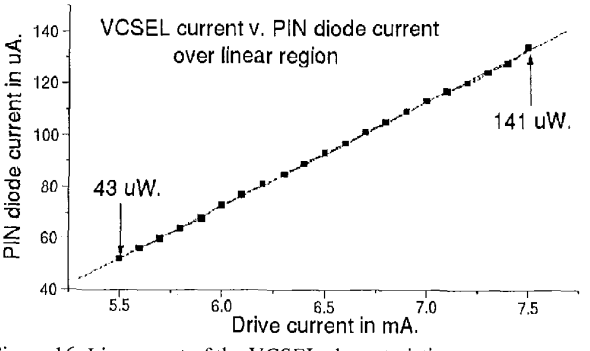

Figure 16: Linear part of the VCSEL characteristic.

Over this range the rms linearity is of the order of 0.5 %. The VCSEL produced additional noise when biased to the centre of its linear characteristic. This was measured to be 31 μV rms at the output. The VCSEL was driven by a high impedance linear driver circuit and biased to provide the maximum linear operating range. The signal after transmission down the optical fibre at a clock frequency of 40 MHz is shown in Fig. 17. No deterioration with respect to transmission over copper can be observed.

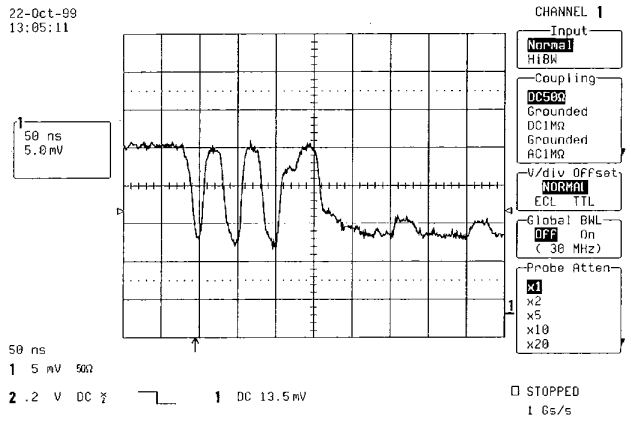

Figure 17: Scope view of 40 MHz readout operation through VCSEL optical link system.

V. Radiation Hardness

Given extreme radiation levels as expected in the trackers of experiments at the LHC the radiation hardness is a very important issue of any front-end chip. Although the SCT128A-HC chip is realised in the DMILL radiation hard technology the radiation effects in the devices are not negligible and cannot be ignored. A particularly critical issue is the noise of the front-end circuit.

The front-end circuit is built as a transimpedance amplifier using a bipolar input transistor. One of the noise sources, which contribute to the equivalent input noise charge is the shot noise of the base current of the input transistor. Due to a short shaping time of 25 ns, and a large detector capacitance, the relative contribution of this noise is acceptable as long as the base current does not exceed a level about 2 μA. For given detector capacitance, shaping time and current gain factor β of the input transistor, one can find an optimum value for the collector current which yields a minimum value of ENC.

In modern bipolar transistors the current gain factor β is degraded by the ionisation effects as well as by the displacement damage. Both types of radiation effects, ionisation and displacement damage, lead to reduction of the lifetime of minority carriers in the transistor base. Thus, a significant degradation of β has to be anticipated, which implies that, first of all, the circuit design has to be insensitive to variation of β regarding DC bias conditions as well as AC characteristics. With respect to noise there are two aspects to be taken into account, namely the size of the transistor and the collector current in the input transistor.

The degradation of β depends on the actual current density in the transistor, therefore from that stand point of view one would prefer to use a minimum geometry transistor in the input stage. On the other hand, in order to minimise the series noise contribution from the base spread resistance, one would rather use a large area input transistor. These two requirements are contradictory and an optimum size of the input transistors can be defined provided we know how the β degrades after irradiation for a given technology. The radiation effects in the bipolar transistors in the DMILL technology have been studied and based on these results we chose the emitter area of the input transistor to be 1.2×10 μm^2.

From the radiation tests performed up to now we expect that β of the input transistor will change significantly, by a factor of about 4, during irradiation up to a level of 2×10^{14} n/cm^2. With the β value decreasing during the lifetime of the experiment the optimum value of the collector current in the input transistor will also decrease. Therefore we have implemented a 5-bit DAC to be able to adjust the current and optimise the noise performance according to the actual value of β in the input transistor.

The present version of the SCT128A-HC chip was produced in the DMILL process not being completely stabilised at that time yet. In particular, we used in the chip resistors which exhibited a high sensitivity to radiation, resulting in increases about 50% after irradiation up to maximum radiation levels. This effect creates problems for the DC bias conditions of the circuit so that the noise performance cannot be tested up to the ultimate radiation levels. The front-end circuit of the SCT128A-HC chip is almost identical to that one implemented in the ABCD chip, which was produced in an upgraded version of the DMILL process and uses a different type of resistors. After replacing the resistors in the SCT128A-HC for the new ones we expect the same radiation hardness performance as observed now in the ABCD chip.

The ABCD chips were irradiated separately with 24 GeV proton beam up to a fluence of 3×10^{14} p/cm^2, neutrons from a nuclear reactor up to 2×10^{14} n/cm^2 and with X-ray up to a total dose of 10 Mrad. The noise as a function of the current in the input transistor before and after those radiation tests is shown in Fig. 18.

After X-ray irradiation we see a small increase of noise as expected since one does not expect a significant degradation of β in this case. For the chips irradiated with relativistic protons up to 3×10^{14} p/cm^2 the increase of noise is significant. A large increase of noise is observed after neutron

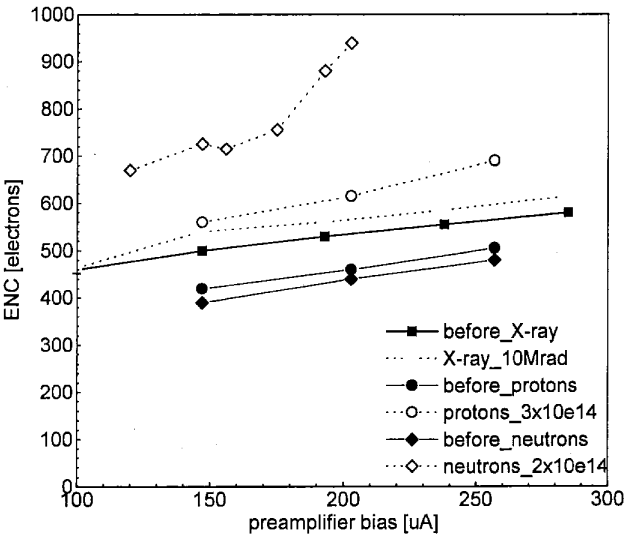

Figure 18: Noise as a function of the current in the input transistors after X-ray, proton, and neutron irradiation.

irradiation up to 2×10^{14} n/cm^2. Assuming that the shaping function of the overall front-end circuit can be approximated by a CR-RC^3 filter with a peaking time of 25 ns one can evaluate the β values corresponding to the measured noise levels, as about 60 after proton irradiation and about 30 after neutron irradiation respectively.

VI. Conclusions

A fast radiation-hard front-end chip, the SCT128A-HC, has been developed for the readout of Si strip detectors employed in the inner tracking detectors of LHC experiments. The chip is produced in DMILL technology. The architecture of this chip is implemented according to the specifications for use in LHC experiments.

Si strip detector prototype modules have been built and tested in the test bench as well as in the test beam. Performance adequate for the requirements of the tracking systems of LHC experiments has been demonstrated.

References

[1] "APV6-RH A 128 Channel Read-out Chip For The Silicon Tracker In CMS" Fourth Workshop on Electronics for LHC experiments Rome, September 21-25,1998, CERN/LHCC/98-36.

[2] F.Anghinolfi et al. "AROW - A 128 Channel Analogue Pipeline with Wilkinson ADC and Sparsification ASIC", First Workshop on Electronics for LHC experiments, Lisbon, September 11-15,1995, CERN/LHCC/95-56.

[3] D. Campbell et al. "The ATLAS binary chip", Second Workshop on Electronics for LHC experiments, Balatonfured September 23-27, 1996, CERN/LHCC/96-39.

[4] "DMILL, a Mixed Analog-Digital Radiation-Hard Technology for High Energy Physics Electronics", RD29 Status Report, CERN/LHCC 97-15, March 1997.

[5] W. Dabrowski et al. "Design and performance of the ABCD chip for the binary readout of silicon strip detectors in the ATLAS Semiconductor Tracker", presented at this conference.