TOTAL DOSE AND SINGLE EVENT EFFECTS (SEE) IN A 0.25μm CMOS TECHNOLOGY

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ABSTRACT

Individual transistors, resistors and shift registers have been designed using radiation tolerant layout practices in a commercial quarter micron process. A modelling effort has led to a satisfactory formulation for the effective aspect ratio of the enclosed transistors used in these layout practices. All devices have been tested up to a total dose of 30Mrad(SiO_2). The threshold voltage shift after irradiation and annealing was about +45mV for NMOS and -55mV for PMOS transistors, no leakage current appeared, and the mobility degradation was below 6%. The value of resistors increased by less than 10%. Noise measurements made on transistors with W=2mm and L varying between 0.36 and 0.64μm revealed a corner noise frequency of about 200kHz for the NMOS and 12kHz for the PMOS. Irradiation up to 30Mrad(SiO_2) did not significantly affect the noise performance. The shift registers continuously operated at 1.25MHz during the irradiation, and no error was detected in the pattern propagation. No functional degradation was observed. An irradiation with a heavy ion beam was made on the shift registers to study their sensitivity to Single Event Effects (SEE). No Single Event Latch-up (SEL) was observed up to a LET of 89 MeVcm^{2}mg^{-1}. The register designed using dynamic logic, with a threshold LET lower than 3.2 MeVcm^{2}mg^{-1}, proved to be considerably more sensitive to Single Event Upset (SEU) than its static logic counterpart, which had a threshold LET of about 15 MeVcm^{2}mg^{-1}. A novel SEU-tolerant design was demonstrated to be extremely effective as storage cell.

1. MOTIVATION

In agreement with the first measurements on ultra-thin oxides [1], recent studies confirmed the total dose hardness of the thin oxide of a commercial 0.25μm CMOS technology [2]. The use of radiation tolerant layout practices, based on the systematic use of enclosed NMOS transistors and guardrings, was demonstrated to extend the tolerable total dose level well beyond the inherent technology limit [3].

All these results are extremely promising in view of the possible use of deep submicron technologies for the readout electronics of LHC. In this respect, some important issues not addressed in references [2] and [3] still needs to be studied.

How to estimate the correct effective aspect ratio of enclosed geometry transistors, an important parameter entering in the design of a circuit, is not known. The noise of transistors in deep submicron technologies needs to be characterised. Moreover, no investigation of Single Event Effects has been carried out on structures designed in a deep submicron process using radiation tolerant layout practices.

This paper describes the work in progress to study all the above issues.

2. EXPERIMENTAL DETAILS

2.1 Description of the test vehicle

We have designed a test vehicle in a commercial 0.25μm process using three of the five available metal layers. The relevant features of this technology are summarised in Table I.

The test vehicle consisted of a series of individual NMOS and PMOS transistors in both standard linear and enclosed geometry, a ring oscillator, three shift registers and a few logic gates. Also, a prototype front-end readout chip for pixel detectors was integrated, for which results are presented separately at this conference [4].

The standard linear NMOS and PMOS transistors were designed with the same gate width, W=10μm, and with gate length varying between 0.28 and 5μm. All the enclosed geometry NMOS transistors had the same size for the inner diffusion, and gate length varying between 0.28 and 5μm. In this case, two identical transistors for

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each gate length were integrated in order to study the matching properties of enclosed devices.

Table I: technology features.

Vdd = 2.5V
Min. L (drawn) = 0.24 μm
t_{ox} (physical) = 5 nm
Vth N/P = 550/-450 mV
Zero-Vt NMOS transistors available
Shallow trench device isolation (STI)
2 to 5 levels of global metal (+ M0 for local connect.)
Stud contact and wiring level vias
Metal to metal capacitor available

Two zero-V_t NMOS transistors were designed with enclosed shape, with channel length L_{drawn}=0.6μm and L_{drawn}=1μm. Several n-well resistances were integrated.

To study the radiation behaviour of the field oxide, a series of Field Oxide Transistors (FOXFET) has been designed, using polysilicon or metal 1 gates. In some of these devices, the two n+ diffusions constituting the source and drain are separated by a p+ strip. This simulates the presence of a guardring, and allows the direct measurement of its effectiveness in preventing any leakage current.

Three shift registers were integrated to study SEEs on circuits designed in the quarter micron process, each register made up of a number of identical D-Flip-Flop (FF) cells. One of the registers used the standard static architecture for the FFs, another one used a dynamic architecture, and the third one was static but implemented using a dedicated SEU-tolerant ("hard") design. This design is the successor of two other architectures successfully used to harden memory cells against SEU [5][6]. The size of the FF was 18x16μm for the dynamic, 33x16μm for the standard static and 50x16μm for the "hard". The number of FFs was 2048 for the two static registers and 1024 for the dynamic design.

All the shift registers used radiation tolerant layout practices: all the NMOS and most of the PMOS were designed with enclosed geometry, and guardrings surrounded all the NMOS devices. All together, the three shift registers contained some 150000 transistors, and occupied an area of about 2.7mm^2.

2.2 Irradiation conditions

Total dose irradiation tests were performed at room temperature and under bias, mainly using a SEIFERT RP-149 X-ray irradiation facility with a tungsten target for X-ray production (about 10keV fluorescence peak). For individual transistors, worst case bias was applied in all cases. Another set of irradiations was performed on individual transistors using a ^{60}Co γ-ray source. Annealing took place in all cases under bias: at room temperature for one day, to monitor the fast annealing, and then for one week at 100°C following the ESA qualification procedure [7].

Single Event Upset (SEU) and Latch-up (SEL) measurements were performed at the LBL (Lawrence Berkeley Laboratories, California) cyclotron using a heavy ion beam at room temperature. The LET (Linear Energy Transfer) was changed by selecting the ion species (Nitrogen, Neon, Argon, Copper, Krypton and Xenon) and by tilting the device up to 55° relative to the beam line. In this way, LETs varying from 3.2 to 89 MeVcm^{2}mg^{-1} were obtained.

3. ENCLOSED NMOS: ASPECT RATIO AND OUTPUT CONDUCTANCE

If the use of the enclosed geometry for the NMOS transistors eliminates radiation-induced leakage currents, their special shape does not constitute a common practice in VLSI design. Therefore, no effort has been conducted so far in modelling transistors with such shape. The absence of a convenient model, at least for the effective aspect ratio (W/L), poses a problem especially for analog design. The approximation for the aspect ratio proposed in [3] and based on the assumption of square equipotential lines under the gate might lead to a 30-40% over-estimate. To solve this problem, we have developed a model to estimate the aspect ratio of the enclosed transistors.

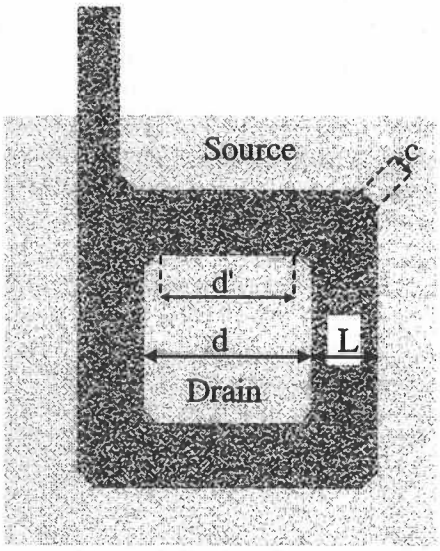

Figure 1: Enclosed transistor shape.

3.1 Transistor shape

There is a wide range of possible enclosed shapes: squared, octagonal, squared with corners cut at 45°, and all of them can have different behaviour and require a separate model. To simplify the problem, we have chosen one specific shape compatible with the design rules of the quarter micron process, and we concentrate our modelling efforts on that. This shape is shown in Figure

1. The corners of the gate are cut at 45° so that the size of the cut (c in the figure) is constant for all gate lengths. Compared to the octagonal shape, in the chosen geometry the current flows mainly in two orthogonal directions, assuring in general a better homogeneity. This in turn results in better device matching.

3.2 Aspect ratio

A detailed study of the transistors with enclosed geometry has been made, and is described in [8]. This study proposes a model for the effective W/L of enclosed transistors. If applied to the shape of Figure 1, the model leads to the following expression for the aspect ratio:

$$\left(\frac{W}{L}\right)_{eff} = 4\frac{2\alpha}{\ln\frac{d'}{d'-2\alpha L_{eff}}} + 2K\frac{1-\alpha}{1.13\cdot\ln\frac{1}{\alpha}} + 3\frac{\frac{d-d'}{2}}{L_{eff}}$$

In the formula, d is the size of the central drain as shown in Figure 1, $d' = d - 2\frac{c}{\sqrt{2}}$ is the length of the linear inner side of the gate, L_{eff} is the effective channel length, and α is a constant set to 0.05. K=7/2 for short channel transistors ($L \le 0.5\mu m$), otherwise K=4. In our test transistors, d=0.84μm. To derive the above expression, the enclosed transistor is decomposed into three parts. The first part corresponds to the linear edges of the transistor, the second to the corners without the 45° cut, which then is taken into account separately as the third part. The presence of the up-left polysilicon strip, necessary to integrate the gate contact outside the thin gate oxide region, eliminates a part of the corresponding transistor corner: this is taken into account in the formula.

Table 2: Estimated and extracted $(W/L)_{eff}$ for enclosed NMOS transistors with different gate length.

L_{drawn}	Estimated $(W/L)_{eff}$	Extracted $(W/L)_{eff}$
0.28	14.8	15
0.36	11.3	11.2
0.5	8.3	8.3
1	5.1	5.2
3	3	3.2
5	2.6	2.6

The estimated aspect ratio obtained using the above equation has been compared to the one extracted for the individual transistors integrated in the test vehicle. The effective aspect ratio $(W/L)_{eff}$ of enclosed transistors has been extracted by comparing, for the same V_{GS}-V_{th}, their drain current to the drain current of standard transistors with the same L. The results are summarised in Table 2. The maximum difference between estimated and extracted values is about 6%.

The expression for the aspect ratio can also be used for transistors designed by stretching in one or both directions the shape in Figure 1, provided the corners are not modified. In that case, one just needs to add the contribution of the linear regions generated by the stretching. Transistors with aspect ratio as large as desired can be designed in this way. On the contrary, there is a limitation in the minimum aspect ratio obtainable with enclosed transistors.

As shown in Table 2, the aspect ratio decreases when the gate length is increased. For channel length close to 7μm, the dominant contribution to the transistor current comes from the gate corners. This corresponds to the second term in the above expression, which does not depend on the gate length. Therefore, the aspect ratio reaches a "saturation" value of about 2.3 for $L_{drawn} \approx 7\mu m$. This important limitation for analog design is inherent to the use of enclosed transistor shapes.

3.3 Output conductance

In an enclosed shape transistor, source and drain are not symmetric. The inner diffusion has a much smaller area, hence capacitance, than the outer one. As the gate perimeter is different in the inner or outer side, the transistor output conductance in saturation changes depending on whether the inner or outer diffusion is chosen as the drain. Measurements summarised in Table 3 show that the output conductance is lower when the outer diffusion acts as the transistor drain, and that this asymmetry increases with the gate length. This second trend is easily explained by the fact that the outer gate perimeter increases with the gate length, whilst the inner one does not.

Table 3: Output conductance for enclosed NMOS transistors of different gate length. G_{di} = inner diffusion as drain, G_{do} = outer diffusion as drain. Difference = $(G_{di}-G_{do})/G_{di}$. Measurements for V_{GS}-V_{th}=300mV.

L_{drawn} (μm)	G_{di} (μS)	G_{do} (μS)	Difference (%)
0.28	11.09	9.62	19
0.36	7.17	5.55	23
0.5	4.10	2.73	33
1	1.68	0.79	53
3	0.57	0.17	70
5	0.41	0.10	75

This characteristic asymmetry of the enclosed NMOS should be taken into account for the choice of which of the two diffusions is the drain. In general, capacitive load and improved output conductance will have to be traded off against each other.

4. TOTAL DOSE RESULTS

In the following all results refer, unless otherwise specified, to X-ray irradiation tests at a dose rate varying

between 20 and 30 krad(SiO_2)/min. During irradiation and annealing, the bias of the individual transistors was kept in the "worst case" condition. This means $V_{source}=V_{drain}=V_{sub}=0V$ and $V_{gate}=V_{dd}=2.5V$ for the NMOS, and all terminals grounded for the PMOS transistor.

4.1 Individual transistors using radiation tolerant layout practices

In this paragraph, we group the results concerning enclosed NMOS (including Zero-V_t enclosed transistors) and standard PMOS transistors, which are used together in designs where a high level of radiation tolerance (>100-200krad) is required.

The threshold voltage shift as a function of the total dose is shown in Figure 2 for an irradiation up to 30Mrad(SiO_2). The results refer to transistors with minimum (NMOS and Zero-Vt) or close to minimum (PMOS) gate length. Similar results were obtained for all other channel lengths. Immediately after irradiation (black points), the threshold voltage shift is less than 35mV for the NMOS, and about 70mV for the PMOS transistors. For a total dose of 10Mrad, these values are 15 and 30mV respectively.

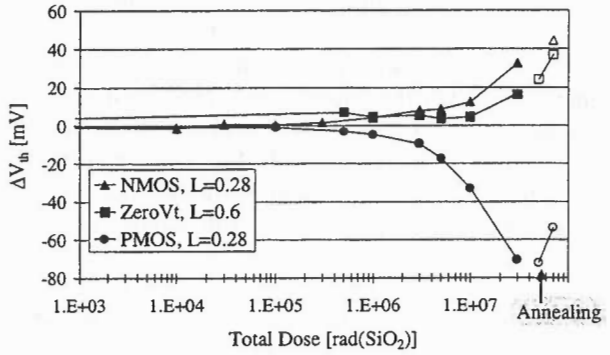

Figure 2: Threshold voltage shift of enclosed NMOS, enclosed Zero-V_t NMOS and standard PMOS transistors as a function of the total dose. The white points represent the measurement after 24hours at room temperature (first point) and after final high temperature annealing (last point).

During the annealing (white points), the threshold voltage shift increases to about 45mV for the NMOS and decreases to about 55mV for the PMOS transistors. This is due to the de-trapping of the charge trapped in the oxide and, for the NMOS, to the creation of new interface states. As expected for the thin gate oxide of the quarter micron process, both trapping of charges in the oxide and generation of interface states give contributions of the order of tens of mV to the threshold voltage shift. This is clearly demonstrated by the measurement of the sub-threshold swing (the inverse of the slope), which increases only by about 5mV/dec for the NMOS and 2mV/dec for the PMOS transistors. The change in the swing is directly related to the creation of new interface states.

The mobility degradation is minor as well: we measured a maximum decrease of about 6% for the NMOS (Zero-V_t devices included) and 2% for the PMOS transistors after 30Mrad(SiO_2) and annealing.

The output conductance of both NMOS and PMOS transistors is practically unchanged after the highest dose irradiation and annealing, as shown in Figure 3 for transistors with gate lengths of 0.28 and 2μm. The dashed lines, referring to the post-irradiation measurements, are practically indistinguishable from the pre-irradiation lines.

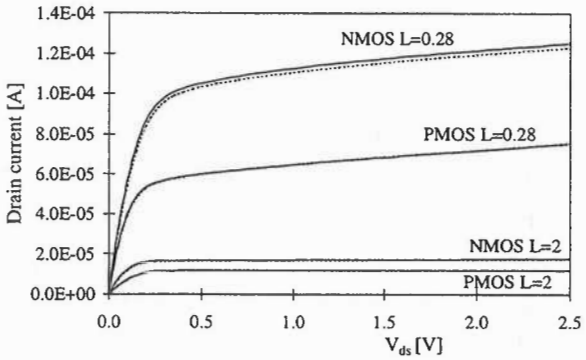

Figure 3: Saturation curves for enclosed NMOS and standard PMOS transistors before (solid lines) and after 30Mrad(SiO_2) and annealing (dashed lines). V_{GS}-V_{th} was about -330mV for the PMOS and 230mV for the NMOS transistors in all measurements.

The enclosed geometry of the NMOS transistors effectively eliminates any source-drain leakage path. This is shown in Figure 4, where the transistor leakage current is plotted as a function of the total dose. The PMOS transistor leakage decreases slightly at high total doses. This is explained by the fact that before irradiation the PMOS transistor is at the very beginning of the weak inversion already for $V_{GS}=0V$ and $V_{DS}=2.5V$. As the leakage current is measured under such bias, the weak inversion current is seen as a leakage. With the irradiation, the threshold voltage increases, and this leakage disappears.

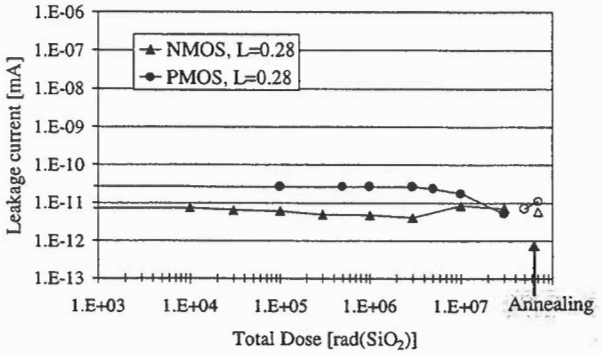

Figure 4: Leakage current for enclosed NMOS and standard PMOS transistors.

Our measurements also confirmed that the systematic use of guardrings around NMOS transistors is effective in preserving the device isolation: no leakage current has been measured in the FOXFETs where a p+ diffusion separated source and drain, even after a total dose of 30Mrad(SiO_2).

4.2 Standard NMOS transistors

For applications where a low level of radiation tolerance is required (10-20krad), our previous study [2] suggested that the quarter micron technology could be used without applying radiation tolerant layout practices. To explore this possibility, we have measured the behaviour of standard NMOS transistors of different channel lengths up to a total dose of 200krad(SiO_2).

The transistor leakage current for NMOS transistors is shown in Figure 5. Up to the total dose of 200krad(SiO_2), no increase of the leakage current is observed on any transistor. The measurement of the integrated FOXFETs showed no leakage between adjacent n+ diffusions. This means that, up to this level of total dose, the electrical isolation between devices is still very effective.

The threshold voltage shift was in all cases less than 2mV, the sub-threshold swing changed less than 1mV/dec, and the mobility was practically unchanged.

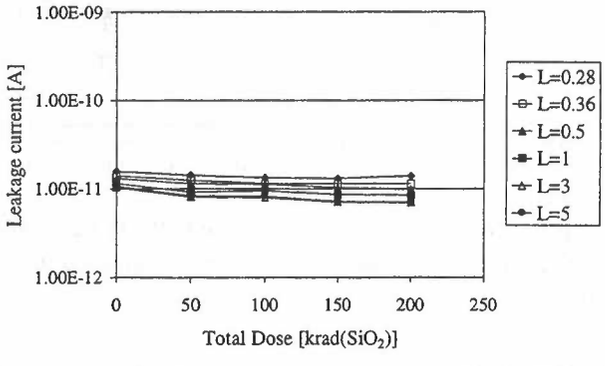

Figure 5: Leakage current for standard NMOS transistors of different gate length.

These results were confirmed by an additional irradiation made using a ^{60}Co γ source up to 200krad. In that case, the leakage was always below $6 \cdot 10^{-11}$A, the threshold voltage shift was less than 2mV, and the sub-threshold swing change was less than 5mV/dec.

All the above results confirmed that, for applications requiring a low level of radiation tolerance, the safety margin for the technology is sufficiently wide to allow its safe use without specific radiation tolerant layout. Nevertheless, as the radiation tolerance of a commercial process is not a guaranteed or even monitored parameter, a qualification process should be put in place to assure that the radiation performance constantly meets the requirement during the production phase.

4.3 Resistors

Three n-well resistors were integrated in the test vehicle to measure their evolution with the total dose. These resistors had nominal values of 3.3, 1.65 and 0.2kΩ. They were irradiated with X-rays at a dose rate of 30krad(SiO_2)/min and with the two leads grounded. The irradiation results are shown in Figure 6. The maximum variation after a 30Mrad(SiO_2) irradiation is below 10% in all cases.

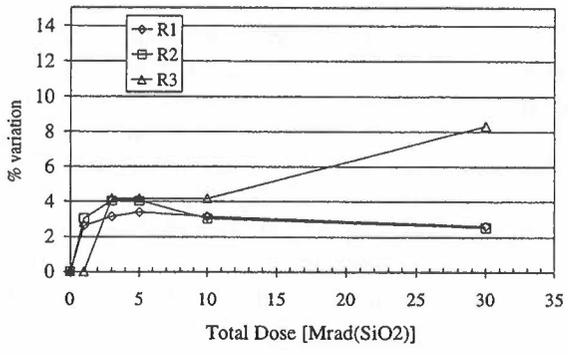

Figure 6: Evolution of the resistors with irradiation. Before irradiation, R1=3.83kΩ, R2=1.980kΩ, R3=240Ω.

4.4 Shift Registers

The three shift registers have been irradiated with X-rays up to a total dose of 30Mrad(SiO_2), applying a supply voltage V_{dd}=2V. Intermediate measurements were done at 1, 3, 5 and 10Mrad. During the irradiation, performed at a dose rate of 30 (up to 10Mrad) and 40krad/min (from 10 to 30Mrad), the shift registers worked continuously. A pattern of alternate 1s and 0s was circulated at a frequency of 1.25MHz, and the output from the registers was compared with the written pattern to detect eventual errors in the propagation. No error was detected in any of the registers during the irradiation up to 30Mrad.

Our setup only allowed us to establish the functionality, but could not be used for high-speed measurements (>2.5MHz). Functionality was conserved during and after irradiation and annealing. The lower limit of operating frequency for the dynamic register, determined by the transistors leakage current, is reduced by the irradiation below 4.9kHz. This result can be understood from the decrease of the PMOS leakage current shown in Figure 4.

The results obtained on the shift registers demonstrate at the circuit level that, with the use of radiation tolerant layout practices in deep submicron commercial technologies, it is possible to design ICs able to stand high total doses.

5. NOISE

In the design of front-end circuits for the readout of particle detectors, a good understanding of the noise characteristics of the transistors is fundamental as it determines the lowest achievable circuit noise. To study the noise of transistors in the quarter micron process, we have integrated large transistors (W=2000μm) with high transconductance, which offer high drain current white noise density.

The noise measurement chain consisted of a transimpedance amplifier, a voltage gain stage and a spectrum analyser, and is described in detail in reference [9]. With this setup, we could explore the 200Hz-30MHz range. Measurements were performed with the transistors biased in moderate inversion and in saturation (V_{DS}=800mV), and with a drain current of 500μA. Three gate lengths were studied: L=0.36, 0.5 and 0.64μm.

The noise spectra of NMOS and PMOS transistors before irradiation, expressed as equivalent voltage noise at the gate, are shown in Figure 7 for two gate lengths. For the PMOS transistors, no relevant short channel effect is apparent, and the noise scales approximately with the transistor size as expected: the 1/f noise density decreases with the gate area, and the white noise density decreases with the transconductance. The cutoff frequency, where the 1/f and the white noise densities are equal, is about 12kHz.

On the other hand, a significant short channel effect appears in the noise characteristics of NMOS transistors. Both the 1/f and the white noise are higher than expected according to the scaling laws. As a result, the cutoff frequency of the 0.36μm transistor is 1.5MHz, significantly higher than the 200kHz measured for the 0.64μm transistor. These results generally indicate that, in low-noise designs, NMOS transistors with channel length below 0.5μm should be used with care.

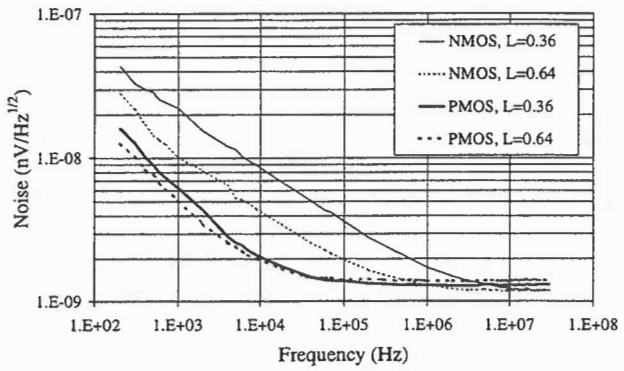

Figure 7: Noise spectra of NMOS and PMOS transistors before irradiation.

The transistors were irradiated with X-rays up to a total dose of 30Mrad (SiO_2) under worst case bias, and the noise measurement was repeated. The measured noise spectra are compared to the pre-irradiation ones in Figure 8 for a channel length of 0.36μm, and similar results were measured for the 0.5 and 0.64μm transistors. Even after such a high total dose, the degradation of the noise characteristics is very limited: the white noise increases by less than 5%, and the cutoff frequency moves only slightly towards higher frequency.

These results indicate that transistors in the 0.25μm process have an excellent noise performance, even after irradiation, and are compatible with the requirements of low noise analog design.

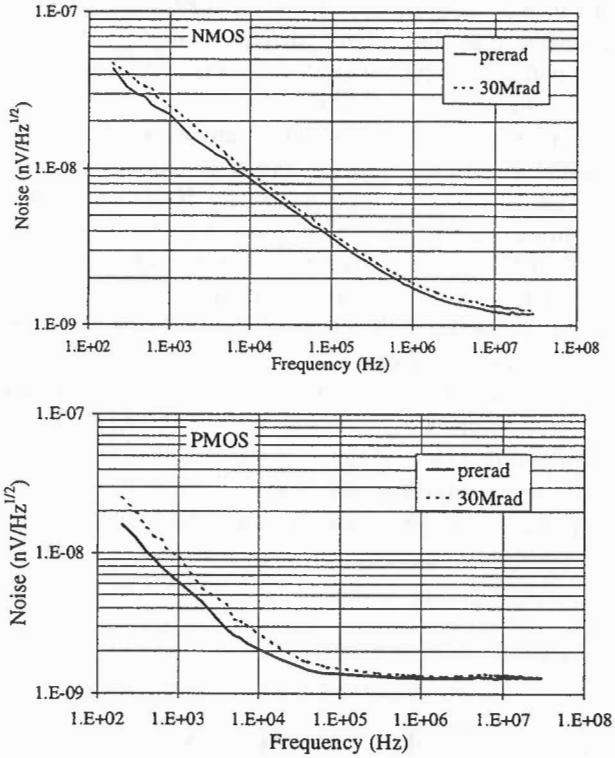

Figure 8: Noise spectra of NMOS and PMOS transistors with L=0.36μm before and after an irradiation up to 30Mrad(SiO_2).

6. SINGLE EVENT EFFECTS (SEE)

6.1 Single Event Latch-up (SEL)

SEL is a destructive SEE threatening all bulk CMOS and bipolar technologies in a radiation environment. It is triggered by excess current in the base of either a parasitic pnp or npn transistor following the charge deposition from a heavily ionising particle. This switches the parasitic thyristor in a high current self-maintaining state that can cause destructive burnout. Therefore, it can be detected by monitoring the current consumption of the circuit.

During the heavy ion irradiation, we constantly monitored the total current consumption from the three shift registers. The monitoring circuitry also included a block able to inhibit the power supply to the registers for a few ms in case of latch-up detection. This is sufficient

to break the latch-up condition and bring the circuit back to its normal operating mode.

No SEL was observed during the whole irradiation campaign, at an applied supply voltage of 2.5V, up to the maximum LET available of 89 MeVcm^{2}mg^{-1}. Similar results had previously been obtained even on standard (without guardrings) structures integrated in the same technology [10]. This result already pointed to a good robustness of this quarter micron process against SEL. As the systematic use of guardrings decreases the latch-up sensitivity [11], the result obtained on the shift registers was expected.

A recent simulation study [12] has shown that the maximum energy deposition occurring with some probability in the LHC radiation environment will correspond locally to a LET lower than 50 MeVcm^{2}mg^{-1}. This will happen in the very rare case of a nuclear interaction in the tungsten, which is often used in ICs for connection purposes between layers. Therefore, the measured threshold for SEL indicates that latch-up will not be a threat in LHC circuits designed using radiation tolerant layout practices.

As the SEL sensitivity is strongly layout-dependent, the same conclusion can not be generally extended to circuits designed using standard layout. Nevertheless, the results in [10] seem to indicate that, with a reasonable distribution of substrate and well contacts, SEL should not occur even in this case.

6.2 Single Event Upset (SEU)

The charge collection following a heavily ionising particle strike can change the state of the circuit node hit and cause false information to be stored: this phenomenon is called SEU. As the minimum charge collection needed to generate the upset is proportional to the node capacitance and the supply voltage, SEU sensitivity increases with the scaling of VLSI technologies towards smaller device size [13].

SEU sensitivity is also widely design-dependent: dynamic logic is in general considerably more vulnerable than static logic, and the sensitivity can be lowered by increasing the capacitance or the drive capability of the nodes.

To study the sensitivity of circuits designed in the 0.25μm process using layout tolerant design practices, we have irradiated the shift registers with heavy ions under different conditions, applying a supply voltage V_{dd}=2V. A first set of measurements was performed in what we call "un-clocked mode". A test pattern was written into the register (at 2.5MHz), then the clock stopped during a time interval ranging from 2 s to a few minutes, and finally the pattern was read out and compared with the original one: each difference was counted as a SEU. In this case, the write and read time was negligible compared to the storing time, and the circuits were working as "memory elements". Of course, only the two static registers could work in this mode, the dynamic register always requiring a clock to be functional.

During the second set of measurements, in what we call "clocked mode", the pattern was written and read continuously, and the comparison between data took place all the time. The clock was therefore applied throughout the test, at the constant frequency of 2.5MHz.

1) Un-clocked mode

The result for the standard static register is shown in Figure 9, where the SEU cross-section (σ) is plotted as a function of the particle LET. The cross-section is the number of errors divided by the particle fluence and the number of memory elements, hence it is expressed in cm^2/bit. Cross-section curves are a standard practice in SEU testing of circuits, as they give an immediate picture of the upset sensitivity. The cross-section value at high LET, where the curve shows a saturation, is representative of the total sensitive area of each memory cell. It is indicated as σ_{sat} and, when multiplied by the number of memory elements, it gives the total sensitive area of the chip. The other important parameter visible in the cross-section curve is the threshold LET (LET_{th}), the value at which the circuit starts to be sensitive to SEU.

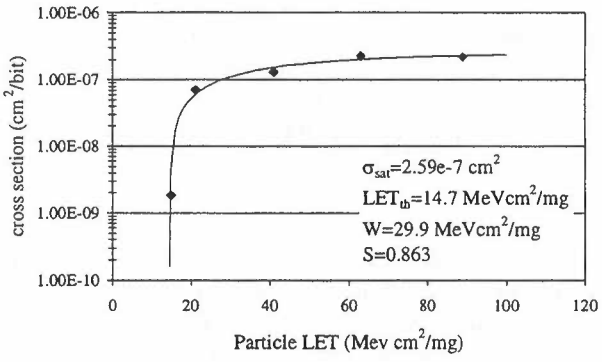

Figure 9: Experimental SEU cross-section for the static standard register.

It is common practice [14] to fit the experimental points with a Weibull curve, using the expression:

$$\sigma = \sigma_{sat}\left\{1-\exp\left[-\left(\frac{L-L_{th}}{W}\right)^{S}\right]\right\}$$

This allows for the extraction of σ_{sat} and of LET_{th}. W and S are fitting parameters without physical meaning. The values extracted are shown in Figure 9. It is interesting to note that the saturation cross-section of about 26μm^2 well matches the integral area of the sensitive node in the circuit layout (about 22 μm^2). Also, the critical charge estimated with the SPICE simulation of the cell (170fC) is close to the one approximately extracted from the LET_{th} (155fC).

The observed threshold at about 15 MeVcm^{2}mg^{-1} is considerably higher than what one would expect for

memory designs in the quarter micron technology. In ref. [10], which refers to a different design in the same technology, a LET_{th} of about 4 was measured. This difference is attributed to the increased transistor size, typical of the radiation tolerant layout practices, and therefore of the associated parasitic capacitance and drive capability. This translates into a decrease of the SEU sensitivity.

The simulation work reported in [12] shows the probabilities for energy depositions leading to upset in the LHC radiation environment. The probability for an energy deposition higher than 3MeV in the charge-collecting region (called "sensitive volume") is shown to be practically negligible. The measured LET threshold can be simply translated into energy deposition once the sensitive volume is defined. If we assume (as in [12]) a $1\mu m^3$ sensitive volume, then the threshold energy deposition for upset equals 3.5MeV. This leads to the first order conclusion that the standard static architecture could be robust enough not to experience a significant rate of SEU in LHC. This should be verified experimentally by a proton irradiation test, which is part of our future work plan.

The static "hard" register began to experience upsets only starting from the highest available LET of 89 $MeVcm^2mg^{-1}$. Even at that high LET, the cross-section was measured to be lower than 10^{-8} cm^2/bit. The proposed architecture is therefore very effective in protecting the content of memory elements not only at the LHC, but also in the radiation environment of Space, where heavy ions are present.

2) Clocked mode

Due to some limitations in our test setup, this measurement was limited to the dynamic and the static "hard" register. Also, it was not possible to precisely draw a cross-section curve, but only to extract the tendency for the SEU sensitivity.

The measurement on the dynamic shift register confirmed the general tendency that dynamic logic is significantly more sensitive to upsets than static logic. A considerable number of SEUs was already observable at the lowest LET available of 3.2 $MeVcm^2mg^{-1}$, from which one can deduce a critical charge lower than 35fC. SPICE simulations lead to an estimated value of about 34fC. With such a low threshold, the circuit would be quite sensitive to SEU in the LHC radiation environment (especially in the tracker), hence this architecture and more generally all dynamic architecture is not advisable or should be used with great care.

Also the static "hard" register showed a considerable number of errors when the LET was increased to 5.6 $MeVcm^2mg^{-1}$. This is due to the particular architecture of the cell, which was designed as a memory cell. During the write phase, the output node does not see any low resistance path towards Vdd or Vss for half of the clock period. Therefore, this node can temporarily change its logic state if hit by an ionising particle. This change does not affect the cell itself, which shows the correct output at the end of the write cycle. Nevertheless, in the specific case of the shift register, the momentary corruption of the output presents the wrong data at the input of the next cell. As this happens during the write cycle, the wrong data is latched into the next cell, originating an upset.

7. CONCLUSION

The use of radiation tolerant layout practices in a commercial quarter micron process has led to the design of devices and circuits able to stand total doses up to 30Mrad(SiO_2). Enclosed geometry NMOS and guardrings effectively eliminate any leakage current path. Therefore, the total dose limit comes from the radiation tolerance of the thin gate oxide, which is naturally extremely resistant to radiation effects.

As enclosed NMOS transistors are not commonly used in VLSI design, we had to develop a specific model for the evaluation of their effective aspect ratio, which is complicated by the presence of gate corners. The availability of such a model now allows designers to more comfortably deal with such transistor shape.

Standard linear NMOS transistors did not show any leakage current up to a total dose of 200krad(SiO_2). The transistor isolation was also not affected by such level of irradiation. Therefore this 0.25μm technology could safely be used, without any special layout practice, for designs requiring a low level of radiation tolerance.

The transistor noise in the quarter micron process is compatible with low noise analog design: the corner noise frequency is about 200kHz for the NMOS and 12kHz for the PMOS transistor. Irradiation up to 30Mrad(SiO_2) does not significantly affect these parameters.

The study of sensitivity to Single Event Effects has been performed with a heavy ion beam on shift registers designed using radiation tolerant layout practices. These circuits showed very good performance in terms of immunity to Single Event Latch-up. According to this result, SEL is not going to affect circuits implemented with these layout practices in LHC.

Single Event Upset heavily affects the performance of dynamic logic, but a high SEU threshold of 15 $MeVcm^2mg^{-1}$ was measured for the static shift register. An SEU-tolerant architecture has been developed and proved to be very effective in protecting the content of memory elements.

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