The NA48[1] LKr Calorimeter Readout Electronics

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Abstract

The NA48 experiment at the CERN SPS accelerator is making a measurement of the direct CP violation parameter $\varepsilon\prime/\varepsilon$ by comparing the four rates of decay of K_S and K_L into $2\pi^0$ and $\pi^+\pi^-$. To reconstruct the decays into $2\pi^0$ the information from the almost 13500 channels of a quasi-homogeneous liquid krypton electromagnetic calorimeter is used. The readout electronics of the calorimeter has been designed to provide a dynamic range from a few MeV to about 50 GeV energy deposition per cell, and to sustain a high rate of incident particles. The system is made by cold charge preamplifiers (working at 120°K), low-noise fast shapers followed by digitizer electronics at 40 MHz sampling rate that employs a gain switching technique to expand the dynamic range, where the gain can be selected for each sample individually (i.e. every 25 ns). To reduce the amount of data collected the system contains a zero suppression circuit based on halo expansion.

I. Introduction

The NA48 Collaboration has built a detector to measure the direct CP-violating parameter ε'/ε in neutral kaon decays[1].The accuracy of the measurement aim to be of the order of 2×10^{-4}. To measure the decays of K^0 into $\pi^0\pi^0$ it uses an electromagnetic calorimeter with liquid Krypton. The calorimeter has about 13,500 cells made by Cu-Be electrodes stretched in slight zig-zag along the beam axis. A photon/electron shower is reconstructed from the signals of a grid of about 11x11 cells around the impact point (due to the properties of the liquid, up to 40% of the shower energy is deposited in the impact cell).

The requirements for the calorimeter performance had influenced heavily the readout electronics. The LKr calorimeter has[2]:

- Energy resolution of $3.5\%/\sqrt{E}$ with a constant term of 0.5%, for a good background rejection and determination of the energy scale
- Time resolution of about 200 ps to correlate events with the trigger counters and to separate quasi-in-time accidental events
- Good space resolution ($\approx$ 1 mm) to reduce ambiguity in pairing photons and for mass resolution
- Noise level on one cell less than 5 MeV
- Maximum energy expected in one cell 50 GeV
- Cell to cell calibration of about 0.5%.

The readout uses a fast shaping technique and initial current readout with a cell capacity of about 200 pF to cope with the time resolution requirement and with high rate capability. The signals are then sampled at 40 MHz. The noise requirements lead to a dynamic range for the output signal of about 1:15000 i.e. 14 bits. The characteristics of the showers (one cell with a large signal and long tails with lower energy) require to sum up more than 100 cells to measure the energy of the shower and consequently the coherent noise must be kept very low. Cell to cell calibration means the need for a stable calibration system and accurate measurement of the calibration constants.

II. Preamplifiers

The preamplifiers[3] are mounted inside the cryostat in the 120°K liquid krypton, directly attached to the calorimeter strips. This choice has been done to minimize the charge transfer time and the noise. The circuit, shown in figure 1, is based on Si-JFET and integrates the anode current of 2.4 μA/GeV with a restoring time of 150 ns. The signal is then sent out using 50 Ω coaxial cables and feedthroughs on the top of the cryostat.

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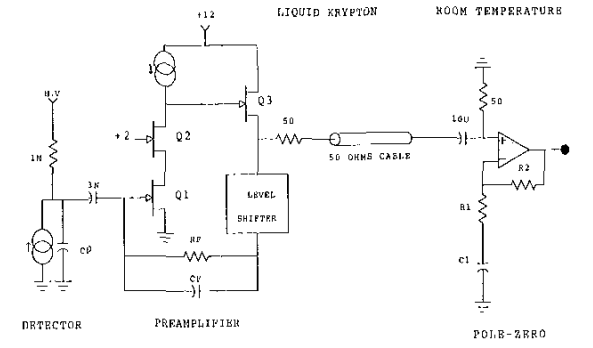

Figure 1: : Schematic of the preamplification and calibration circuit.

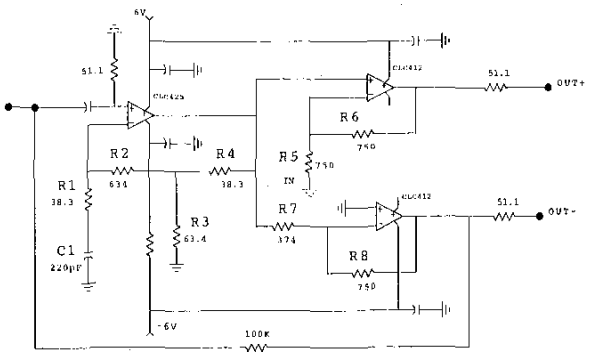

Figure 2: : Schematic of the line driver circuit.

To control the response uniformity and the stability over the whole calorimeter to better than 0.5% a precise and stable calibration system has been developed. This is implemented using about 2000 pulse generators (each one serving 8 channels) controlled by the voltage set with a single 15 bits DAC. A DMOS switch triggers an RC circuit injecting a signal similar to an ionization pulse. The preamplifiers and the calibration circuits are on the same boards, directly mounted on the calorimeter backplane.

The transconductances of the calibration circuit were measured globally to 0.5% using a precise current injector both at room temperature and at 120°K, and a table of conversion factors between reference voltages and current in the calorimeter has been derived.

III. Line Drivers

The signals coming out of the preamplifiers are sent to line driver boards[4]. These boards are located directly on the feedthroughs and share the Faraday cage made by the cryostat. Figure 2 shows the circuit diagram. The functionalities of these boards are multiple. By a proper choice of R1, R2 and C1 the circuit performs a pole-zero compensation, eliminating the τ=150 ns time constant of the preamplifier and replacing it with a faster τ=20 ns, thus recreating a triangular current signal as given by the calorimeter cell. The loss of amplitude in the signal due to the pole-zero cancellation is compensated by a similar amplification defined by R3 and R4.

Moreover, to improve the transmission of the signal from the cryostat to the readout, the second stage of the line driver is a differential line driver with an extra amplification to match the downstream dynamic range and the attenuation due to the cable termination.

IV. The Calorimeter Pipeline Digitizer

The CPD (Calorimeter Pipeline Digitizer[5][6]) modules perform the final shaping and the digitization of the calorimeter signal, together with the handling of the digital pipeline. At the time of the design of the module (1994) only a few low-cost 10 bit ADCs at 40 Msamples/s were available, although since then 12 bit ADCs have become available. To overcome this limitation in dynamic range, we have used a method of dynamic range expansion (dynamic range switching) which expands the dynamic range of the ADC with four bits in four gain ranges while maintaining the resolution of the ADC.

The initial shaper stage narrows the triangular signal coming from the line driver to increase the rate capability by avoiding pile-up and to improve the time resolution. The schematic of the shaper is shown in figure 3. The line driver signal is differentiated with a time constant of 20 ns by a passive network and fed both to a 9-pole Bessel filter and to three discriminators for the gain switching logic. The Bessel filter produces a pulse delayed by 50 ns with respect to the original input, with a 40 ns rise time, 73 ns FWHM and 160 ns at the baseline, followed by an undershoot at 3% of the pulse amplitude which lasts for a time equal to the drift time of the electrons across the calorimeter cell (about 2.85 μs). A separate copy of the shaped signal is also provided for building sum signals among channels for triggering purposes.

The output signal of the shaper is then amplified by a passive network with 4 different gains. The 3 gain ratios are given by the ratios of resistor values and stable to 0.07% while the spread in the gain ratios between different channels is less than 1%. The typical gains are equivalent to 3.6, 10.2, 24.6 and 60.5 MeV/ADC count. The decision of which gain range to use is made by the three discriminators mentioned above with different thresholds. The delay characteristic of the Bessel filter has been chosen so that there is sufficient time for the discriminators and logic circuit to settle.

Every 25 ns cycle of the centrally distributed experiment clock a different gain can be selected and the lowest gain reached for a given input pulse can be frozen for a programmable number of subsequent cycles. This allows to measure the relevant part of a pulse using the same amplification, thus simplifying the calibration needs. Moreover a programmable offsets can be applied to the selected gain signal to avoid underflow conditions in case of two signals coming close in time. Gain switching thresholds, offsets and gain hold periods are programmable via 6 bit DAC registers.

For compactness, power consumption and cost reduction, the collaboration has developed a customized mixed analog/digital BiCMOS ASIC, which is named KRYPTON, which contains the gain discriminators and gain switching

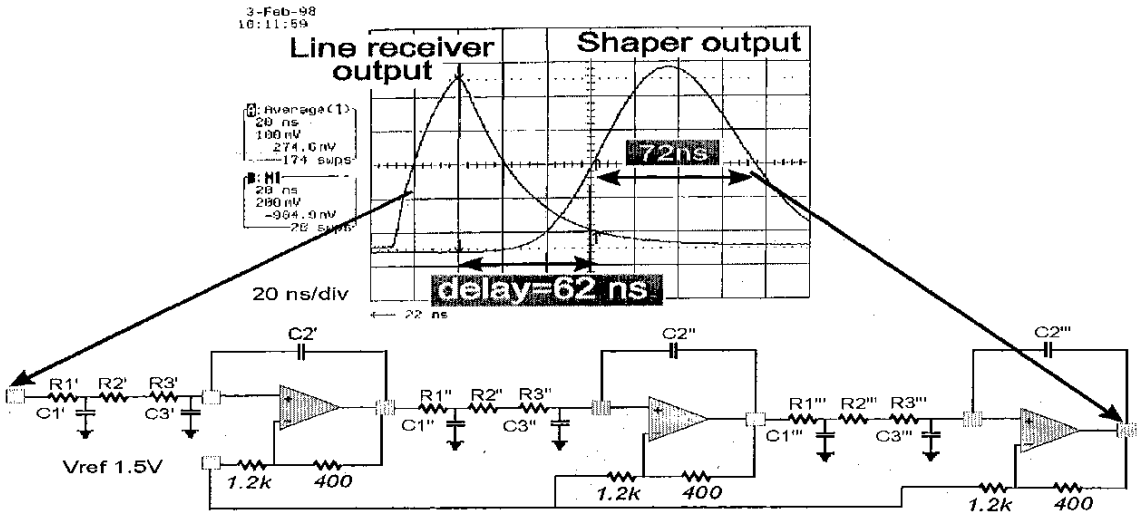

Figure 3: : Schematic or the shaper circuit and scope pictures of input and output signals..

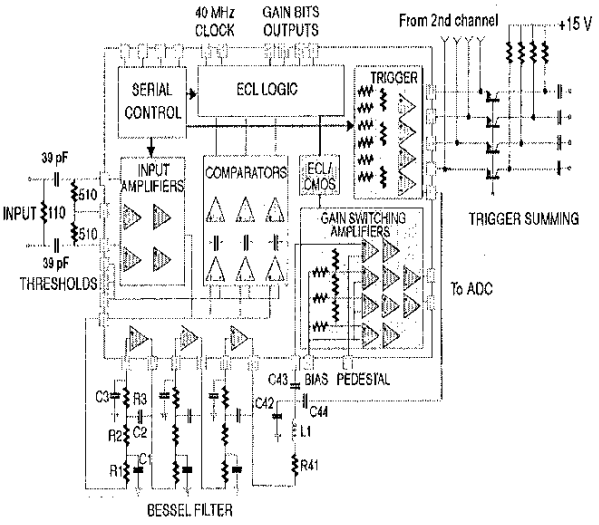

Figure 4: : Block diagram of the KRYPTON ASIC with external components.

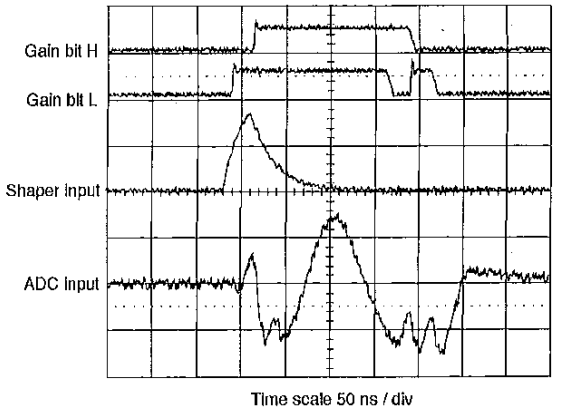

Figure 5: : Digital gain bits, signal at the Bessel filter input, and analog input at the ADC for a step input signal.

logic. Figure 4 shows the block diagram of the KRYPTON ASIC; figure 5 shows the signals entering and coming out from the ASIC for a step input signal.

The output of the switched gain amplifier is then sampled by a 10 bit 40 MHz FADC (Philips TDA8760) and the 2 bit information coming from the three discriminators is added to this word. Figure 6 shows a grid of 7x7 cells with the signals of a 100 GeV photon shower.

Modules have been built that combine the shaper, FADC and sample buffer memory for 64 channels. These modules are built in a 3-slot wide Fastbus board and each of them holds 32 daughter cards (CPDAS), 1 Fastbus decoding card (CPDFIC), 1 memory address controller (CPDMAC) and 1 trigger sum card (CPDTR). Each CPDAS (a double side mounted card serving two channels) contains shaper circuit, FADC and the pipeline with its control. The pipeline buffer is made by 16k $\times$ 12bit 15 ns SRAM which is logically divided into two 8k parts: the first is used as a 204.8 μs circular buffer while the second one is used as a linear buffer where selected data are transferred before being read out. The control of the pipeline buffer is made by a gate array called MIGA (Memory Interface Gate Array[7]) which performs three main operations:

- receives 12 bits of data from the FADC every 25 ns via the data bus. It sends 24 bits of multiplexed data into the SRAM every 50 ns.
- it moves data from the circular buffer into the linear one when a timestamp operation is dispatched by the

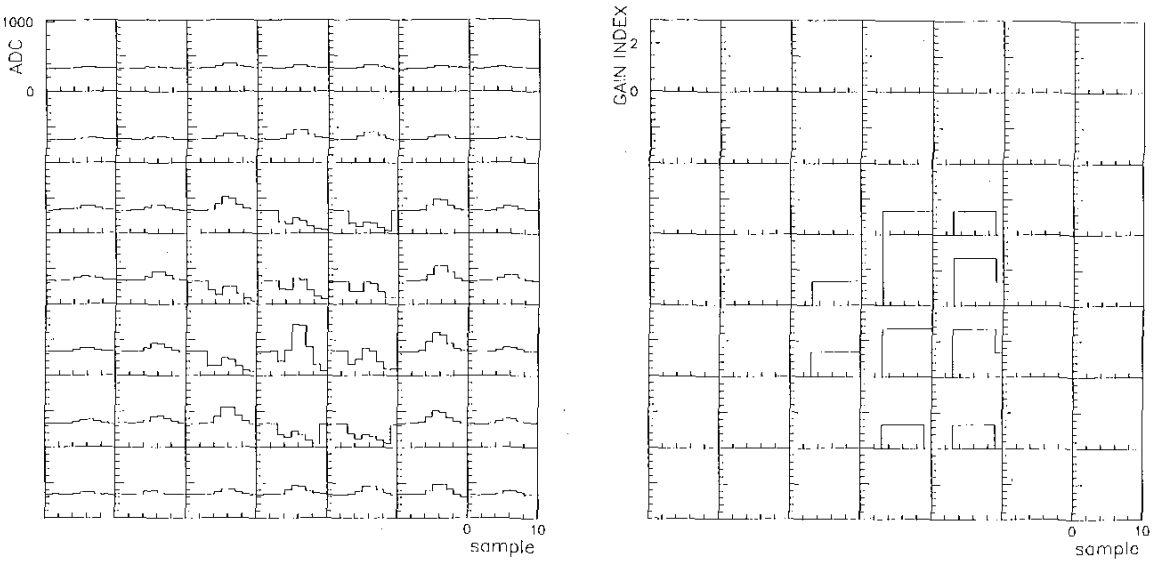

Figure 6: : Grid of 7x7 calorimeter cells with 10 consecutive samples of a 100 GeV photon shower. On the left the CPD ADC values, on the right the switching gain values.

CPDMAC card.

- it reads data from the linear buffer and sends them to the read-out data bus when the CPDMAC issues a *read linear buffer* command

The control of the memories in the CPD is common to all the channels. The implementation of such a control is the CPDMAC card. It is this card that actually divides the memory into circular and linear buffers and keeps track of the addresses to use for each buffer. The CPDFIC card contains a custom chip (Fastbus Slave Interface Chip[8]) which implements the Fastbus interface; it handles the serial loading of the parameters in the CPDAS cards. The CPDTR card provides the analog signals for the neutral trigger. Each CPD covers an 8x8 square matrix of calorimeter channels. The CPDTR provides 2x8 analog sums in both x and y view. Each input to the sum can be disabled or amplified with a programmable gain to equalize amplitudes. The signals used to make the sums are taken after the shaper, before the gain switching amplifier.

Due to the number of channels to be read, the experiment uses 216 CPD modules, for a total of 30 Fastbus crates. To address them as a Fastbus cluster[9] custom-made hardware couplers between successive Fastbus backplanes have been built (Cluster Interconnect[10]).

V. The Data Concentrator (DC)

The CPD module provides only the digitization phase. At a trigger rate of 10 kHz with 10 samples per channel the 216 CPDs produce about 4 GByte/s of data. Since the majority of the detector channels contains only pedestal, to reduce the amount of data read out and stored to a manageable amount, a scheme of zero suppression with a reduction factor of 20-30 is used.

A simple suppression scheme based on comparison of each individual signal with a threshold would discard the cells covered by the tail of the shower: even if the signals in these cells are quite small, they have to be taken into account in order to reach the desired energy resolution of $3.5\%/\sqrt{E}$ with a constant term of 0.5%. In order to keep them, a custom processing unit called TZSA (Trigger and Zero Suppression ASIC[11]), has been designed. The task of the TZSA is to mark the channels with an energy peak and in a second phase to mark the channels up to a given radius from this center. Thus the central peak plus the surrounding halo is marked for selective read-out. To achieve two-dimensional zero suppression, a technique borrowed from image processing has been used. A SIMD(Single Instruction Multiple Data) matrix of 128x128 1-bit PE's (Processing Elements), each connected to its orthogonal neighbours, performs an expansion algorithm around the outstanding peak (see fig. 7). Each TZSA consists of 16 PE's. The DC contains 1024 of these ASICs, housed on 32 Data Concentrator Processor modules, each module accepting inputs from 8 CPD modules. They are housed in two crates with Fastbus mechanics and a custom backplane that provides the interconnectivity necessary for the halo expansion.

During normal operation the CPDs can deliver up to 16 samples for each channel. From the CPDs the data are transferred to the DC using optical fibers. Each optical link has a capacity of 26 MB/s and carries the data of one CPD module (64 channels).

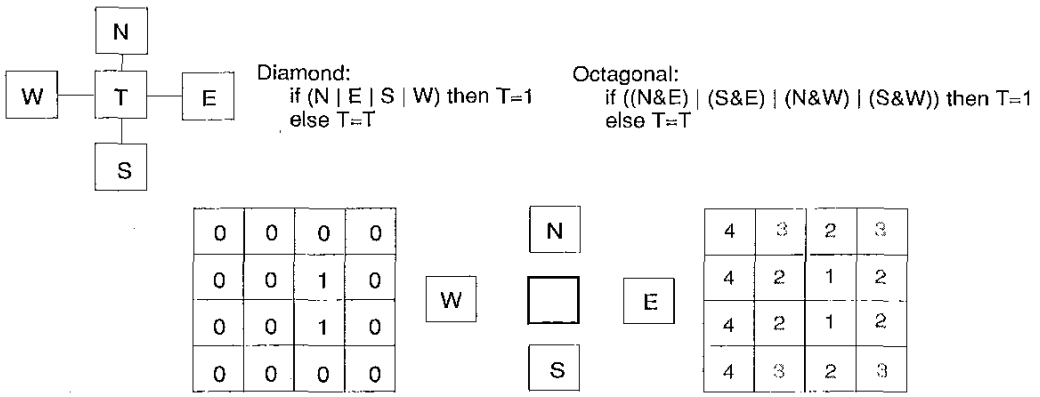

Figure 7: : DC halo expansion algorithm. On top the two possible algorithms are shown. Given a channel T, its neighbours are checked against thresholds; depending on the the result and algorithm used the channel T is marked to be read out. The process is repeated as many times as the radius of the desired halo. On bottom a 16-channel "hit" array with 2 hits (left side) turns into "mark" array via the halo expansion algorithm (right side).

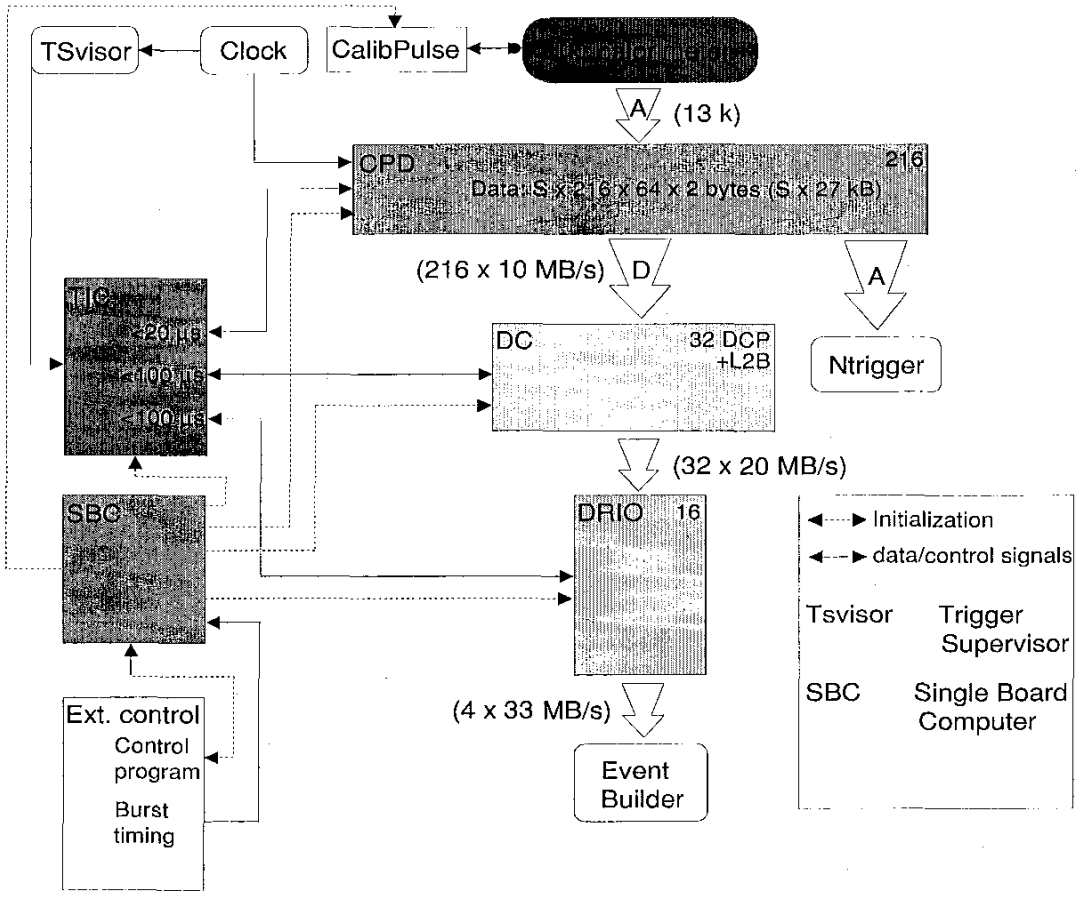

Figure 8: : Block diagram of the data and control flow in the readout system.

VI. Data flow

Every 25 ns a 12 bit word (10-bit FADC sample + 2-bit gain index) is written into the circular buffer of the CPDs. In the entire experiment the digitization and sample storage are driven by a common 40 MHz clock. This allows the direct translation of a second level trigger given as a timestamp in a circular buffer address.

Figure 8 shows the readout and control flows through the electronics. Upon arrival of a trigger, the trigger interface (TIC, a module based on CES RIO8260 processor[12] with custom I/O interface) selects a time window of ten samples (ten 12-bit words) around the trigger timestamp to be copied for all channels from the circular buffer into the linear one. This information is passed to the CPDs via normal Fastbus bus. From the linear buffer the samples are later moved into the 9-stage digital pipeline of the DC via optical links. The samples of the cells surviving the halo zero suppression are sent via optical links to 16 Data RIO boards (DRIO modules based on CES RIO8260[12] with custom I/O interfaces). From here the "calorimeter event" data are sent to the experiment event builder via 4 custom-made 16-bit wide ECL links capable of a maximum transfer rate of 33 MB/s.

VII. Conclusions and Performance

To summarize, the NA48 collaboration has built a readout system for its liquid Krypton electromagnetic calorimeter that provides a dynamic range from a few MeV to about 50 GeV energy deposition per cell, and copes with a high rate of incident particles. The system has been built with low noise fast shaper circuit followed by a 1-of-4 gain amplification and 40 MHz FADC. The gain can be selected for each sample individually. To keep the amount of data collected manageable, a zero-suppression circuit based on halo expansion has been built. The system hase been in use since 1997; during 1998 it worked at an average trigger rate of 8 kHz giving a data rate into the event builder of about 170 MB/s.

VIII. Acknowledgments

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