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Test results of the ALICE SDD electronic readout prototypes

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Abstract

The first prototypes of the front-end electronic of the ALICE silicon drift detectors has been designed and tested. The integrated circuits have been designed using state-of-the-art technologies and, for the analog parts, with radiation-tolerant design techniques. In this paper, the test results of the building blocks of the PASCAL chip and the first prototype of the AMBRA chip are presented. The prototypes fully respect the ALICE requirements; owing to the use of deep-submicron technologies together with radiation-tolerant layout techniques, the prototypes have shown a tolerance to a radiation dose much higher than the one foreseen for the ALICE environment.

Summary

The design of the readout electronic for the ALICE silicon drift detector is a very challenging task, due on one side to the huge amount of data produced by those detectors (256 10-bit words for each detector anode, in the case of the ALICE SDDs) and on the other hand to the stringent constraints in term of space, power consumption and radiation hardness. The chosen architecture is based on 2 integrated circuits, PASCAL and AMBRA. It works in two different phases: during the acquisition phase the detector signal is amplified and stored into a fast analogue memory; when the trigger signal validates the data, the readout phase starts and the analogue information in the memory is

converted by an A/D converter and transferred into a digital multi-event buffer. All the analogue functions (amplification, storage and conversion) are embedded in a single chip (PASCAL), while the digital event buffer, plus most of the control logic, are on a separate chip (AMBRA).

The analogue memory is of the write-voltage read-voltage type; it uses MOS capacitors as storage elements in order to save space. The intrinsec MOS capacitor non-linearity limits the dynamic range to about 1.5 volts over a 2.5 power supply. The A/D converter is of the switched-capacitor, successive approximation type; the 10 bit resolution is obtained by an 8 bit main DAC followed by a 2 bit secondary DAC with direct coupling.

Prototypes of the analogue memory and the A/D converter in a commercial 0.25 um technology with radiation tolerant design techniques have been designed and tested. The results show that both prototypes fully satisfy the ALICE requirements in terms of performances and power consumption. Owing to the adopted radiation tolerant technique, the prototypes do not show any significant degradation after a total dose up to 10 Mrads.

The first prototype of the PASCAL chip is currently under production. The first prototype of the AMBRA chip has been designed and tested in a 0.35 um technology. The chips fully satisfy the ALICE requirements; radiation tests are ongoing in order to check the radiation tolerance of a fully digital deep submicron technology without radiation tolerant layout techniques.