An automated test bench for the ATLAS shapers and SCAs

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Abstract:

An automated test bench has been developed for the ATLAS shapers and the analog memory integrated circuits. The measurement setup is based on a Labview application and the testing printed circuit board has a GPIB bus interface. The testing program works a handshake with a four axis table-top mounted robot, which handles carefully the QFP100 packaged circuits during the positionning pick-up and sorting phase. This test bench provides an autonomy of 660 chips.

I) Introduction :

Testing analog integrated circuits for ATLAS front end is an important challenge regarding the volume of the production needed (200,000 channels), the analog features, and the packaging used. An automated test station has been developed for the shapers and analog memories also called switched capacitors array (SCA). Both circuits are packaged in the QFP100 format to save space on the front end board and to ease the interconnection of the circuits on the front-end board.
This test station consists of an automated measuring system in handshake communication via a series bus with a manipulating robot.

II) The shaper test board:

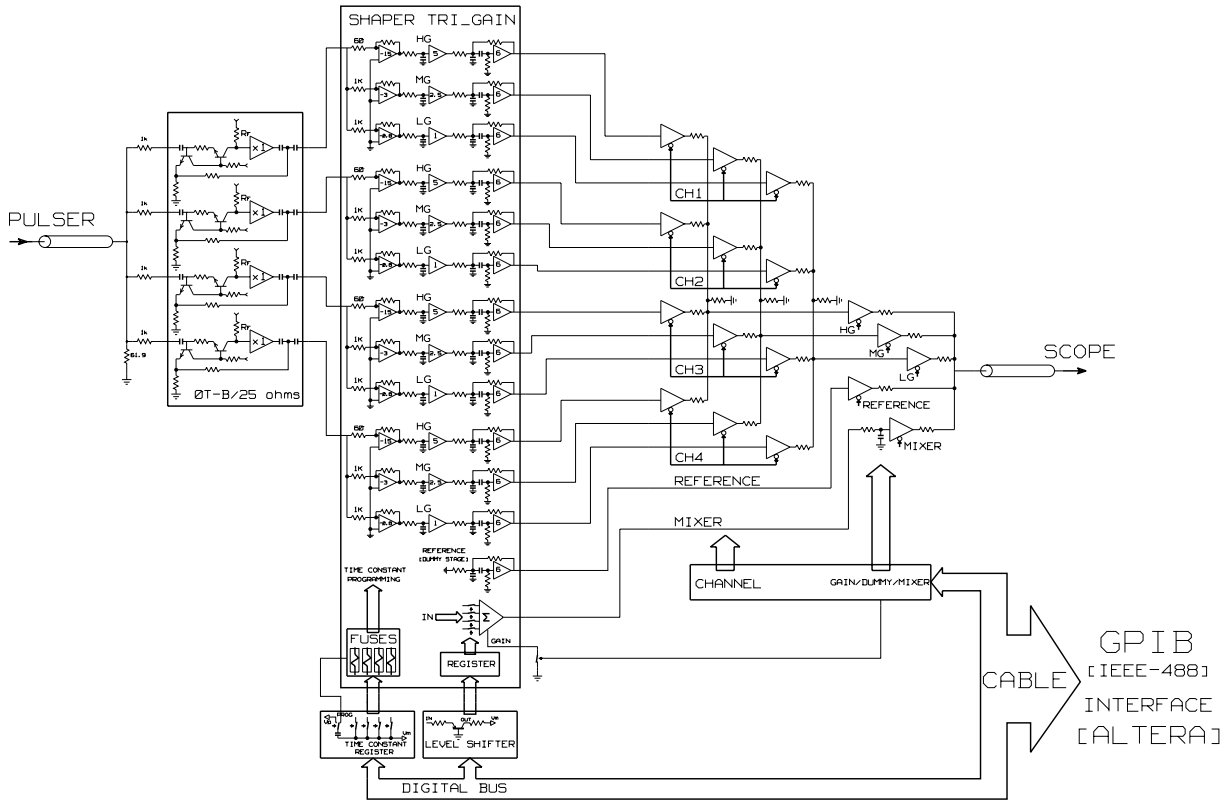

Figure 1: Shaper test board schematic

A specific test card has been designed to test the shaper production (QFP-100 package) with the LabView environment. To be as close as possible to the real input signal shape, a four channel 0T-hybrid with a common "ATLAS like" calibration input signal generates the pulses to be fed into the four shaper channels. The shaper chip is mounted on a high reliability QFP socket ("Clamshell" from Yamaichi or equivalent). This socket is plugged on a specific support soldered on the test card; therefore changing socket is easy in case of contact failure.

An analog multiplexer, designed with operational amplifiers (CLC410 with disable input), connects one of the 14 shaper outputs (4x3 Gains, Analog Mixer and Reference [dummy stage]) to the oscilloscope.
Two registers are implemented on the board :

- four bits to select the multiplexer channel
- four bits to select the time constant with an extra bit to burn the fuses and fix the time constant (time constant programming)
- a bank of level-shifters is used to enable or disable the mixer inputs via the internal shaper register and analog switches.

Some ancillary logic generates the "handshake dialogue" with the GPIB [IEEE-488] interface via a flat cable. This interface is implemented, on a second card, in a FPGA [ALTERA] with external logic drivers. Figure 1 presents the testing board architecture. We used « Rad-tolerant » components on the testing board, in prospect to employ the same board for shapers irradiations (neutrons and gammas).

III) MEASUREMENT PROCEDURE

The time constant is calculated for every chip to find a peaking time very close to a well defined target value.
For every gain and for each channel, the input signal amplitude is controlled to reach the highest amplitude at the output, in the linear range. Then the following parameters are measured and stored in the database: the power dissipation, the peaking time, the base-line and its dispersion, the time constant used, and the circuit final qualification (good or not). This qualification results from a comparison of each measured parameters against a well-known template. The amplitude and time parameters are measured using the digital scope functions. For each successfully tested circuit, the time constant is fixed by blowing its integrated fuses.All the measurement software for the shaper is written in Labview.

IV) PICK AND PLACE AUTOMATION

1) Pick and place system

The FPQ100 package used for shapers and SCA has the benefit of saving space on the front-end board, but it presents the drawback of fragile leads. Therefore great care must be taken to hold them during the production tests. Packaged circuits are delivered on 6*11 unit plates. We use a table-top mounted Scara robot from Adept Technology to handle them for testing and sorting. Figure 2 shows its side view.

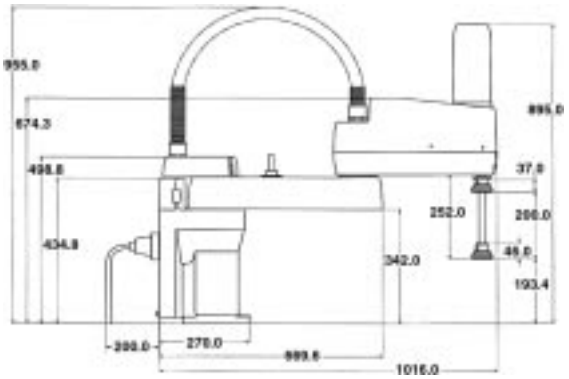

Figure 2: Robot side view

Over the robot working area 20 trays are laid out as in figure 3. On the right side are settled 10 trays filled with circuits to be tested.

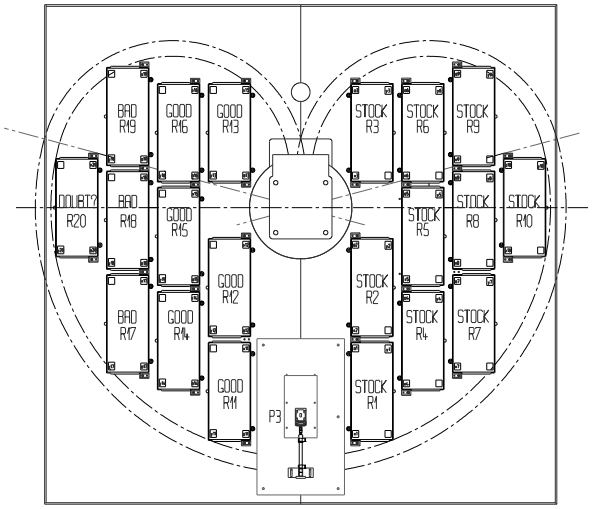

Figure 3 : Trays in the robot working area.

On the left are those categorized after testing: there is a set of six trays for successfully tested circuits, a second set of three trays for chips with at least one analog parameter measured out of range; the last tray receives dubious chips found regarding the logic register check or the fuse blowing steps.
To ensure the package leads integrity, great care has been taken against mechanical stress when handling chips. A special silicon conductor sucker is used to approach .5mm close to the chips. This contact point is grounded via the robot arms (figure 4) in order to avoid electric static discharges (ESD) while preserving a smoothly approach.

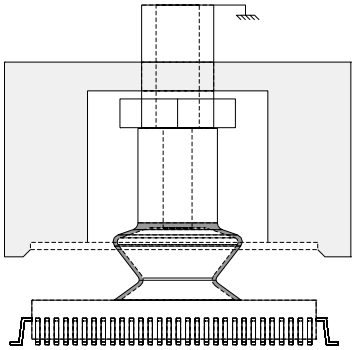

Figure 4 : Picking up a chip with a suction pad

Then an electric control vacuum pump holds the chips via the suction pad without any stress. A self aligned cavity is added to compensate position errors in the horizontal plane. The package to-be-tested is then moved onto the test board. A “zero insertion force” socket is used at the test point to avoid any damage on the chip leads. Then a pneumatic jack secures the socket before measuring phase starts. The socket “open” and “closed” positions controlled via two inductive sensors fixed on the jack (figure 5). The measuring computer communicates with the robot controller via a RS232 series port, to define when to start measuring and what is the final result.

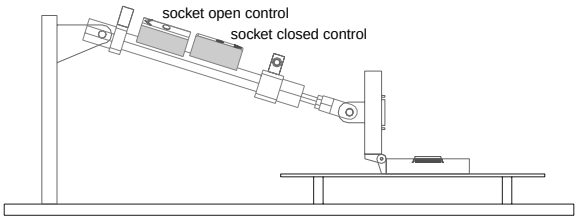

Figure 5: A pneumatic jack to open or close the socket.

2)Accuracy and security

The robot position repeatability is +/- 0.02mm in the (x,y) horizontal plane, +/- 0.01mm in the z vertical direction, and +/- 0.03° in the theta position around z axis. The maximum speed is better than 1m/s or 360°/s. We work at a medium speed, which is fast enough to reach the most distant point from the testing board in less than 1s.
Three optical fiber photoelectric switches (OMRON E3X-NH) have been fixed to the socket to control the circuit insertion as shown in figure 6. Two of them control that a plan .5mm above the package of the circuit remains clear. The third optical switch is an extra security element to control that the socket is really empty before inserting another one.

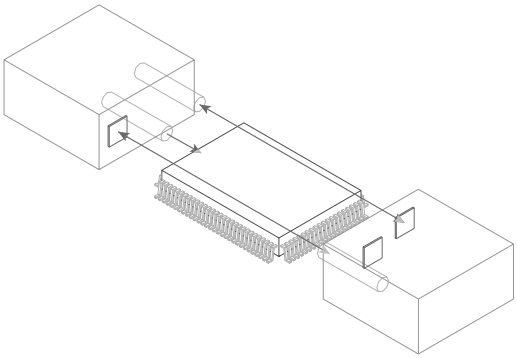

Figure 6: Optical control of package in the test socket.

An overview block diagram of the test station is shown at figure 7.

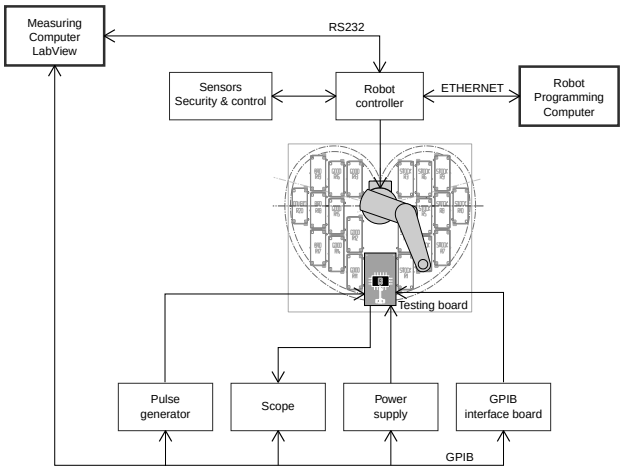

Figure 7: Test bench overview block diagram

V) CONCLUSION

This test bench is now in its evaluation phase in Grenoble with shaper circuits. It should run 8 hours/day during 7months for shapers testing, and more than 9 months for the SCA that needs a longer testing time per chips.