A 128 CHANNELS ANALOG READOUT CHIP (APVD_DC) FOR DC-COUPLED SILICON DETECTORS OF THE CMS TRACKER

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Abstract

The APVD_DC realised in the DMILL technology is a radiation-hard integrated circuit for front-end readout electronics of the silicon tracker of CMS.

DC-coupled silicon microstrip detectors have significant economical advantages compared to AC-coupled devices mainly due to their less complex fabrication process and better yield. The APVD_DC allows the use of DC-coupled silicon detectors with significant leakage currents as it is expected due to irradiation after several years of LHC operation.

In this paper, a solution is presented with an active individual leakage current compensation technique for each input channel. The APVD_DC contains 128 identical analogue channels, each one composed of a low noise preamplifier, a CR-RC shaper, a 160 cells-deep analogue pipeline and an analogue signal processing stage. A deconvolution filter at the latest stage recuperates the initial fast response function of a silicon detector and confines it to one LHC bunch crossing. The 128 analogue channels are readout by a serial output via a high-speed analogue multiplexer. Slow control is implemented on the chip using an I2C serial bus, which allows to bias, to configure the chip and to run the internal calibration system. A current compensation circuit is added in front of every preamplifier to sink the leakage current coming from the detector. Good performance of the circuit has been measured on prototypes for leakage currents between 0 and up to 10 μA.

1. INTRODUCTION

In the CMS inner tracker, several millions channels of silicon detectors are foreseen to be installed. Front-end electronics can be AC coupled as well as DC coupled to these detectors. The AC coupling technique is widely used for readout of silicon detectors with coupling capacitors and bias resistors integrated on the detector. However, AC coupled silicon microstrip detectors are more complex and expensive in fabrication than DC coupled detectors. The APVD_DC has been developed to allow the use of DC coupled silicon detectors with significant leakage currents as expected due to irradiation after several years of LHC operation.

In this paper, after a brief introduction of the APVD_DC architecture, only the charge sensitive preamplifier with its active leakage current compensation is discussed. More detailed information concerning APV type circuits can be found in [1, 2, 3].

The second objective of this paper is to describe a fully stabilised front-end readout electronic in DMILL technology. In previous versions of the APVD some instability problems were encountered. The problem becomes prominent especially at high bias current settings. This paper is focused on a study of this phenomenon by results of tests and extensive simulations. Finally a solution which resolves the oscillation problem of the circuit is described. This solution has been implemented in the most recent submission.

2. APVD_DC DESIGN FEATURES

The APVD_DC is a second generation of the APVD [2, 3] rad-hard front-end readout chip developed in the DMILL process, after it has been transferred from the former version of the APV6 [1] realised in the HARRIS technology.

As other members of the APV family, the APVD_DC contains 128 identical analogue channels. The current pulse delivered by the detector is transformed into voltage by a charge preamplifier and then amplified and filtered by a CR-RC shaper. The signals are buffered by a source follower that is connected to the analogue pipeline, the ADB (Analogue Delay Buffer), where the signals are sampled and stored at 40 MHz. On receipt of a first level trigger, the signals are read and processed by the APSP (Analogue Pulse Shape Processor). The analogue output current signal is read-out serially at 20 MHz. The control of the circuit is provided by several blocks. The I2C interface allows programming of the main parameters of the circuit for the slow control. It also generates signals cycling the APSP. The pipeline control logic (PCL) controls the writing and the reading sequences of the analogue pipeline. The addresses of the tagged cells are stored in a FIFO. The pulse generation unit generates calibration pulses for testing the analogue chain. The bias generator block is a set of RAM based registers and DAC's, and it generates all the bias currents and control voltages for the analogue blocks and some digital patterns for the calibration pulse generator. It is programmed through the I2C controller.

In particular, in the APVD_DC circuit, a current compensation circuit is added in front of every preamplifier to sink the possible leakage current coming from the detector. Fig. 1 presents the general architecture of the APVD_DC circuit.

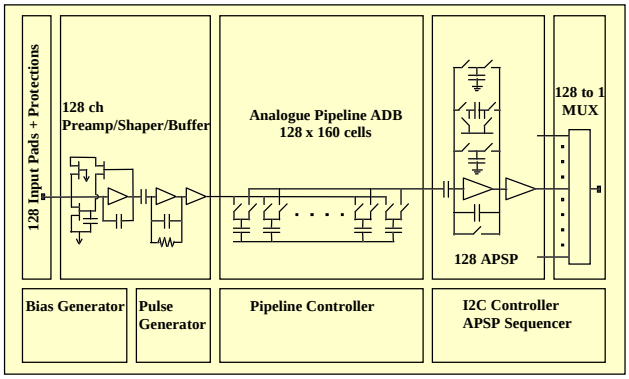

Fig. 1 APVD_DC architecture

3. FRONT-END ELECTRONICS WITH LEAKAGE CURRENT COMPENSATION

The transistor level circuit diagram of the front-end part is shown in figure 2.

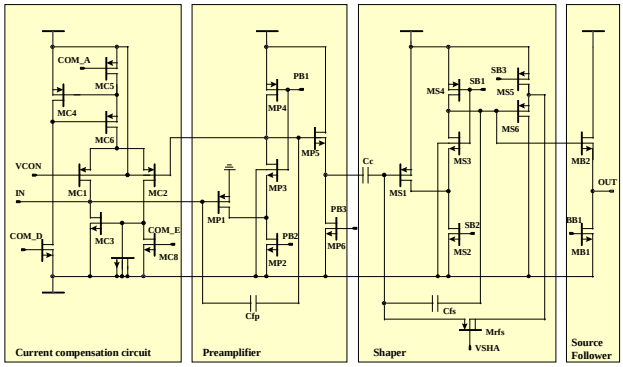

Fig. 2 Front-end amplifier circuit diagram

The front-end electronic circuit contains a preamplifier with associated circuitry for leakage current compensation, a shaper and a buffer to drive the pipeline capacitor.

The preamplifier is a single ended folded cascode structure with 300 pF feedback capacitor buffered by a simple source follower. The input PMOS transistor MP1 with size of 1540 μm /1.2 μm is biased at 250 μA in a trade off between noise matching and power consumption. The DC operating point of the high impedance output (the drain of transistor MP3) is set by means of the differential pair MC1 and MC2 with an external voltage VCON. The transistors MC1 and MC2 are designed to operate in weak inversion region with drain currents about 10 nA. In order to achieve the required precision for the current mirroring, the differential pair (MC1, MC2) is biased by a regulated cascode current source MC4-MC6. The DC leakage current can be sinked by a NMOS current source with the transistor MC3.

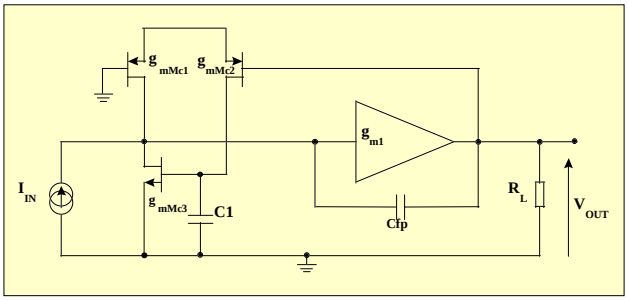

Fig. 3 Simplified small-signal equivalent circuit of the preamplifier

Figure 3 shows a simplified closed-loop small-signal equivalent circuit of the preamplifier with the leakage current compensation circuit.

The transfer function H(S) of the preamplifier is written as follow[4]:

$$H(\mathbf{s}) = \frac{V_{OUT}(\mathbf{s})}{I_{IN}(\mathbf{s})} = \frac{2C_1\,\mathbf{s}}{g_{m_{MC1}} + g_{m_{MC3}} + g_{m_{MC1}} C_1\,\mathbf{s} + 2C_1\,C_{fp}\,\mathbf{s}^2}$$

where $g_{m_{MC1}}$ and $g_{m_{MC3}}$ are small signal transconductances of transistors accordingly MC1 and MC3. The stability criterion is given by [4, 5]:

$$\frac{C_1}{g_{m_{MC3}}} >> 2\frac{C_{fp}}{g_{m_{MC1}}}$$

Noise performance of a charge amplifier is determined by two factors: the intrinsic noise generated by the amplifier itself and the signal impedance seen by the amplifier input, in other words the noise matching conditions must be satisfied. As it is well known, both the optimal noise matching condition and the total noise contribution of the charge preamplifier are mainly determined by the input transistor. The choice of the input transistor as well as its bias current is a key point in the design.

The charge preamplifier is followed by the first order CR-RC semi-Gaussian shaping amplifier. The transfer function of the shaping amplifier is given by the following expression:

$$H_{shaping}(\mathbf{s}) = \frac{V_{OUT}(\mathbf{s})}{V_{IN}(\mathbf{s})} = A_{vs}\frac{\mathbf{s}/\omega_c}{\left(1+\mathbf{s}/\omega_c\right)^2}$$

where A_{vs} represents the DC gain and ω_c is the central frequency of the shaping amplifier. The shaping time can be calculated by Laplace's transform when at the input a step signal is applied.

$$\tau = \frac{1}{\omega_c} = \frac{\left(C_c + C_{is}\right) + \left(C_h + C_{strav}\right)}{g_{m_{MS1}}(1+k)}$$

where $g_{m_{MS1}}$ is the transconductance of the input transistor in the shaper MS1. C_{is} is the input capacitance of the shaping amplifier and C_{strav} is the stray capacitance seen at the amplifier's output. The factor k in the above equation can be calculated by:

$$k = \frac{1}{\sqrt{1 + C_{fs}\left(\frac{1}{C_c + C_{is}} + \frac{1}{C_h + C_{strav}}\right)}}$$

The buffer is a simple source follower having strength to drive pipeline capacitance.

A very good functionality of the leakage current compensation stage has been demonstrated by a few channel prototype of the front-end amplifier. Figure 4 shows measured ENC of the prototype DC coupled charge amplifier as a function of detector capacitance with different leakage currents. The maximum leakage current which can sunk by the amplifier is 13 μA.

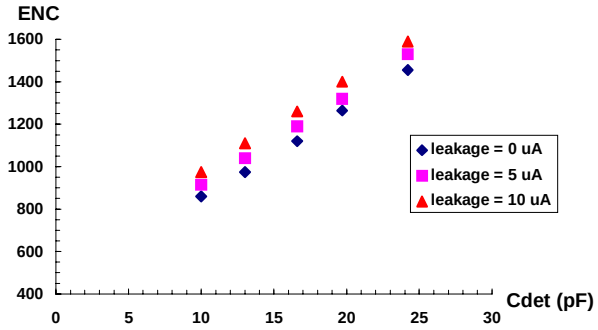

Fig. 4 Measured ENC vs. C_{det} for three values of the leakage currents

$I_{leakage}$ = 0 μA	ENC = 446 e^- + 42/pF
$I_{leakage}$ = 5 μA	ENC = 506 e^- + 42/pF
$I_{leakage}$ = 10 μA	ENC = 573 e^- + 42/pF

4. STABILITY DESIGN

Previously submitted APVD circuits suffer from an instability problem. Laboratory evaluations have shown that instability conditions were satisfied in the analogue input stage when front-end channels were biased at high current values. Three main points were investigated in detail to identify causes of the instability:

- Capacitive coupling coming from back side silicon substrate,
- Capacitive coupling between adjacent channels,
- Resistivity coupling via imperfect power lines.

First, measurements were performed to a few chips before and after thinning backside substrate (the total thickness was scaled down from 600 μm to 250 μm and then to 100 μm). The purpose of these tests was to evaluate impact of capacitive feedback via the backside substrate. Results have shown that the feedback via backside substrate had little influence to the stability of the circuit.

Second, the input transistor of the preamplifier can be blocked by bonding its input to a positive DC potential point. Using this method, it was found that there was a critical number of channels to initiate the oscillation in nominal bias conditions. Further measurements have shown that the oscillation is a function of total currents passed through power lines. It was demonstrated by blocking only even (or odd) channels that the coupling between adjacent channels was not critical in the design.

Third, it turned out that the instability problem was essentially caused by imperfect ground and power supply connections. Indeed, this has been demonstrated by several measurements with different impedance

configurations for the power lines. Two different PCB boards as support for test chips were used, one with backside ground plane and one without. When the common impedances are reduced near to several mΩ on the board equipped with the ground plane, the oscillation is completely stopped.

Because there are number of connections to power supply lines in the analogue channel and because phase shifts in different points of the circuit are significant, it is difficult to investigate the problem of oscillation completely in an analytic way. Instead appropriate simulation models of the imperfect ground and imperfect power supply lines were created. Resistances of the imperfect ground and power supplies were dispatched in 3 parts. First, resistances on chip were calculated by using sheet resistance values of metal levels. Calculated resistances were divided into several parts placed between every two suspected trouble spots of the design. Then, resistances and inductances represented by bonding wires were estimated and included to the simulation. Finally PCB and system cables resistivity was estimated. Ultimately decoupling capacitances with their parasitics were added yielding in a complete model of power supplies connections. Figure 5 presents the model.

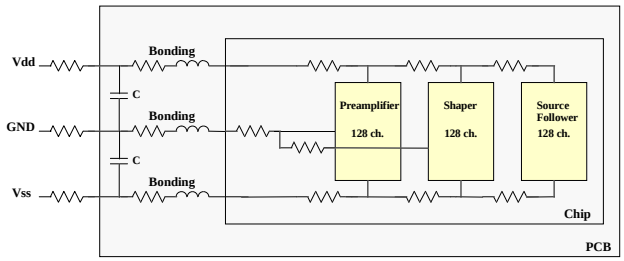

Fig. 5 Simulation model

On the base of that model the most critical parts of the previous APVD designs were identified. It turned out that three points in the design are crucial. They are:

- Bulk and source connection of both preamplifier and shaper input transistors and the connection of the output source follower to power supply lines,
- Large load capacitance value formed by the pipeline stray capacitance and the ADB hold capacitor,
- Large value of the AC current flow through positive power supply line charging this capacitor which is seen by the output of the source follower.

Due to distributed resistors present on the power lines, a small signal voltage accumulates on terminals of the input transistors in both preamplifier and shaper. Because in the previous design bulk and source were connected to different power line, the accumulated voltage was amplified via G_{mB}. Significant role of the G_{mB} parameter of the transistor was demonstrated. Apart of the feedback paths aforementioned it was also observed positive resistive coupling between the source of the input transistor in the shaper and the input transistor in the preamplifier, as well as some possible positive capacitive feedback have been identified. Other capacitive feedback loops are a feedback path via lost silicon of the chip and a feedback via backside substrate. Taking into account these points, verified by simulations, the following changes were introduced to the APVD_DC design (Fig. 2):

1. The bulk of the input transistor in the preamplifier has been connected to GND. Noise contribution is slightly increased (<1%).
2. The source and bulk of the input transistor in the shaper have been connected to Vdd. This modification forces another change, because of the DC level shift. In the shaper PMOS type source follower and PMOS feedback transistor have been used.
3. Value of the feedback capacitance in the shaper has been increased in order to improve the stability. This change has entailed modifications of the capacitors in the feedback of the preamplifier and coupling capacitance between the preamplifier and shaper.
4. Vdd power line has been split in two paths in order to reduce common resistance on this line.
5. The design of the ADB cell has been changed to minimise the total capacitance seen by the output source follower.
6. Parasitic pole of the preamplifier has been pushed further out in the frequency scale. The G_m of the cascode transistor in the preamplifier has been increased by both increasing its W/L and bias current.
7. Almost all large dimension current source transistors situated in critical places have been redesigned in a special parallel layout in order to reduce their C_{db} capacitance.
8. To avoid a capacitance coupling three guard-rings have been employed in the design. A guard ring used as a shielding has been formed by a collector well (Collsink) implanted inside Genpmos wreath down to the SOI level.
9. The 128 channel analogue input pads have been modified in a way allowing for suppressing the capacitive coupling to the back silicon.

Several simulations have been performed to verify the increased immunity to oscillation. Results of the modified design show a total stability of the circuit. They should insure a perfect stability even if several APVD_DC chips would be mounted on the same PCB/hybrid. The circuit submitted on the last June will be delivered on October; this allows us to confirm the stability of the new design.

5. CONCLUSIONS

A 128 channels analogue readout chip (APVD_DC) for DC-coupled silicon detectors of the CMS tracker is presented. It could offer an economic solution for the CMS silicon tracker.

The detailed stability study is also presented in this paper. All of the modifications of the circuit allow us to have a readout electronic satisfying the requirements of the CMS silicon tracker in the DMILL technology.

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REFERENCES

[1] M. French *et al*., 'APV6-RH A 128 Channel Readout Chip for the Silicon Tracker in CMS', Proceedings of the 2nd Workshop on Electronics for LHC Experiments, Balaton, September 23-27, 1996, pp. 463-467

[2] R. Turchetta *et al*., 'APVD: a CMOS Mixed Analogue-Digital Circuit for the Silicon Tracker in CMS', Proceedings of the 3rd Workshop on Electronics for LHC Experiments, London, September 22-26, 1997, pp. 163-167

[3] P. Schmitt *et al*., 'Performance of a CMOS Mixed Analogue-Digital Circuit (APVD) For the Silicon Tracker of CMS', Proceedings of the 4th Workshop on Electronics for LHC Experiments, Rome, September 21-25, 1998, pp. 180-184

[4] F. Krummenacher, 'Pixel Detectors with Local Intelligence: an IC Designer Point of View', Nuclear Instruments and Methods in Physics Research, A305, 1991, pp. 527-532

[5] Y. Hu and R. Turchetta, 'Design of a High Performance, Low Noise Charge Preamplifier with DC Coupling to Particle Silicon Detectors in CMOS Technology', Proceedings of the 4th Workshop on Electronics for LHC Experiments, Rome, September 21-25, 1998, pp. 452-455